METHOD OF FINE REDISTRIBUTION INTERCONNECT FORMATION FOR ADVANCED PACKAGING APPLICATIONS

BACKGROUND

Field

[0001] Embodiments of the present disclosure generally relate to packaging of electrical components. More specifically, aspects of the disclosure relate to fine redistribution techniques to establish interconnection between electronic components in packaging applications.

Description of the Related Art

[0002] As time progresses, the need for advanced packing of electronic components increases. Technology increases in areas such as microelectronics are used in a variety of applications, from smart phones, wearable devices, computers, and other consumable electronics to automotive, transportation, energy, aerospace and defense. Going forward, with exponential growth of big data, evolution of the Internet of Things (IoT) and advancement in Artificial Intelligence (AI), there is an ever increasing need to provide more efficient microelectronics that produce needed results while being energy efficient and cost effective.

[0003] While conventional methods of packaging electronic components may be acceptable in one year, successive years require large increases in efficiency. As a non-limiting embodiment, die sizes for electronic components are based upon a resolution defined as line/space (L/S). Roadmaps of needed resolutions are decreasing from 25/25 μm for embedded die application to a much smaller 15/15 μm in panel-level packaging.

[0004] Resolutions for technologies other than embedded die construction are even more restrictive. For organic panel interposer technology, required resolution progresses from 10/10 μm to 2/2 μm in upcoming years. Resolution based technologies currently used are not capable of production of the electronic components of the future.

[0005] Currently, there are no cost-effective high-density redistribution line technologies for sub-micron line/space resolution in the packaging industry. While

technologies do exist, such as redistribution layer technologies for silicon interposer and embedded copper trace technologies, these types of technologies are extremely cost inefficient and not applicable to large scale manufacturing.

[0006] Referring to FIG. 1, a comparison of redistribution line technologies is presented. For silicon interposer technologies, the applicable platform is a wafer platform and the maximum routing/millimeter is 1300 (L/S .4/.4 μm). Cost of such silicon interposer technologies is higher and RF insertion loss at high frequency is relatively high.

[0007] Further referring to FIG 1, embedded copper trace uses a polymer with a conformal seed material. Like the silicon interposer technology, the embedded copper trace technology can be used on a wafer and may achieve a maximum routing/millimeter of 300 (LS 2/1 μm). While the cost of embedded coper trace technology can be relatively low additional steps are involved in removing copper overburden and seed layer due to the dual damascene based process flow. Such increased number of steps hampers the overall time frames for production. Necessity of employing non-standard equipment in the packaging industry, i.e. chemical mechanical polishing (CMP) tool, for copper overburden and seed layer removal also limits the overall economic viability of this method.

[0008] For illustrated Semi-Additive Process (SAP) Cu trace technology, such methods are applicable to wafer technology and may achieve a maximum routing/millimeter of 500 (L/S 1/1 μm) with low cost. SAP Cu trace technology, however, has a significant drawback in having a high RF insertion loss at high frequency. Each of the major high density redistribution line technologies has at least one major drawback, hampering their use in the ever increasing need for high density packaging.

[0009] There is a need to provide technology that will provide for required resolution trends (line/space) of the future.

[0010] These technologies should be efficient for large scale production facilities as well as economic for production requirements of the future.

SUMMARY

[0011] In one example embodiment, a method for producing an electrical component is disclosed, comprising: providing a polyimide substrate, coating at least one side of the polyimide substrate with an adhesion layer comprising molybdenum, coating the adhesion layer with a copper seed layer, covering at least a portion of the copper seed layer with a coating of photoresist, removing a section of the coating of the photoresist to produce a surface feature, performing a copper plating process wherein the surface feature is filled with copper, removing the photoresist to produce a copper surface, performing a copper seed layer etching on the copper surface to produce copper etched surface and performing an adhesion layer etching on the copper etched surface.

[0012] In another example embodiment, a method for producing an electrical component is disclosed, comprising: providing a polyimide substrate with an adhesion layer containing molybdenum and a copper seed layer, covering at least a portion of the copper seed layer with a coating of photoresist, exposing the coating of photoresist, through a mask, to a radiation source, removing a section of the coating of the photoresist to produce a surface feature transferred from the mask, performing a copper plating process wherein the surface feature is filled with copper, removing the photoresist to produce a copper surface, performing a copper etching on the copper surface to produce copper etched surface and performing an adhesion layer etching on the copper etched surface.

[0013] In another example embodiment, an arrangement is disclosed, comprising: polyimide substrate with a first surface, a molybdenum adhesion layer connected to the first surface, a copper seed layer connected to the molybdenum adhesion layer; and a copper layer connected to the copper seed layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only exemplary embodiments and are therefore not to be

considered limiting of its scope, and may admit to other equally effective embodiments.

[0015] FIG. 1 is a table of prior art high density redistribution line technologies and limitations of such technologies.

[0016] FIGS. 2A, 2B, 2C, 2D, 2E, and 2F are a prior art process for silicon interposer technology.

[0017] FIG. 3A, 3B, 3C, 3D, 3E, and 3F are a prior art process for embedded copper trace technology.

[0018] FIG. 4 provides for a method for creating a copper plating and seed layer etching using molybdenum in an adhesion layer.

[0019] FIG. 5A, 5B, 5C, 5D, 5E, and 5F describe advantages and drawbacks of titanium and molybdenum adhesion layers.

[0020] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. It is contemplated that elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

[0021] In the following, reference is made to embodiments of the disclosure. It should be understood, however, that the disclosure is not limited to specific described embodiments. Instead, any combination of the following features and elements, whether related to different embodiments or not, is contemplated to implement and practice the disclosure. Furthermore, although embodiments of the disclosure may achieve advantages over other possible solutions and/or over the prior art, whether or not a particular advantage is achieved by a given embodiment is not limiting of the disclosure. Thus, the following aspects, features, embodiments, and advantages are merely illustrative and are not considered elements or limitations of the appended claims except where explicitly recited in a claim. Likewise, reference to “the disclosure” shall not be construed as a generalization of an inventive subject matter

disclosed herein and shall not be considered to be an element or limitation of the appended claims except where explicitly recited in a claim.

[0022] Some embodiments will now be described with reference to the figures. Like elements in the various figures will be referenced with like numbers for consistency. In the following description, numerous details are set forth to provide an understanding of various embodiments and/or features. It will be understood, however, by those skilled in the art, that some embodiments may be practiced without many of these details and that numerous variations or modifications from the described embodiments are possible. As used herein, the terms "above" and "below", "up" and "down", "upper" and "lower", "upwardly" and "downwardly", and other like terms indicating relative positions above or below a given point or element are used in this description to more clearly describe certain embodiments.

[0023] FIGS. 2A through 2F illustrate a prior art method for using silicon interposer technology. In FIG. 2A, a silicon wafer is present with etched features from a top side. In FIG. 2B, a dielectric fabrication step is performed, placing a dielectric over the top layer of the etched features of the wafer. In FIG. 2C, a barrier/adhesion layer and a seed layer are placed over the dielectric layer. In FIG. 2D, a step of electroplating occurs, filling the features remaining from the etched features. A layer of overfill from the electroplating also occurs. In FIG. 2E, removal of the excess layer of overfill occurs. Lastly, in FIG. 2F, mechanical methods, such as grinding, or etching may be used to remove the bottom layer of wafer, producing a final product. The slow silicon etch rate with common Bosch process by Deep Reactive Ion Etching (DRIE) and complexity of additional steps involved in insulating vias from the surrounding silicon, on top of the high capital expenditure on required equipment, result in costly fabrication, as listed in FIG. 1.

[0024] Referring to FIGS. 3A through 3F a prior art method for using embedded copper trace technology is illustrated. In FIG. 3A, a silicon wafer is presented with a dielectric layer that has surface features created by a first photolithographic process. In FIG. 3B, a second photolithographic process is performed to provide for further surface featuring on the dielectric layer. In FIG. 3C, a barrier/seed layer is sputtered by physical vapor deposition (PVD). In FIG. 3D, a layer of copper is filled in the features through electrochemical plating (ECP). The layer of copper provide in FIG.

3D has an overburden, which is, along with the excessive barrier/seed layer, later removed by chemical-mechanical polishing (CMP) in FIG. 3E. The process may be repeated for successive redistribution layer (RDL) stack-up, as illustrated in FIG. 3F. As illustrated in FIG. 1, the repeated elimination of copper overburden by CMP has an adverse impact on the overall cost of this method. Nevertheless, the maximum routing/millimeter of this copper dual-damascene based RDL scheme is limited by resolution and depth of focus of the photolithography capability in accommodating uniformity of thick dielectric film, CMP planarization quality, and cleanliness condition during fabrication.

[0025] Referring to FIG. 4, a method for using copper plating and using a seed layer with accompanying molybdenum adhesion layer over a dielectric layer (substrate) is provided. The molybdenum may be in the form of a molybdenum disulfide. The dielectric layer may be in a form of a spin-on, deposited or dry film or substrate and may include such materials as polyimide, epoxy, epoxy with fillers, Kaptrex, Apical, Kapton, UPILEX or other similar materials. In operation 1, a dielectric layer 400 is provided as the substrate. To enable the remainder of the arrangement to adhere to the polyimide layer, an adhesion layer 402 is provided, wherein the adhesion has molybdenum. The adhesion layer 402 may be sputtered on to the top of the dielectric layer 400, as a non-limiting manner of providing the adhesion layer 402. A copper seed layer 404 is also provided over the adhesion layer 402. A surface layer of photoresist 408 is provided over the copper seed layer. The photoresist layer 408 may be patterned to a sufficient amount through a mask 410 to form a template for a desired pattern for electrical processing.

[0026] The photoresist layer 408 may be a positive photoresist layer, such that when the resist is exposed to light, the sections experiencing the light become soluble to photoresist developer (as described later in operation 3). Such patterning may be performed through photolithography, as a non-limiting embodiment. As will be understood, the photolithography may produce a simple configuration or may produce a significantly complex arrangement. In operation 2, copper plating occurs, thereby filling the patterned surface of the arrangement, thus producing an arrangement, extending from bottom to top of: dielectric layer 400, adhesion layer 402, copper seed layer 404, and a layer of photoresist 408 and copper structure 406 on the copper seed

layer 404. Operation 2 can be performed through electrolysis by placement of the entire arrangement in a bath with a direct electric current to dissolve copper from a copper metal rod, thereby transporting copper ions from the rod through the bath to a cathode (the exposed area of the arrangement.

[0027] In operation 3, the photoresist 408 is stripped from the top of the arrangement leaving the copper top and sides exposed along with the copper seed layer 404. In operation 4, a wet etching is performed over the exposed copper tops and sides as well as the copper seed layer 404 to remove a surface layer of copper to expose the portion of the adhesion layer 402 not covered by the copper structure 406. Lastly, in operation 5, a further wet etching is performed to remove the portion of the adhesion layer 402 not covered by the copper structure 406, resulting in a final product.

[0028] As described, the wet etching may use liquid-phase etchants. As an example embodiment, an arrangement may be immersed in a bath of an etchant. During the submersion, the liquid phase etchant may be stirred or agitated to perform an even etching over the required surface.

[0029] The method provided in FIG. 4, provides many advantages over conventional techniques as illustrated in FIGS. 5A-5F. Referring to FIGS. 5A-5F, with use of titanium in the adhesion layer, the removal of titanium gets more and more difficult towards the interface with the dielectric layer. To this end, over-etching is required in FIG. 5A to ensure complete titanium adhesion layer removal as compared FIG. 5D, where an adhesion layer containing molybdenum can be easily removed without over-etching. Such over etching causes production results that are not in conformance with designed features. Referring to FIG. 5B, residual titanium on the dielectric surface leads to surface leakage current compared to FIG. 5E, where there is no metallic residue after barrier/seed etching when an adhesion layer containing molybdenum is used. Referring to FIG. 5C, the electrical resistivity value for titanium is 420 nΩ•m as compared to the electrical resistivity value for molybdenum of 53.4 nΩ•m in FIG. 5F. The intrinsically lower resistivity of molybdenum by one order of magnitude than that of titanium improves device electrical performance.

[0030] The method allows for resolutions to be achieved that were previously unattainable without the serious drawbacks of such conventional methods. The use of the molybdenum does not need over etching and hence minimizes undercut. Use of a conventional titanium layer requires a large over-etch for complete removal that causes an undercut underneath the copper structure, causing electrical and reliability issues of the package. Additionally, residual titanium to dielectric contact leads to surface leakage current minimizing the efficiency of the design. With molybdenum, no such surface leakage occurs. The use of a molybdenum layer also provides for a low resistance compared to titanium, thereby providing for a better electrical contact. The use of molybdenum also provides for superior warpage modulation, compared to titanium arrangements.

[0031] Aspects of the disclosure also allow for minimizing adhesion layer undercut. Such minimization of undercut allows sub-micron line/spacing and thicker barrier seed deposition to compensate for underlayer roughness. Such configurations enable semi-additive process on large substrates/panels.

[0032] In one non-limiting example embodiment of the disclosure, a method for producing an electrical component is disclosed comprising: providing a polyimide substrate; coating at least one side of the polyimide substrate with an adhesion layer comprising molybdenum; coating the adhesion layer with a copper seed layer; covering at least a portion of the copper seed layer with a coating of photoresist; removing a section of the coating of the photoresist to produce a surface feature; performing a copper plating process wherein the surface feature is filled with copper; removing the photoresist to produce a copper surface; performing a copper etching on the copper surface to produce copper etched surface and performing an adhesion layer etching on the copper etched surface.

[0033] In another example embodiment, the method may be performed wherein the copper etching is a wet copper etching.

[0034] In another example embodiment, the method may be performed wherein the removing the section of the coating of the photoresist is performed through a photoresist developer.

[0035] In another example embodiment, the method may be performed wherein the polyamide substrate is one of Kaptrex, Apical, Kapton and UPILEX.

[0036] In another example embodiment, the method may be performed, wherein the coating on at least one side of the polyimide substrate with an adhesion layer comprising molybdenum is performed by a sputtering process.

[0037] In another example embodiment, the method may be performed wherein the sputtering process is produced by a magnetron.

[0038] In another example embodiment, the method may be performed wherein the molybdenum is molybdenum disulfide.

[0039] In another example embodiment, a method for producing an electrical component is disclosed. In this method, the production includes providing a polyimide substrate with an adhesion layer containing molybdenum and a copper seed layer, covering at least a portion of the copper seed layer with a coating of photoresist, exposing the coating of photoresist, through a mask, to a radiation source, removing a section of the coating of the photoresist to produce a surface feature transferred from the mask, performing a copper plating process wherein the surface feature is filled with copper, removing the photoresist to produce a copper surface, performing a copper etching on the copper surface to produce copper etched surface and performing an adhesion layer etching on the copper etched surface.

[0040] In another example embodiment, the method may be performed wherein the copper etching is a wet copper etching.

[0041] In another example embodiment, the method may be performed wherein the removing the section of the coating of the photoresist is performed through a photoresist developer.

[0042] In another example embodiment, the method may be performed wherein the polyimide substrate is one of Kaptrex, Apical, Kapton and UPILEX.

[0043] In another example embodiment, the method may be performed wherein the coating on at least one side of the polyimide substrate with an adhesion layer comprising molybdenum is performed by a sputtering process.

[0044] In another example embodiment, the method may be performed wherein sputtering process is produced by a magnetron.

[0045] In another example embodiment, the method may be performed wherein the molybdenum is molybdenum disulfide.

[0046] In another example embodiment, the method may be performed, wherein the copper plating process is performed wherein the surface feature is filled with copper through electrolysis.

[0047] In another example embodiment, an arrangement is disclosed comprising: polyimide substrate with a first surface, a molybdenum adhesion layer connected to the first surface, a copper seed layer connected to the molybdenum adhesion layer; and a copper layer connected to the copper seed layer.

[0048] In another example embodiment, the arrangement may be configured wherein the seed layer is a copper seed layer.

[0049] In another example embodiment, the arrangement may be configured, wherein the copper layer has features that are at a line space packaging ratio of less than 10/10 μm.

[0050] In another example embodiment, the arrangement may be configured, wherein the copper layer has features that are at a line space packaging ratio of less than 5/5 μm.

[0051] In another example embodiment, the arrangement may be configured, wherein the copper layer has features that are at a line space packaging ratio of less than 2/2 μm.

[0052] While embodiments have been described herein, those skilled in the art, having benefit of this disclosure will appreciate that other embodiments are envisioned that do not depart from the inventive scope of the present application. Accordingly, the scope of the present claims or any subsequent related claims shall not be unduly limited by the description of the embodiments described herein.

CLAIMS

1. A method for producing an electrical component, comprising:

positioning an epoxy substrate;

coating at least one side of the epoxy substrate with an adhesion layer comprising molybdenum, the adhesion layer comprising molybdenum being in direct contact with the epoxy substrate;

coating the adhesion layer with a copper seed layer, the copper seed layer being in direct contact with the adhesion layer comprising molybdenum;

covering at least a portion of the copper seed layer with a coating of photoresist;

removing a section of the coating of the photoresist to produce a surface feature;

performing a copper plating process wherein the surface feature is filled with copper;

removing the photoresist to produce a copper surface that comprises the at least a portion of the copper seed layer that was coated with the photoresist and the copper formed during the copper plating process;

after removing the photoresist, etching the copper surface to remove the at least a portion of the copper seed layer that was coated with the photoresist and leave at least a portion of the copper formed during the copper plating process; and

etching the adhesion layer exposed after etching the copper surface, wherein the adhesion layer is etched to have a width substantially equal to a width of the surface feature adjacent thereto.

2. The method according to claim 1, wherein etching the copper surface comprises a wet copper etching.

3. The method according to claim 1, wherein the removing of the section of the coating of the photoresist is performed through a photoresist developer.

4. The method according to claim 1, wherein the epoxy substrate is an epoxy film.

5. The method according to claim 1, wherein the coating on the at least one side of the epoxy substrate with an adhesion layer comprising molybdenum is performed by a sputtering process.

6. The method according to claim 5, wherein the sputtering process is produced by a magnetron.

7. The method according to claim 1, wherein the molybdenum is molybdenum disulfide.

8. A method for producing an electrical component, comprising:

positioning an epoxy substrate with an adhesion layer containing molybdenum disposed directly on the epoxy substrate and a copper seed layer disposed directly on the adhesion layer;

covering at least a portion of the copper seed layer with a coating of photoresist;

exposing the coating of photoresist, through a mask, to a radiation source;

removing a section of the coating of the photoresist to produce a surface feature transferred from the mask;

performing a copper plating process wherein the surface feature is filled with copper;

removing the photoresist to produce a copper surface that comprises the at least a portion of the copper seed layer that was coated with the photoresist and the copper formed during the copper plating process;

after removing the photoresist, etching the copper surface to remove the at least a portion of the copper seed layer that was coated with the photoresist and leave at least a portion of the copper formed during the copper plating process; and

etching the adhesion layer exposed after etching the copper surface, wherein the adhesion layer is etched to have a width substantially equal to a width of the surface feature adjacent thereto.

9. The method according to claim 8, wherein etching the copper surface comprises a wet copper etching.

10. The method according to claim 8, wherein the removing of the section of the coating of the photoresist is performed through a photoresist developer.

11. The method according to claim 8, wherein the epoxy substrate is an epoxy film.

12. The method according to claim 8, wherein the coating on at least one side of the epoxy substrate with an adhesion layer comprising molybdenum is performed by a sputtering process.

13. The method according to claim 12, wherein the sputtering process is produced by a magnetron.

14. The method according to claim 8, wherein the molybdenum is molybdenum disulfide.

15. A method for producing an electrical component, comprising:

coating a first surface of an epoxy substrate with an adhesion layer comprising molybdenum, the adhesion layer comprising molybdenum being in direct contact with the first surface of the epoxy substrate;

coating the adhesion layer with a copper seed layer, the copper seed layer being in direct contact with the adhesion layer comprising molybdenum;

covering at least a portion of the copper seed layer with a coating of photoresist;

removing a section of the coating of the photoresist to produce a surface feature;

performing a copper plating process wherein the surface feature is filled with copper;

removing the photoresist to produce a copper surface that comprises the at least a portion of the copper seed layer that was coated with the photoresist and the copper formed during the copper plating process;

after removing the photoresist, etching the copper surface to remove the at least a portion of the copper seed layer that was coated with the photoresist and leave at least a portion of the copper formed during the copper plating process; and

etching an exposed surface of the adhesion layer after etching the copper surface to expose the first surface of the epoxy substrate, wherein the adhesion layer is etched to have a width substantially equal to a width of the surface feature adjacent thereto.

16. The method of claim 15, wherein the molybdenum is molybdenum disulfide.

17. The method of claim 15, wherein etching the copper surface comprises wet copper etching.

18. The method of claim 15, wherein the coating of the first surface of the epoxy substrate with an adhesion layer comprising molybdenum is performed by a sputtering process produced by a magnetron.