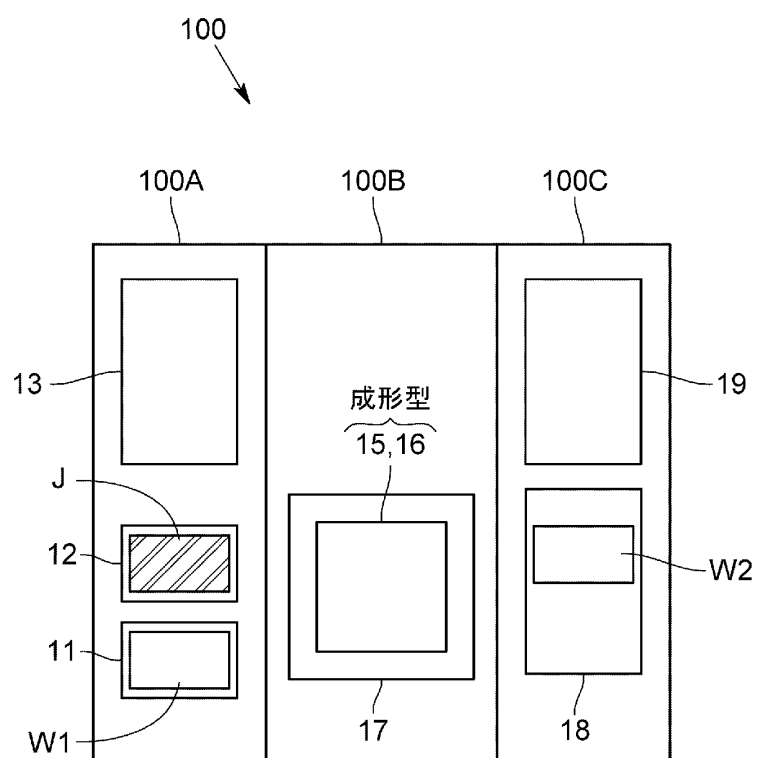
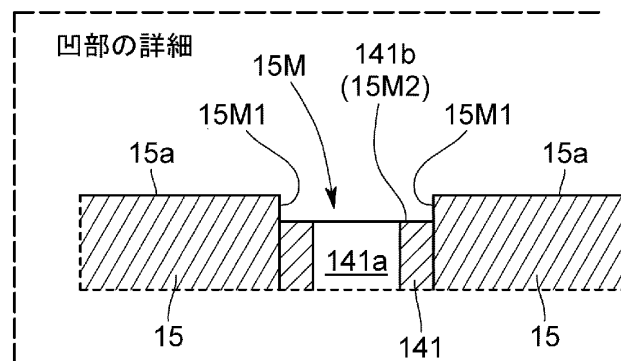
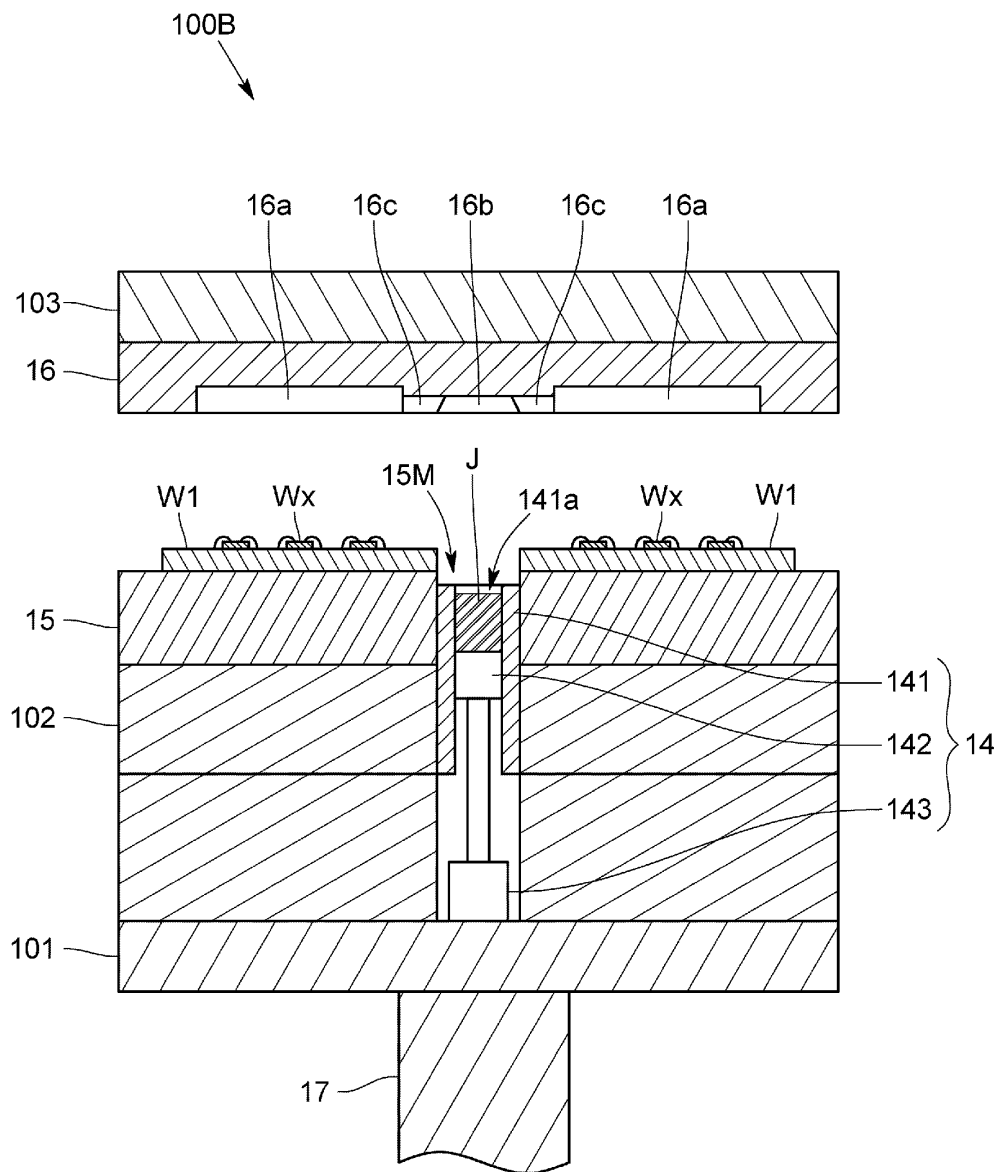


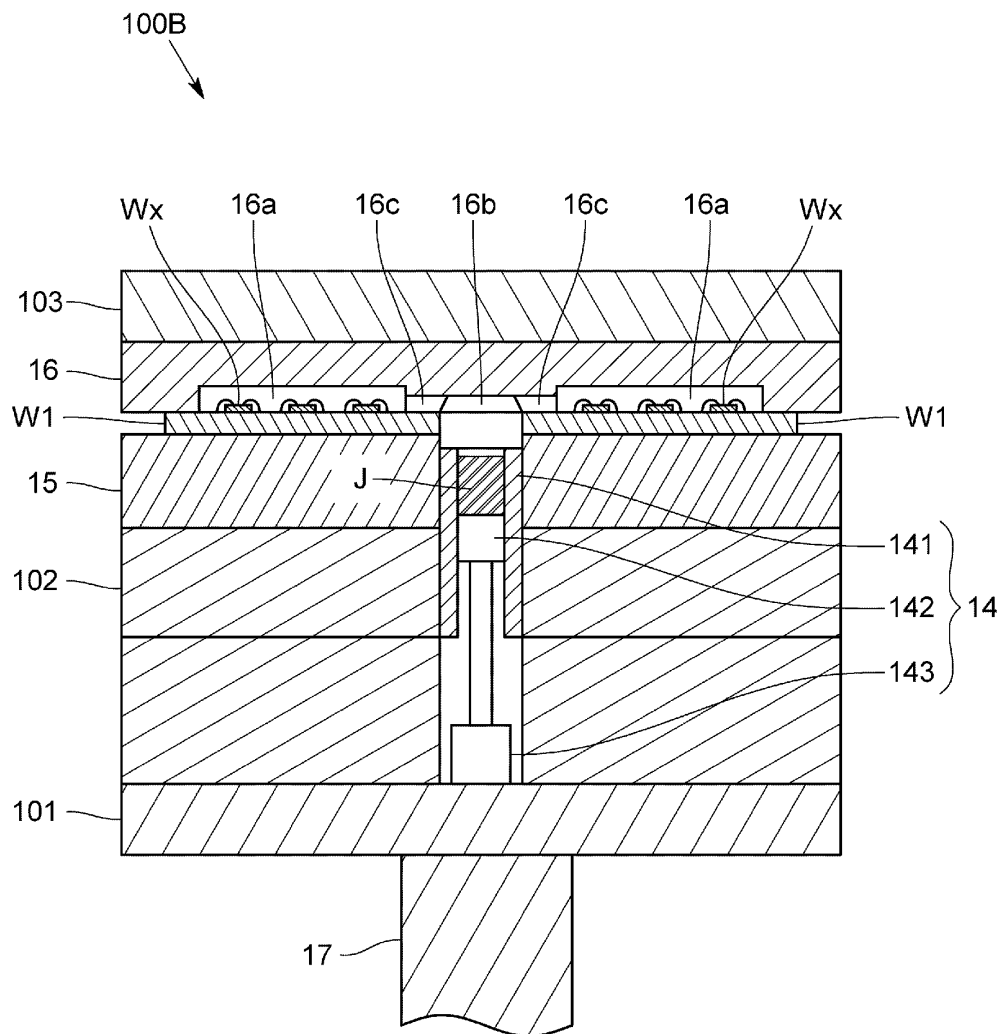
[図1]



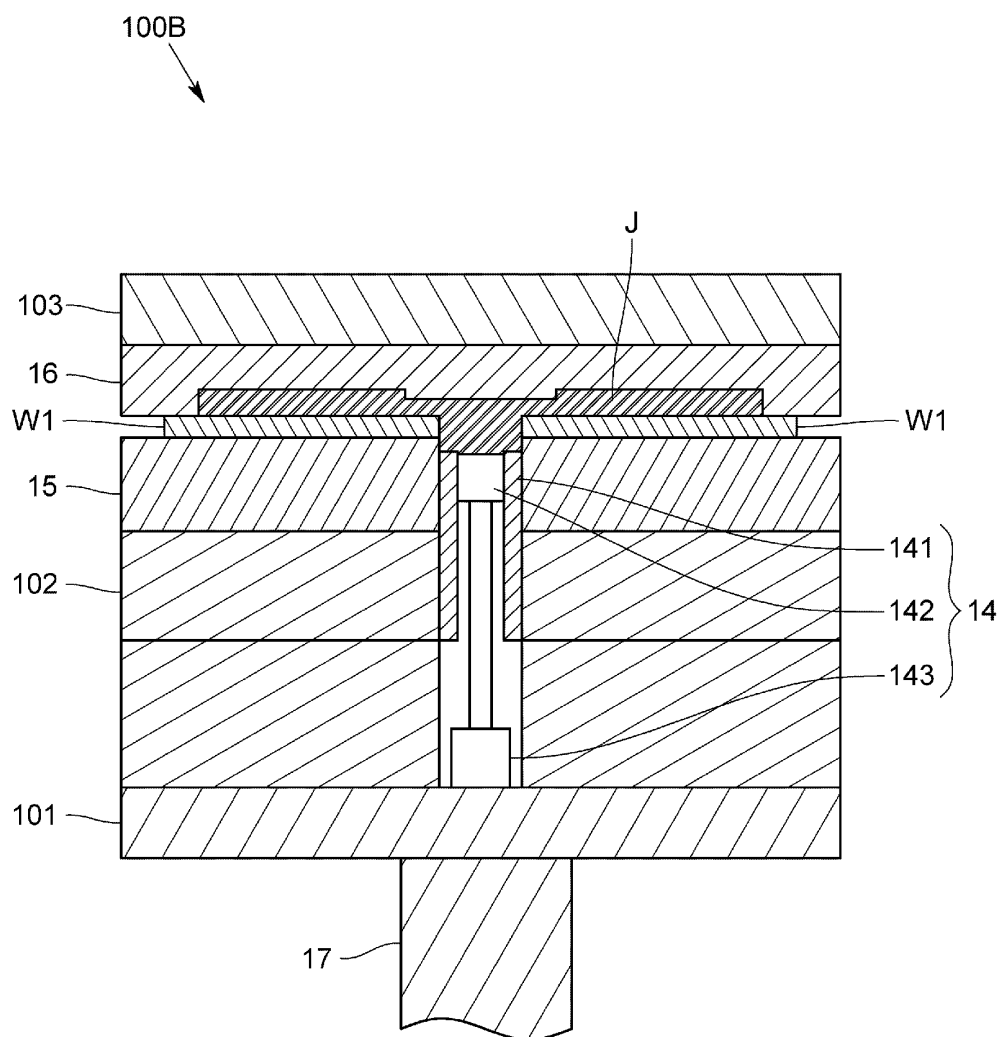
[図2]



[図3]



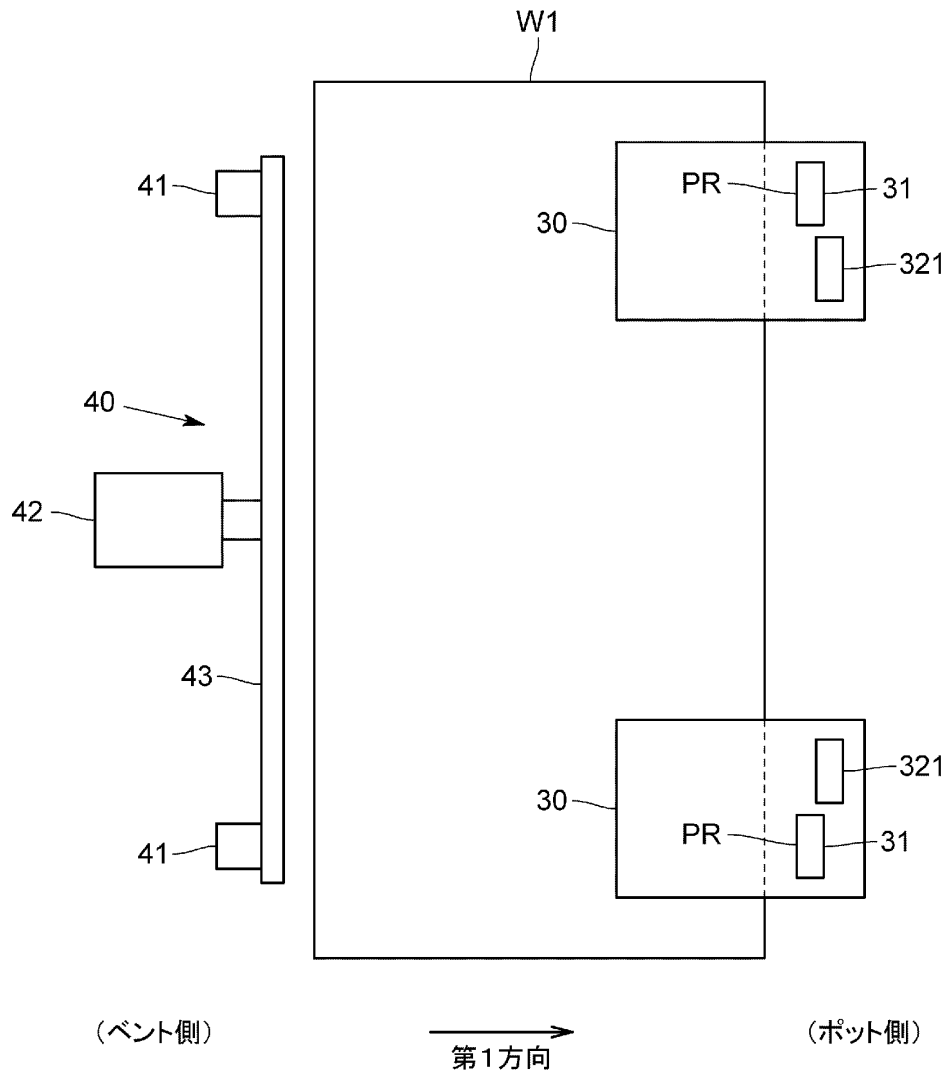
[図4]



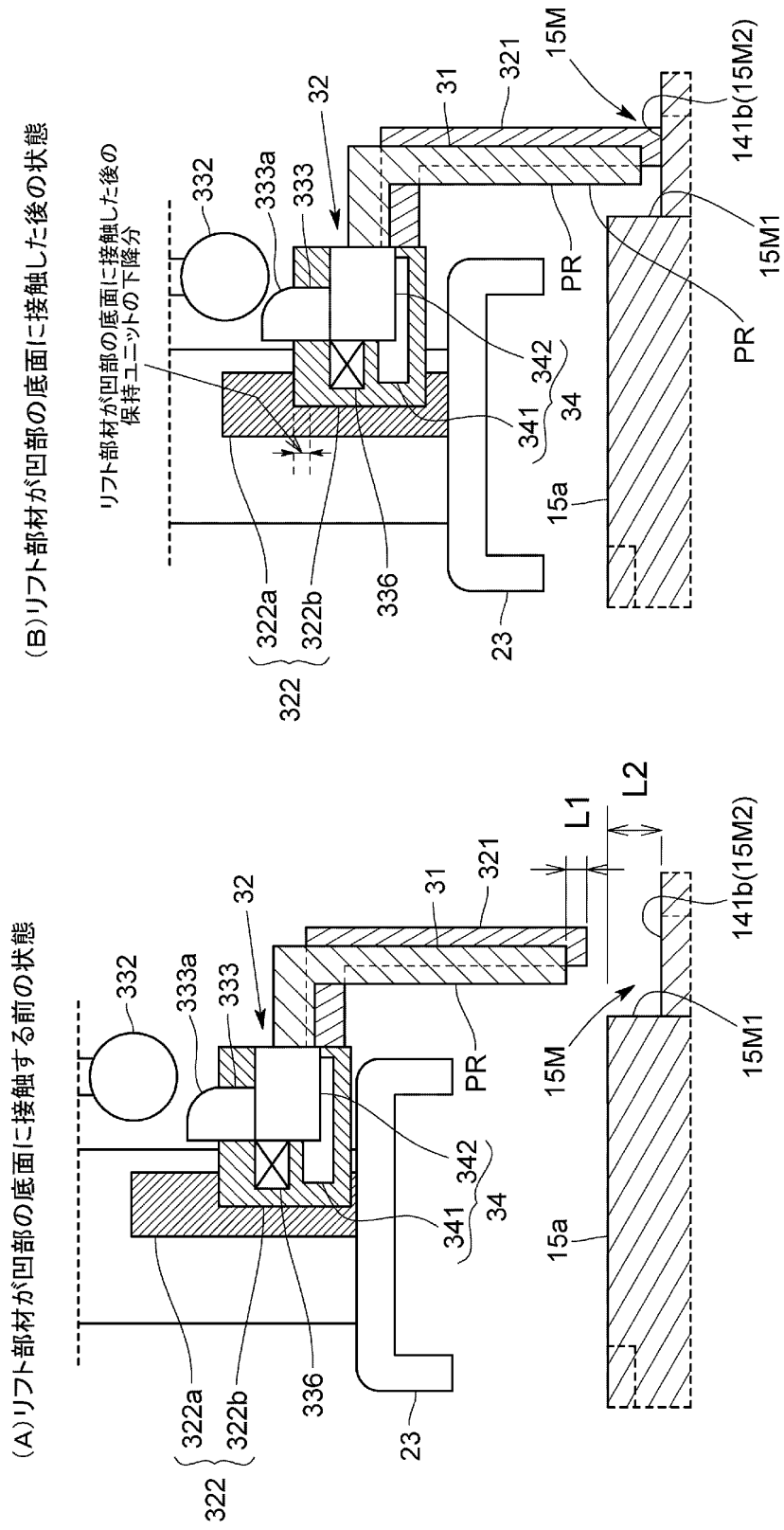
The figure contains two cross-sectional views of a semiconductor device. The top view, labeled 100B, shows a substrate 103 with a layer 16 on top. Layer 16 contains two rectangular regions 16a and a central gap 16b. The bottom view shows a multi-layered structure. From bottom to top, the layers are: 101, 102, 15, and a top layer W2. A central vertical structure 17 passes through layers 101, 102, and 15. On the right side, a bracket groups three layers labeled 141, 142, and 143.



[図7]

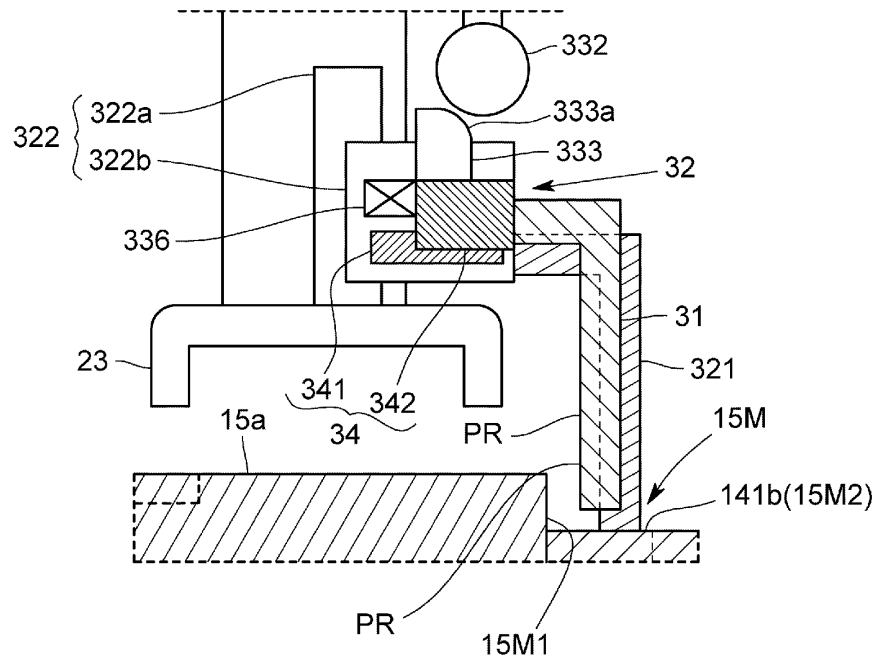


[図8]

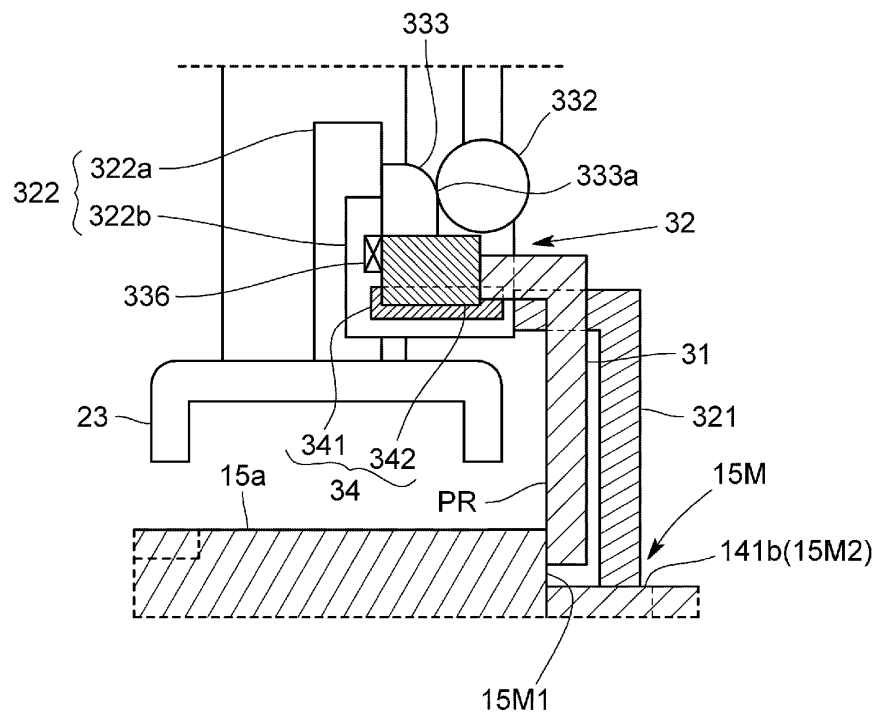


[図9]

(A) 基準面部材が凹部の側面に接触する前の状態

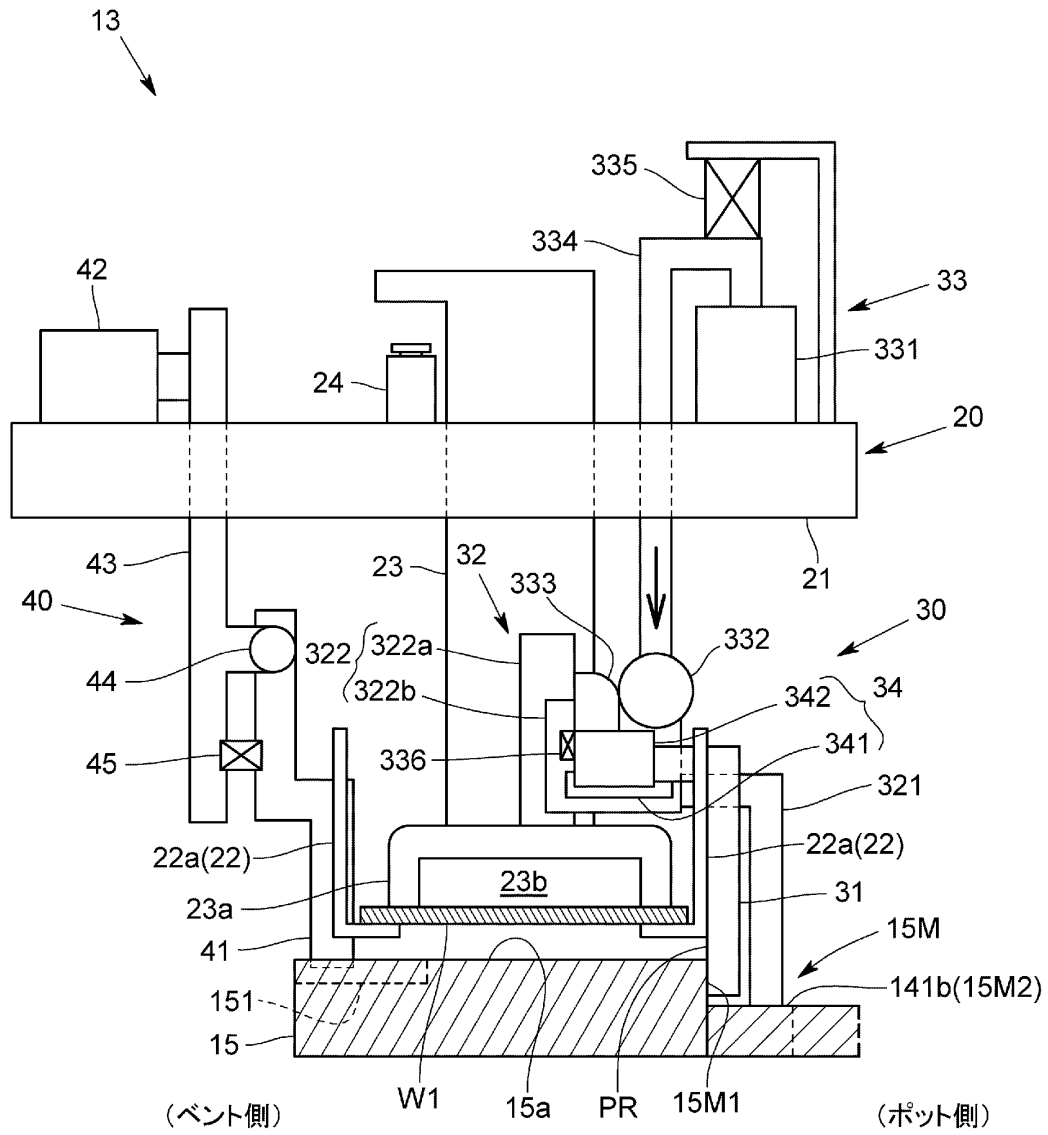


(B) 基準面部材が凹部の側面に接触した後の状態



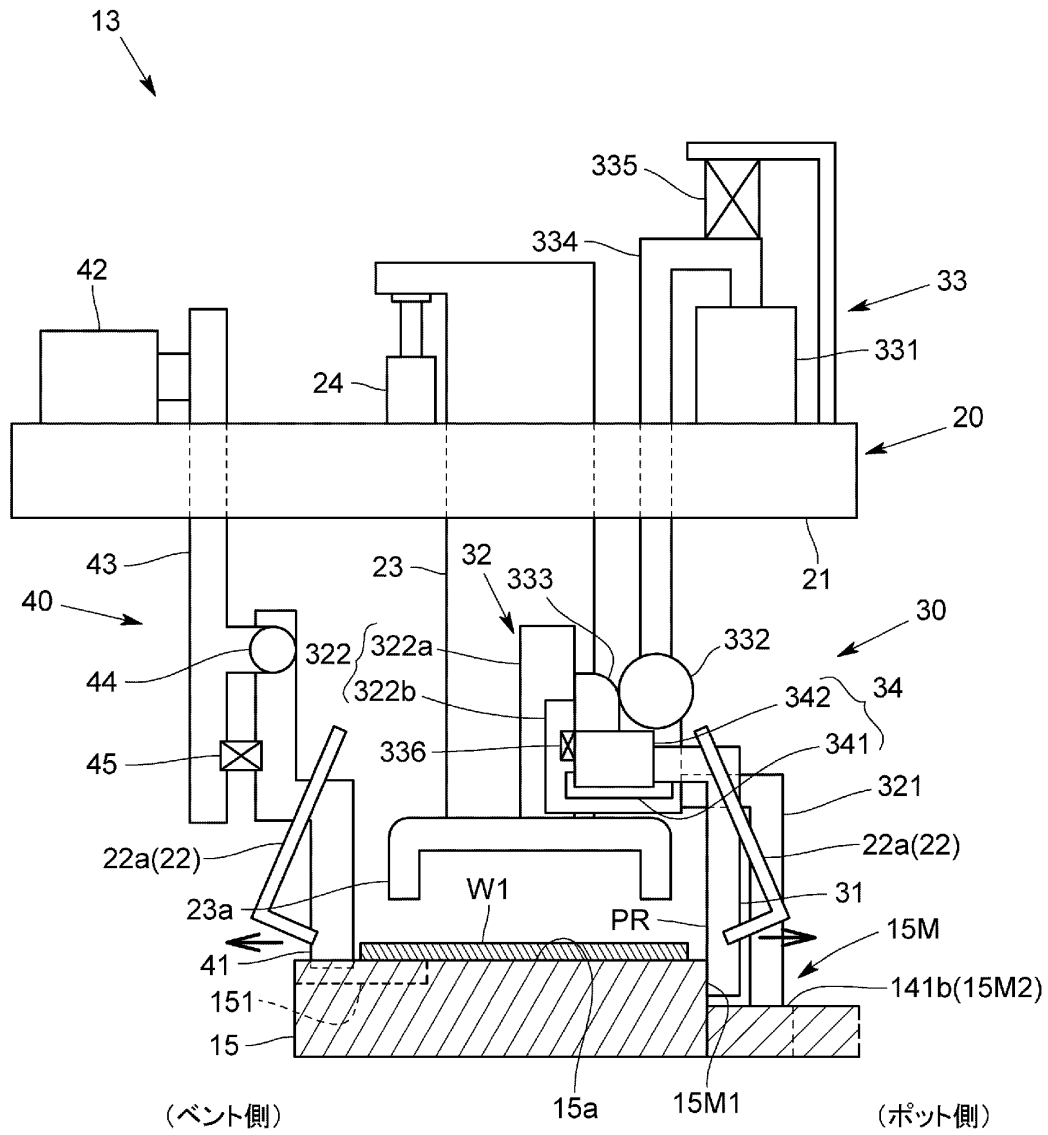


[図11]



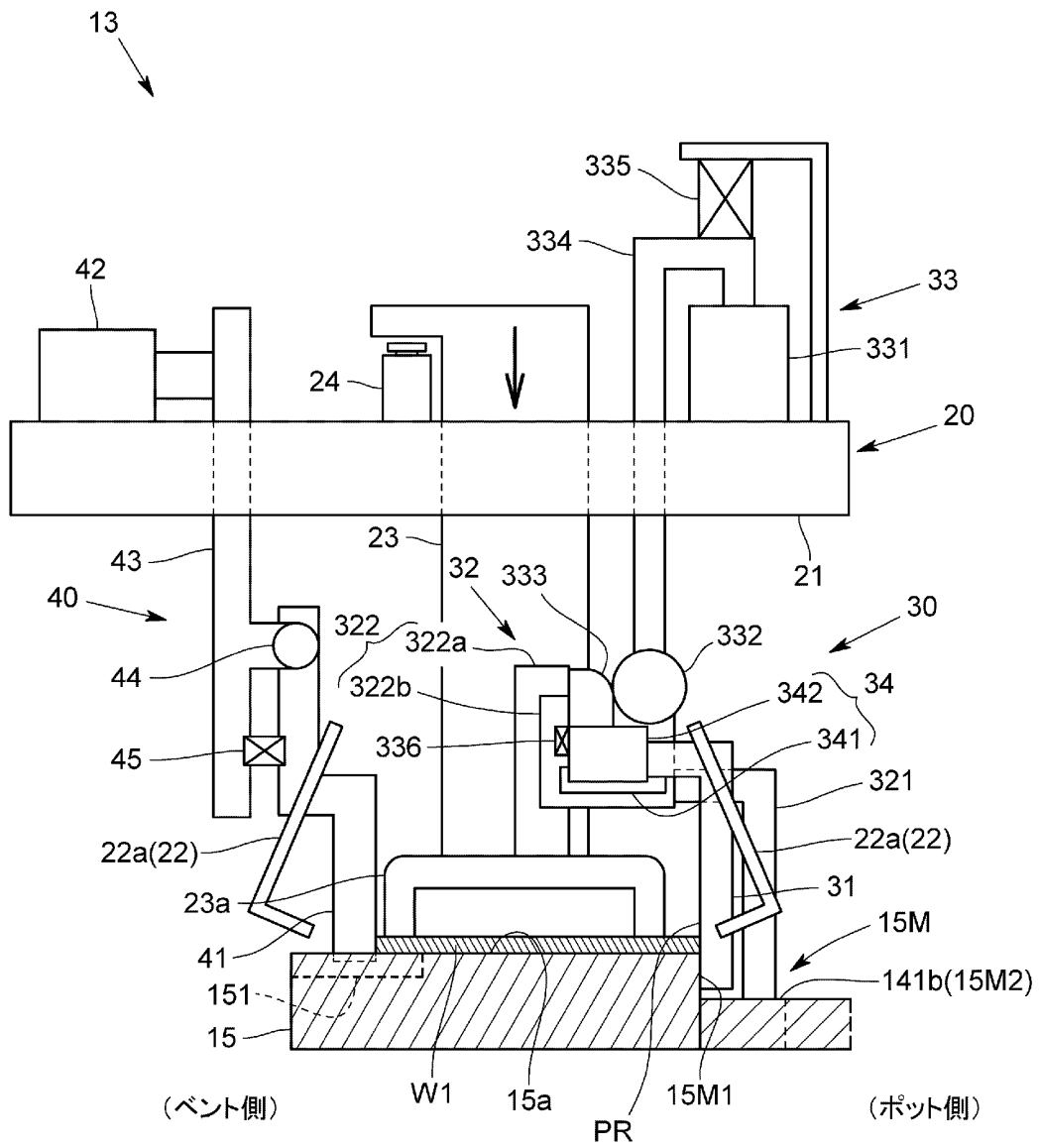


[図13]



[illegible]

[図15]



[図16]

