

1/21

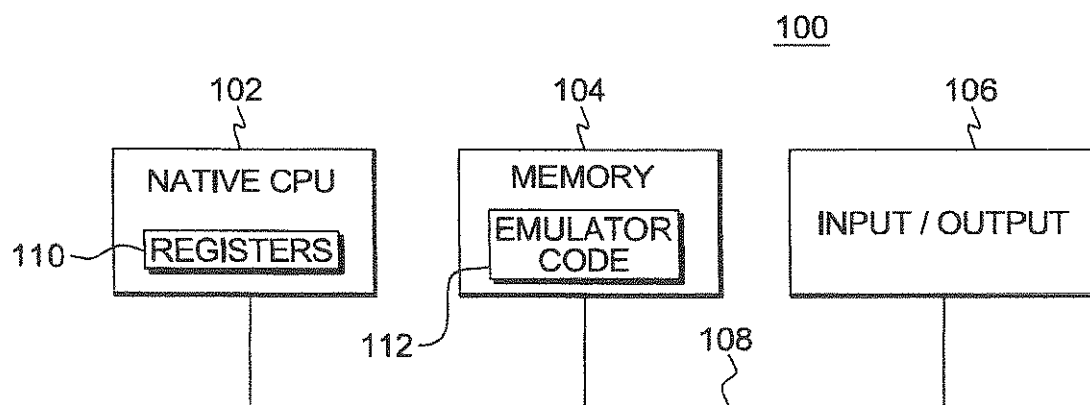


FIG. 1

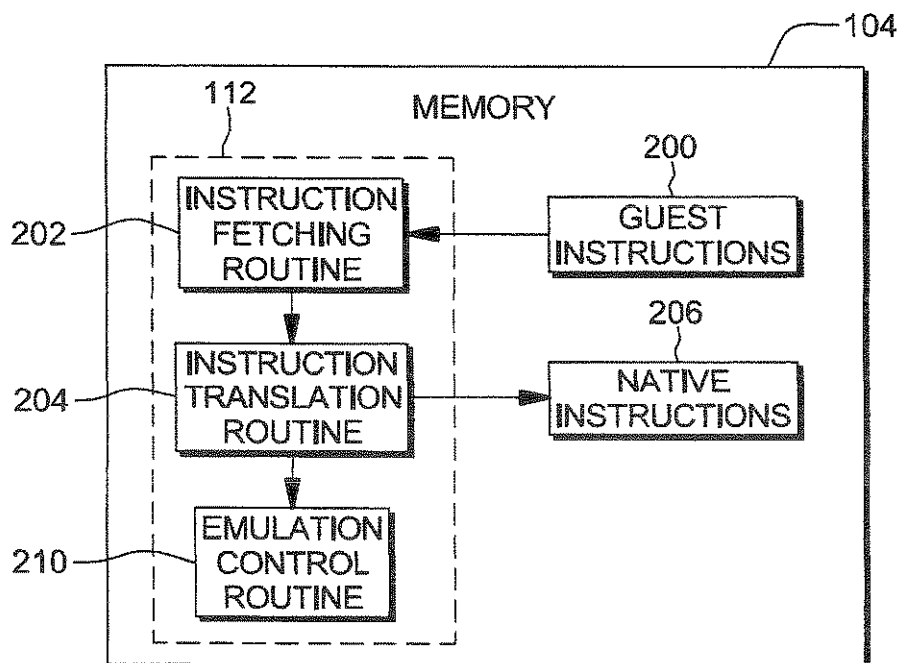


FIG. 2

2/21

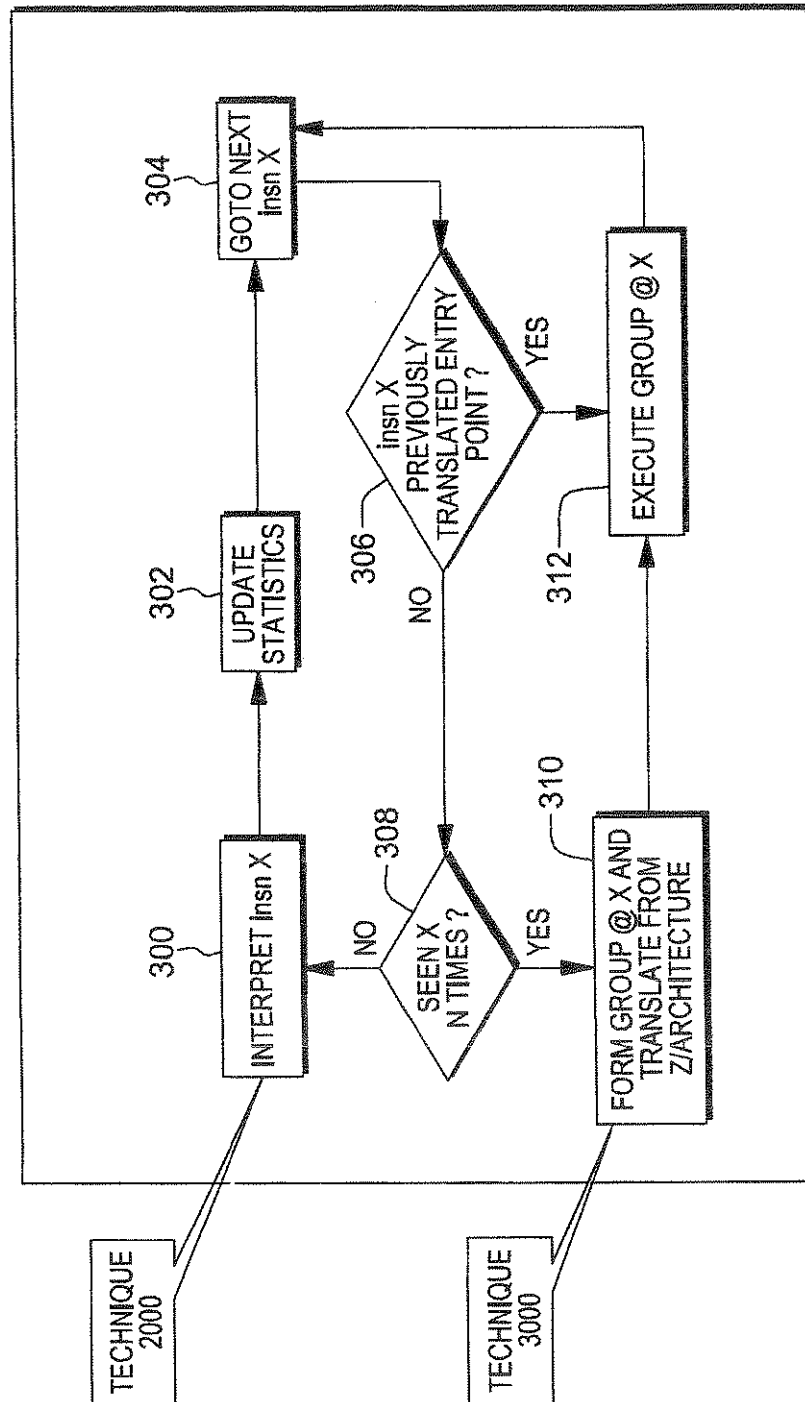


FIG. 3

3/21

TECHNIQUE 2000

EMULATION (INTERPRETATION)

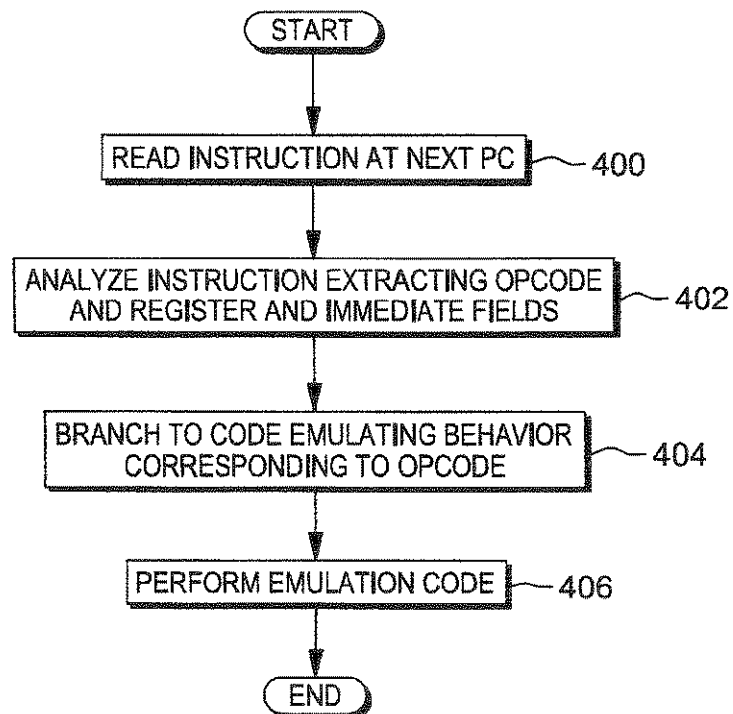


FIG. 4

4/21

TECHNIQUE 3000

EMULATION (TRANSLATION)

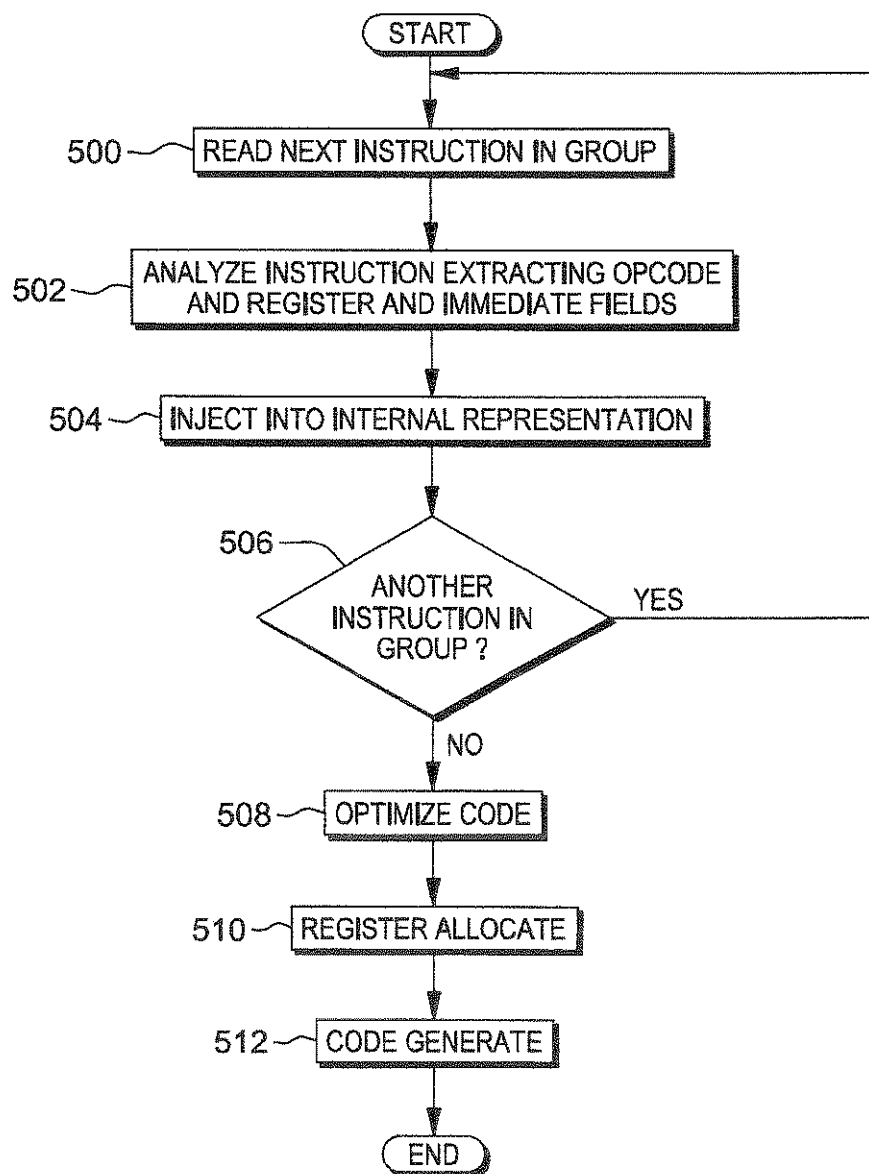


FIG. 5

5/21

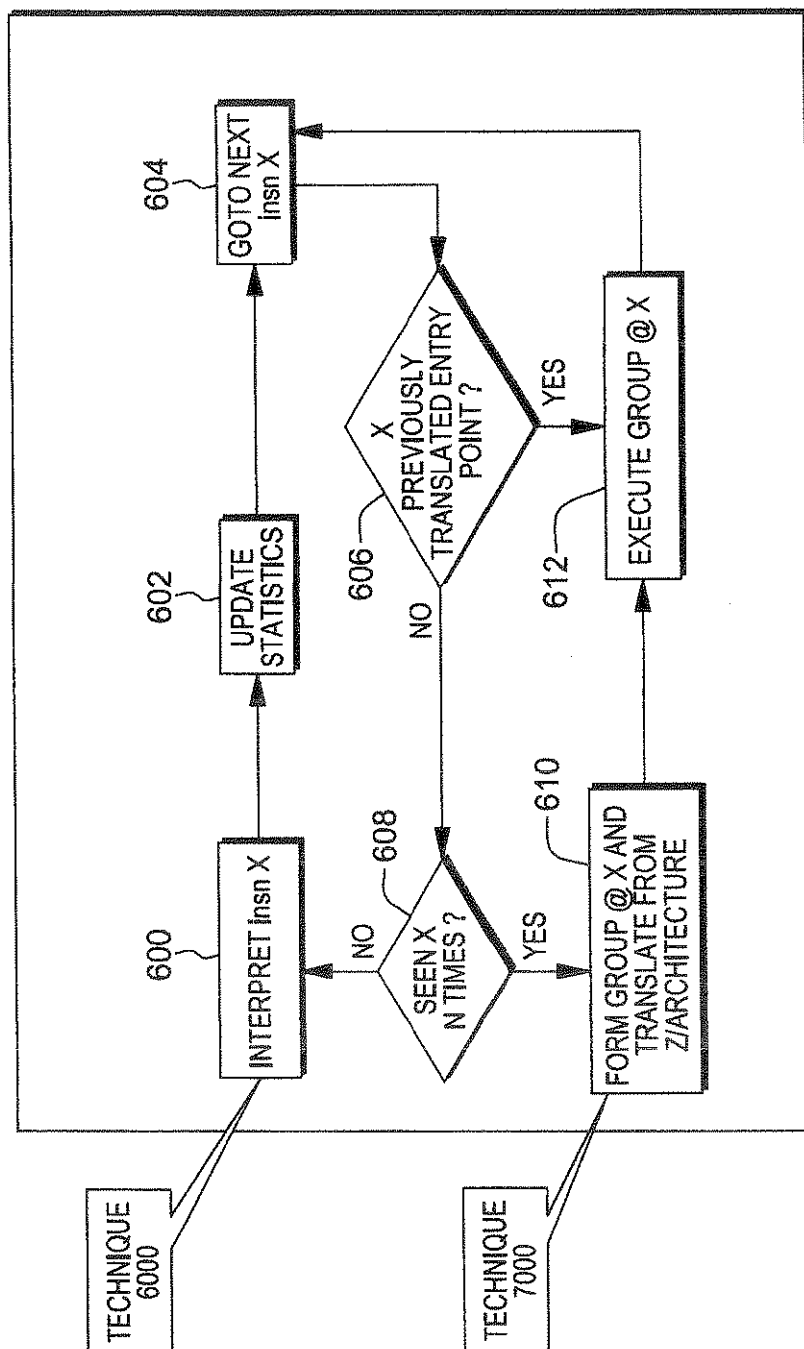


FIG. 6

6/21

TECHNIQUE 6000

EMULATION (INTERPRETATION)

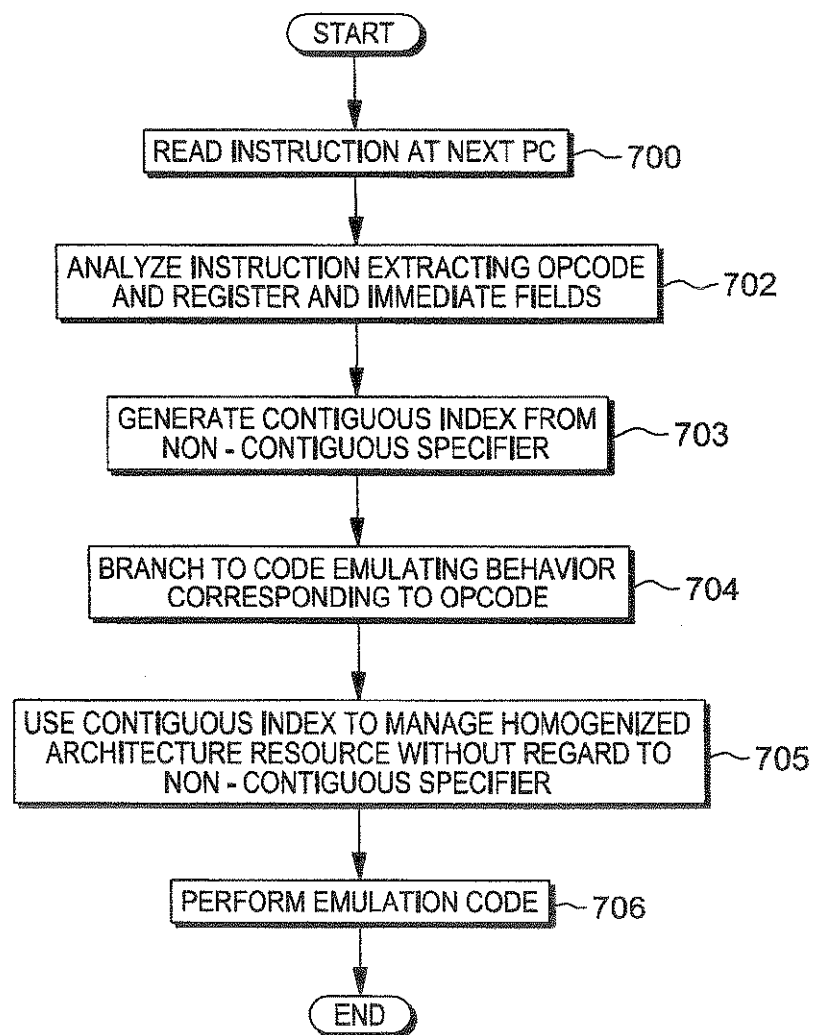


FIG. 7A

7/21

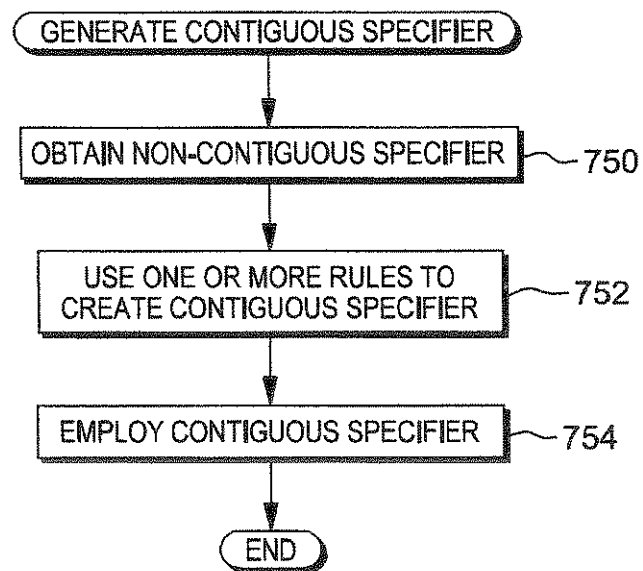


FIG. 7B

8/21

TECHNIQUE 7000

EMULATION (TRANSLATION)

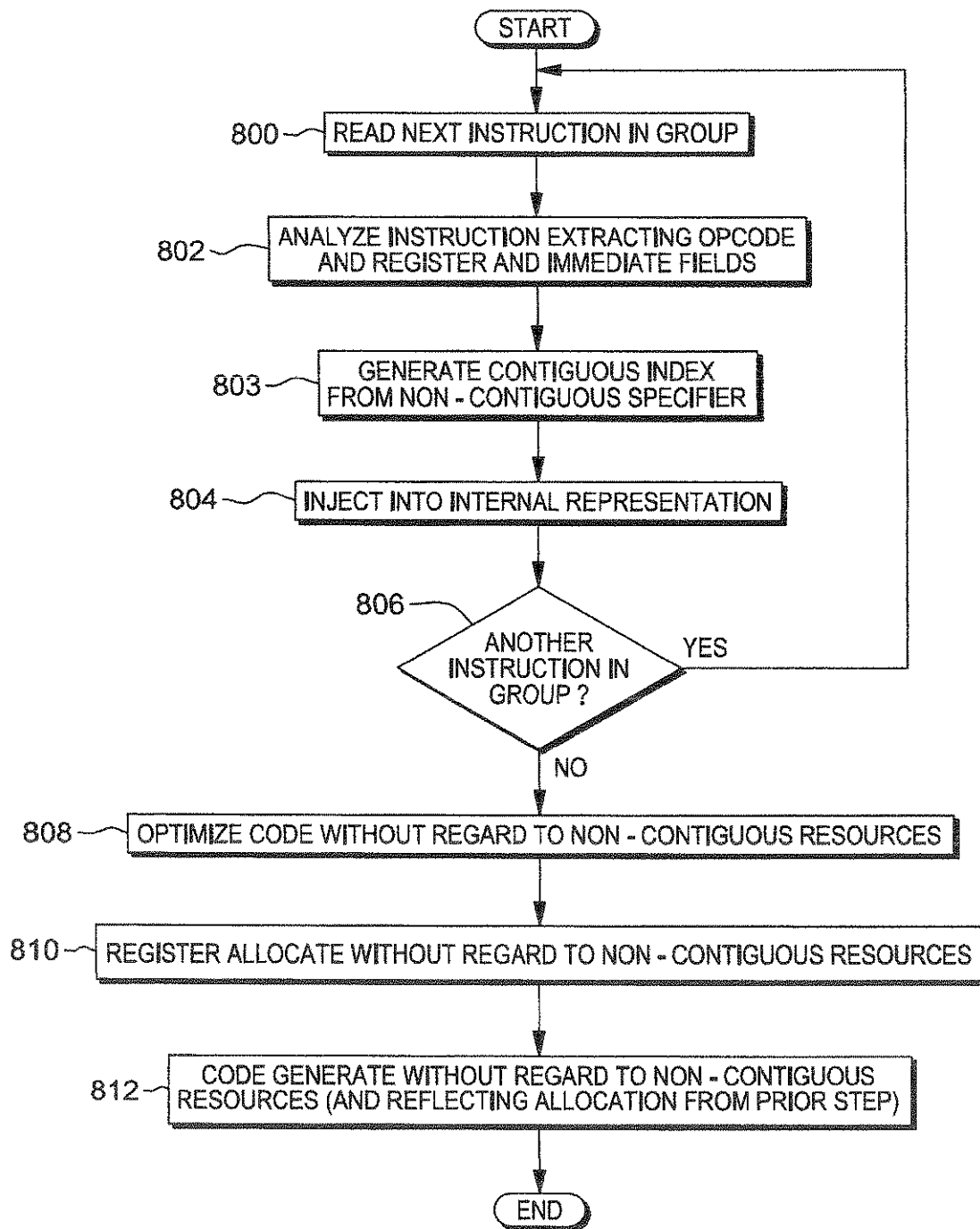


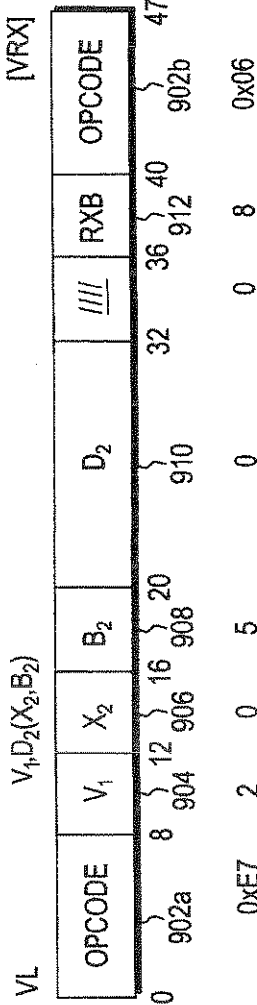
FIG. 8

9/21

(ALLOCATE TO A REGISTER DURING EMULATION)

900

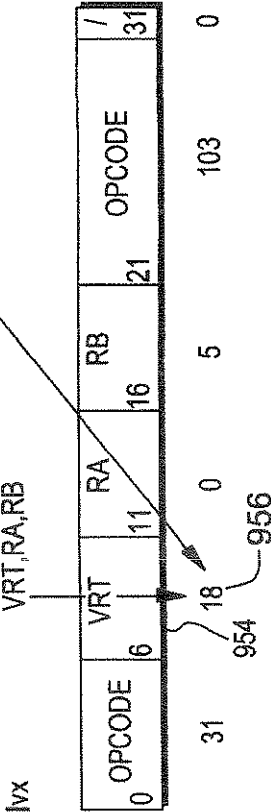
VECTOR LOAD



VL v18, 0(0, gr5)

LOAD VECTOR INDEXED ~ 950

X - FORM



LVX v18, r0, r5

FIG. 9A

10/21

(ALLOCATE TO A REGISTER DURING EMULATION)

900

VECTOR LOAD

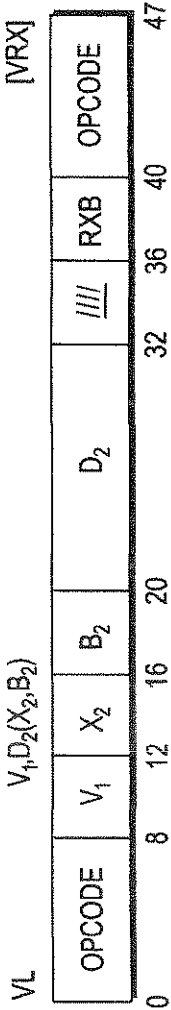
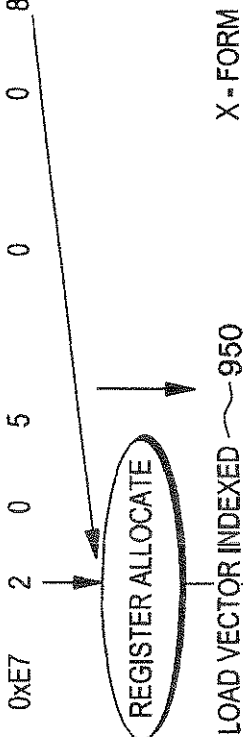
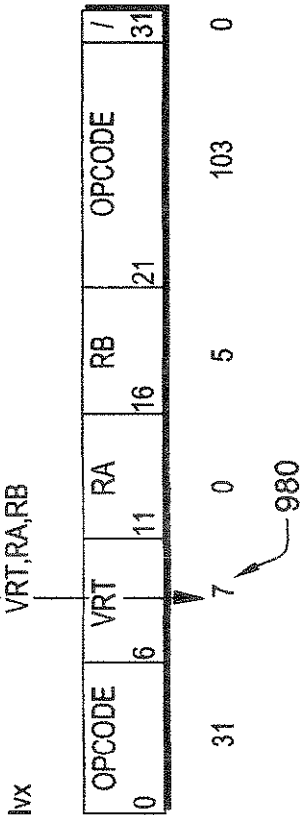
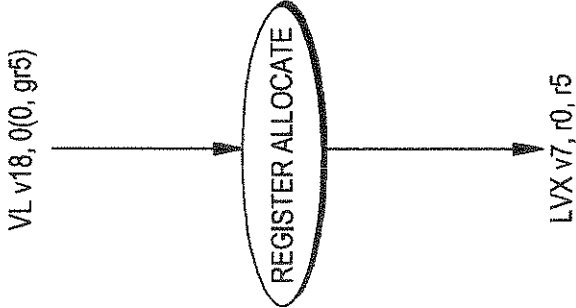


FIG. 9B

1000

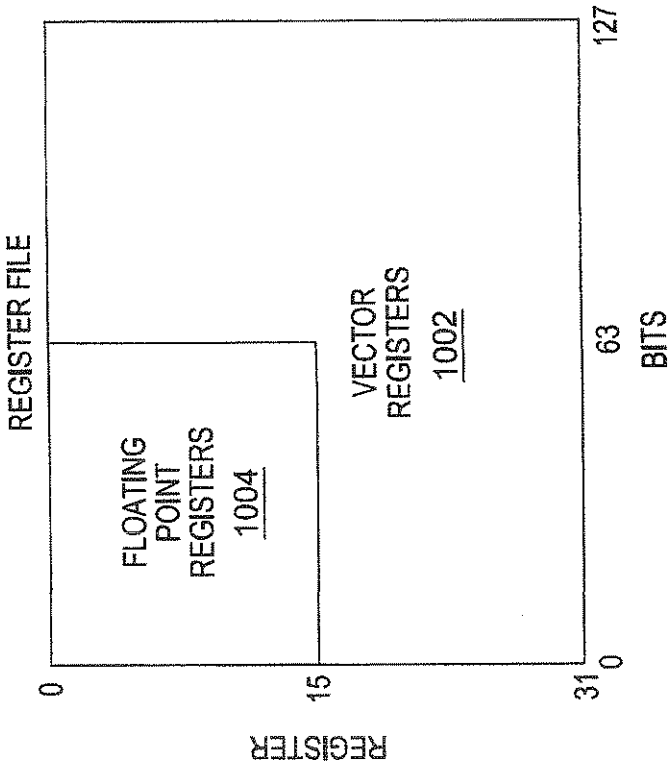


FIG. 10

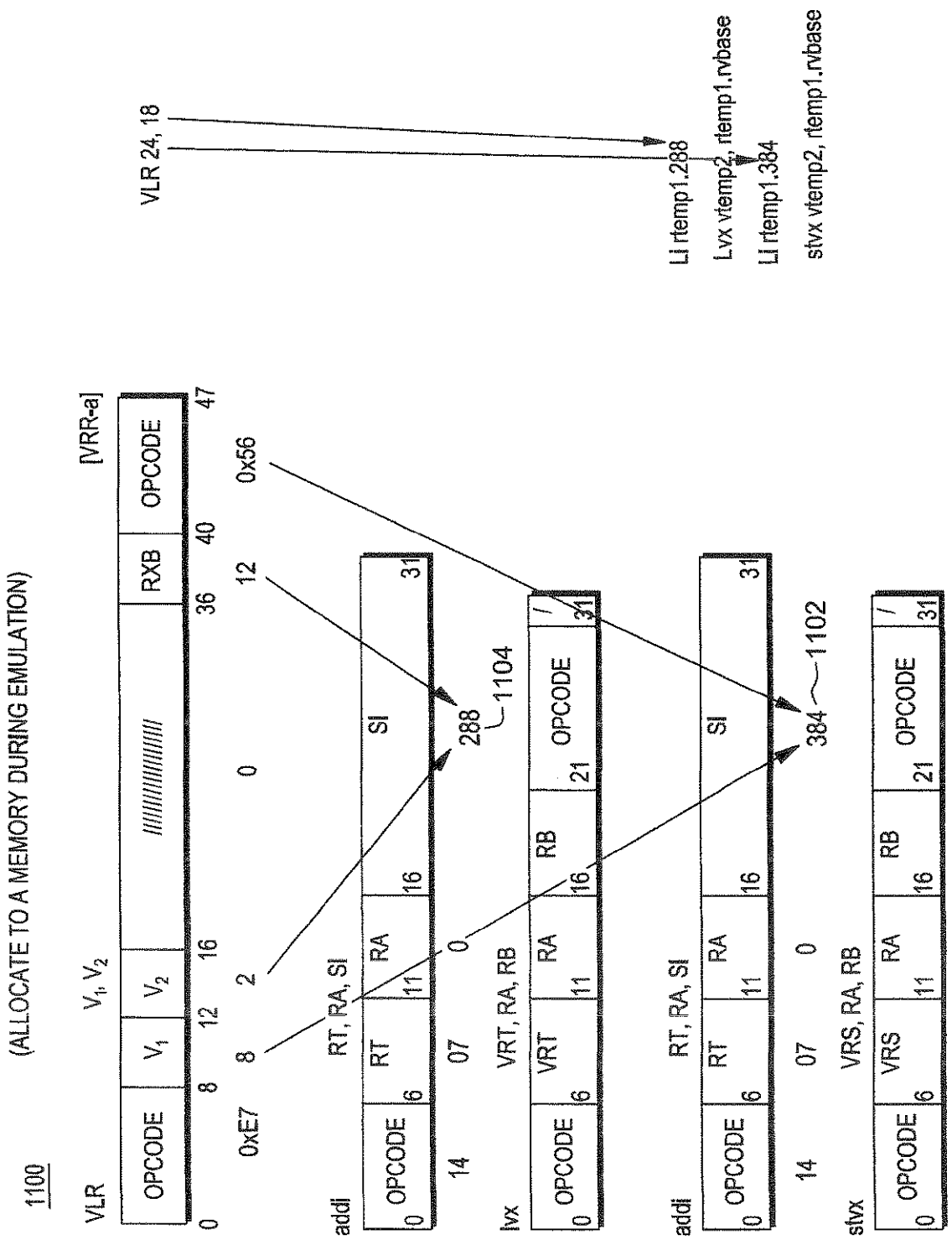


FIG. 11

13/21

COMPUTER
PROGRAM
PRODUCT
1200

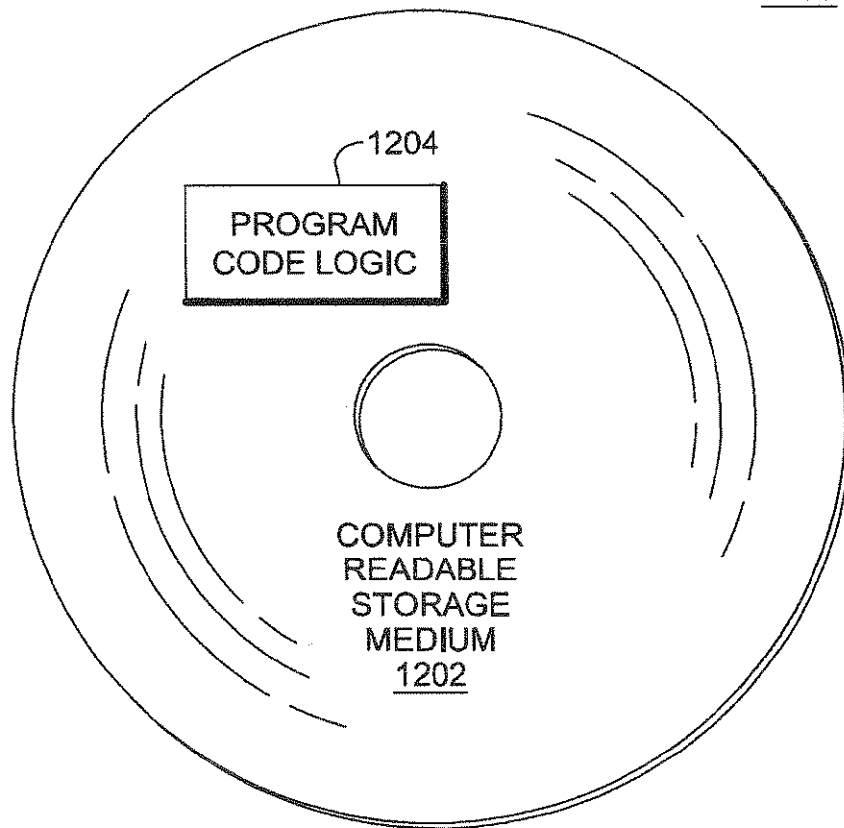


FIG. 12

14/21

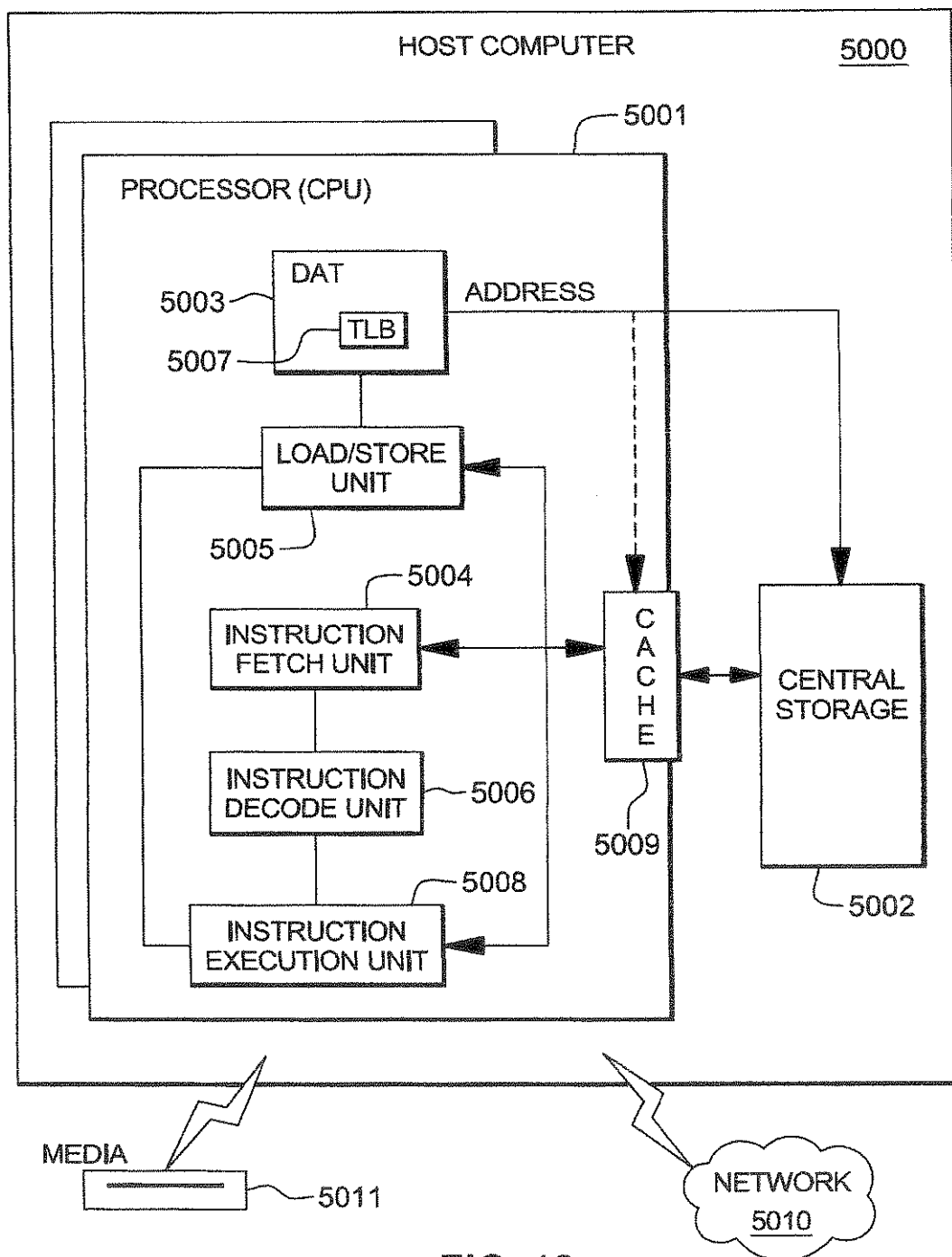


FIG. 13

15/21

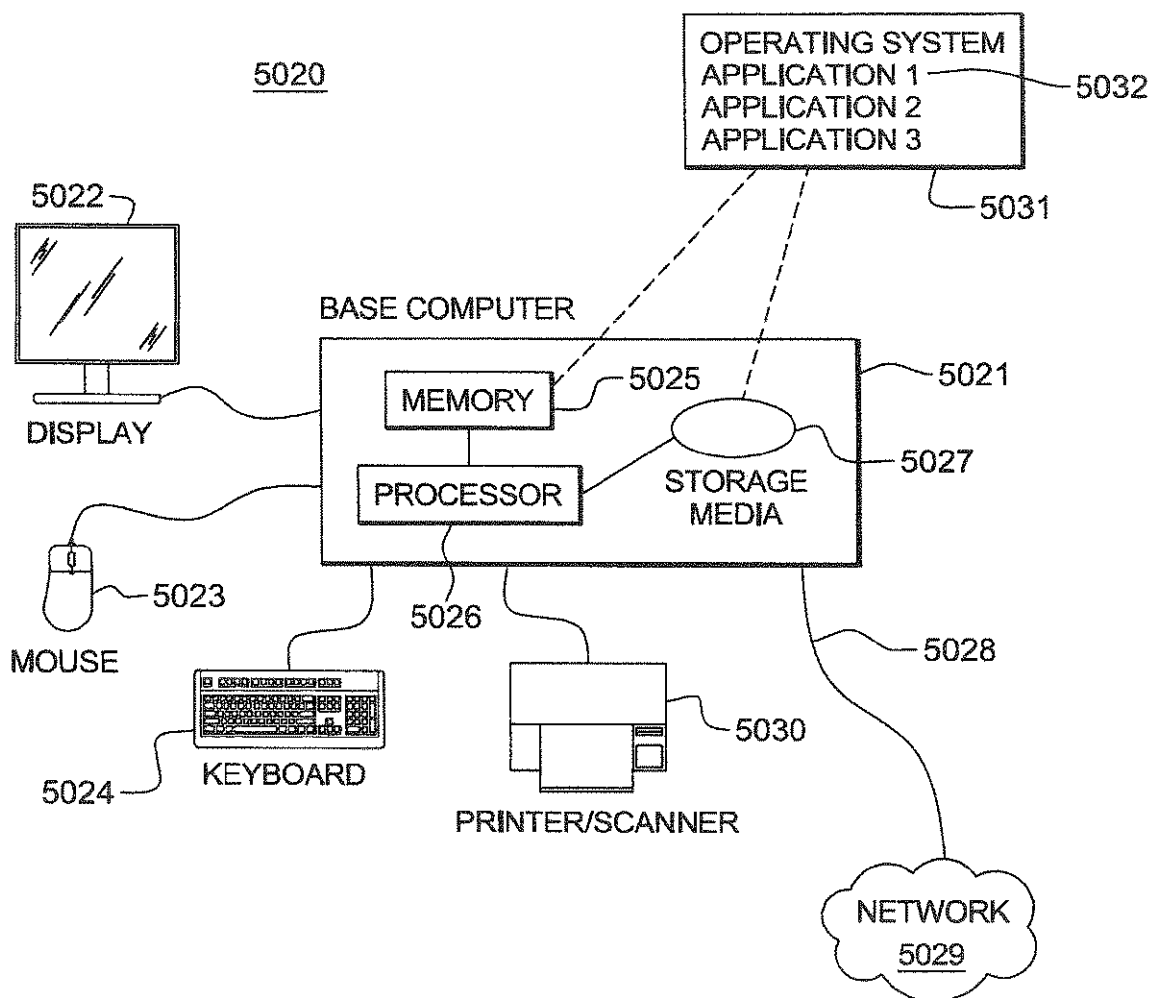


FIG. 14

16/21

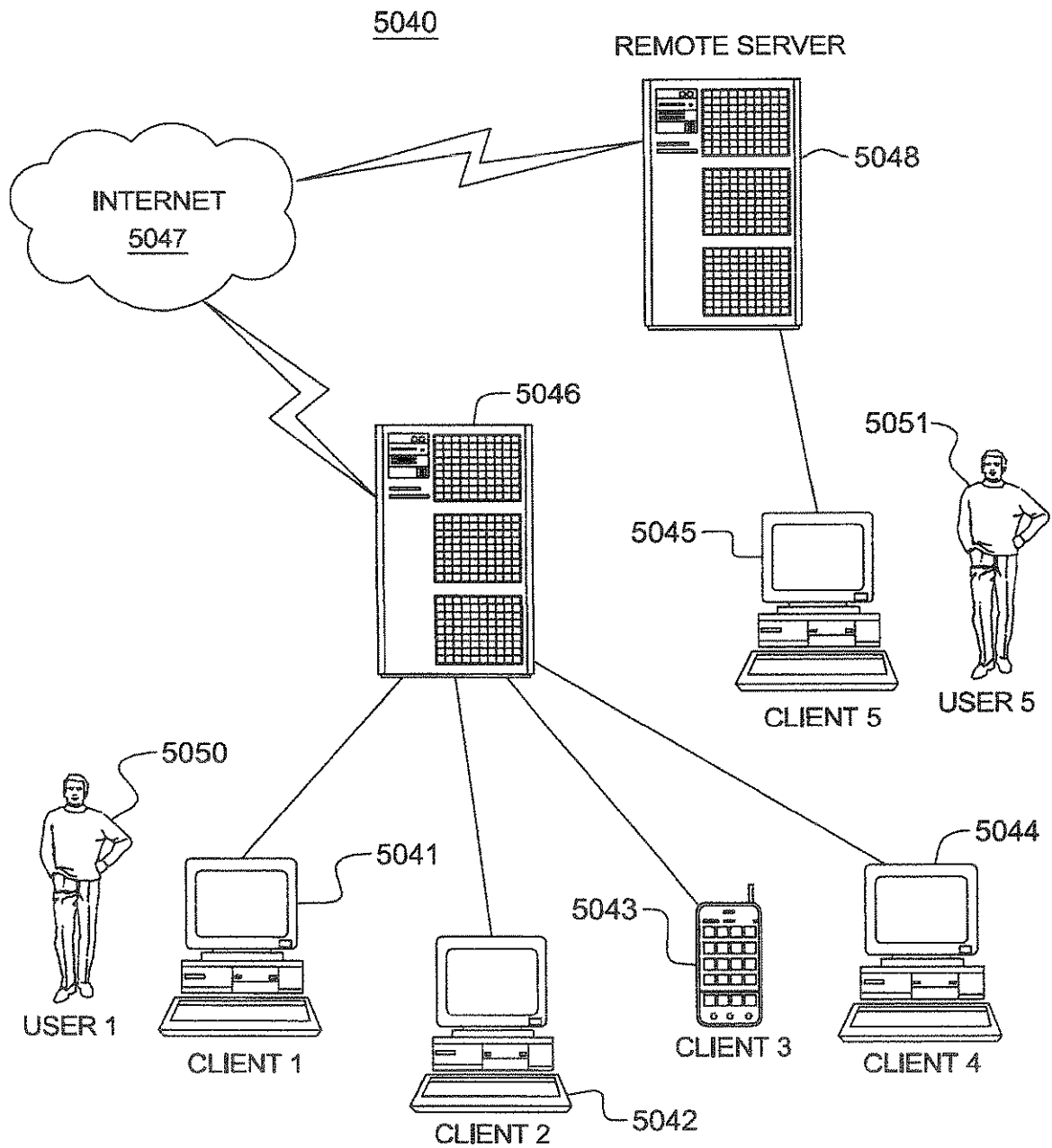


FIG. 15

17/21

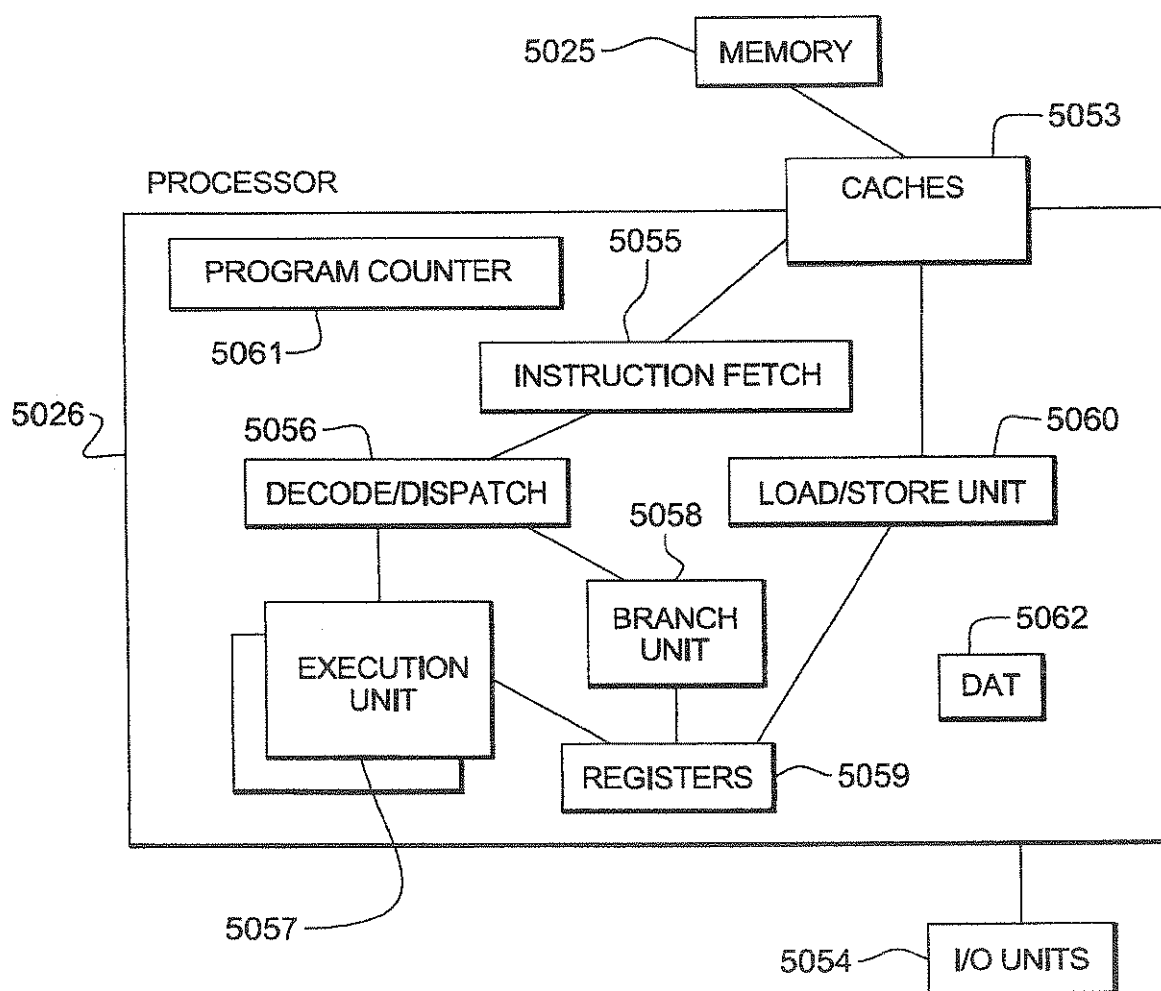


FIG. 16

18/21

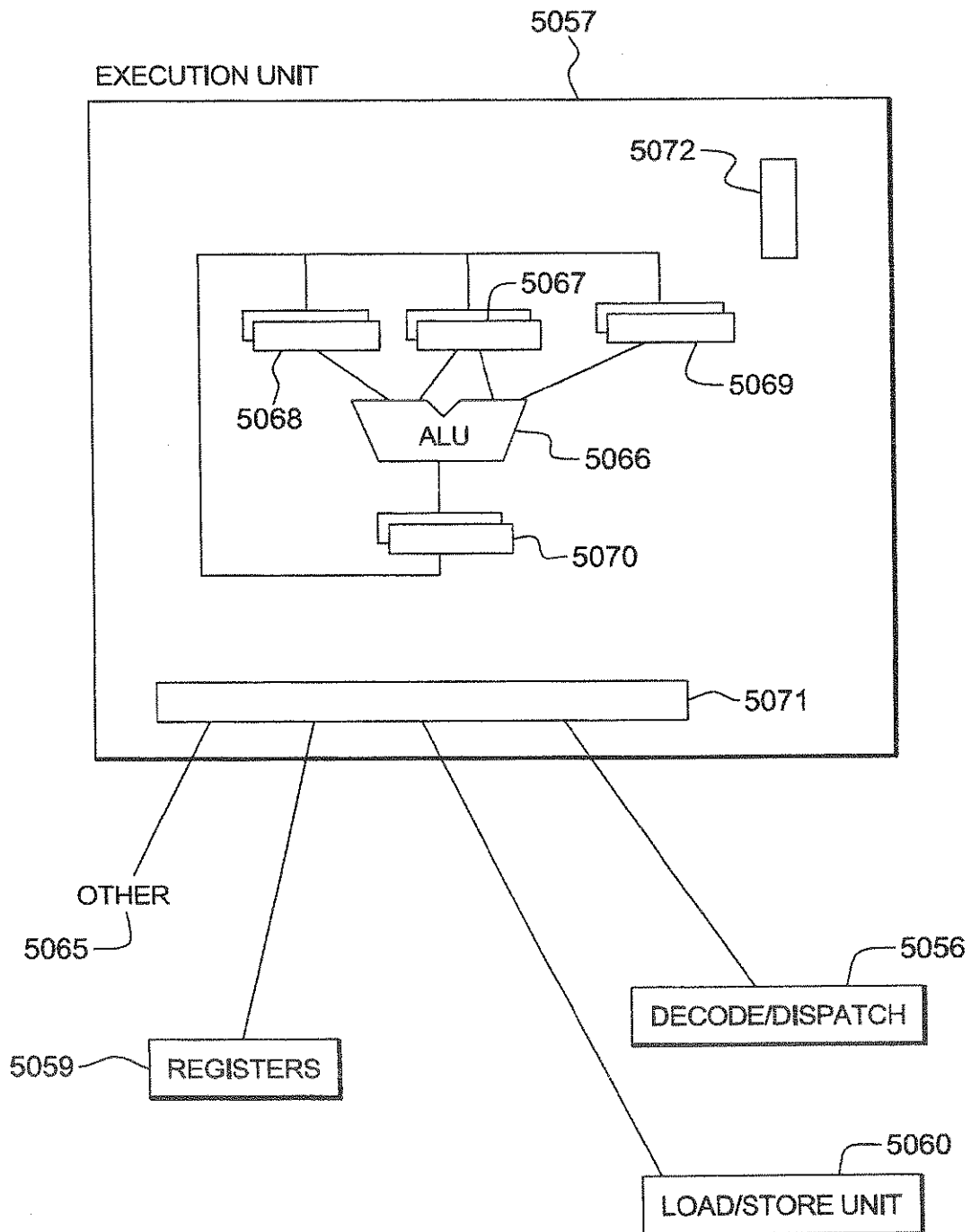


FIG. 17A

19/21

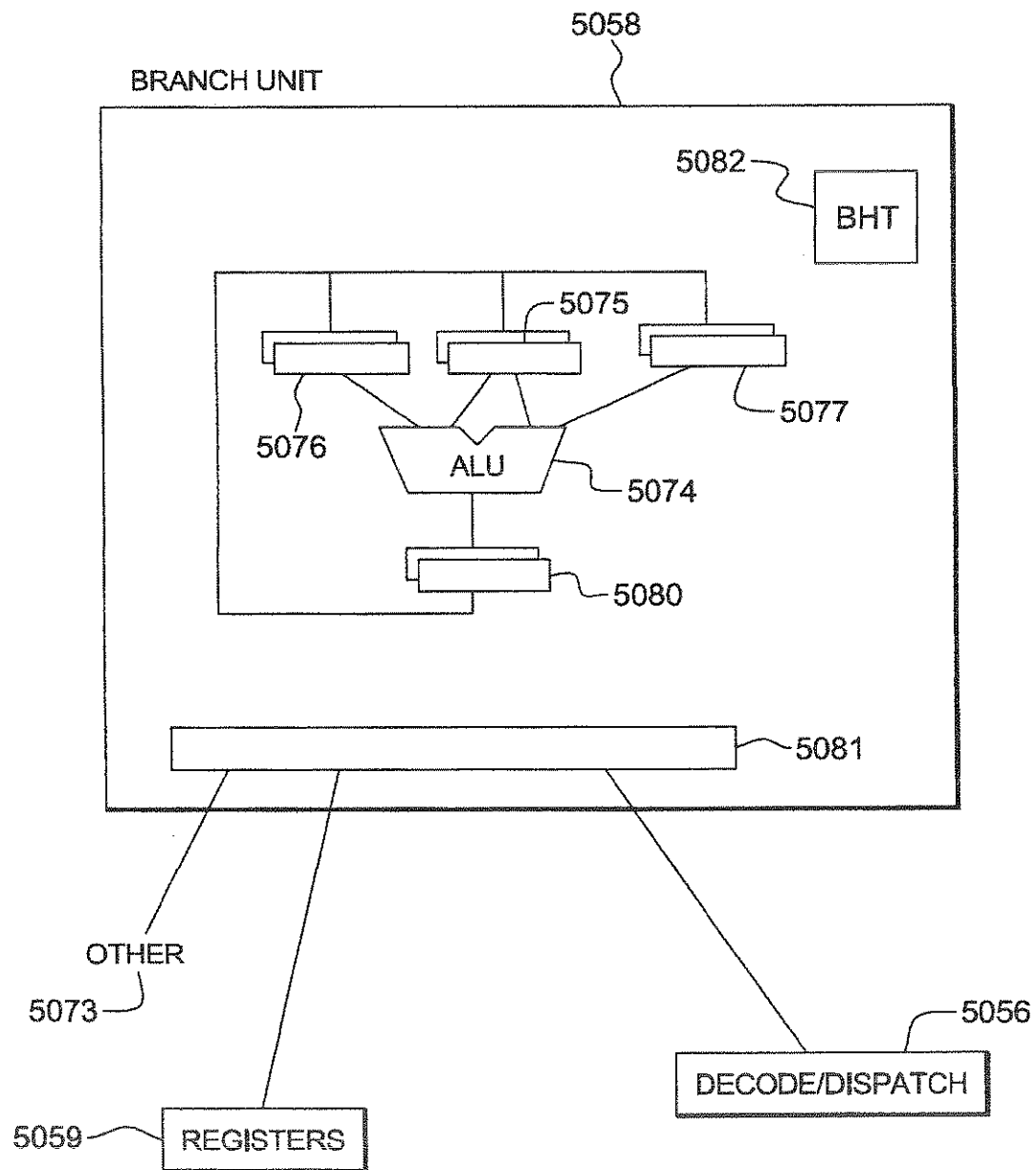


FIG. 17B

20/21

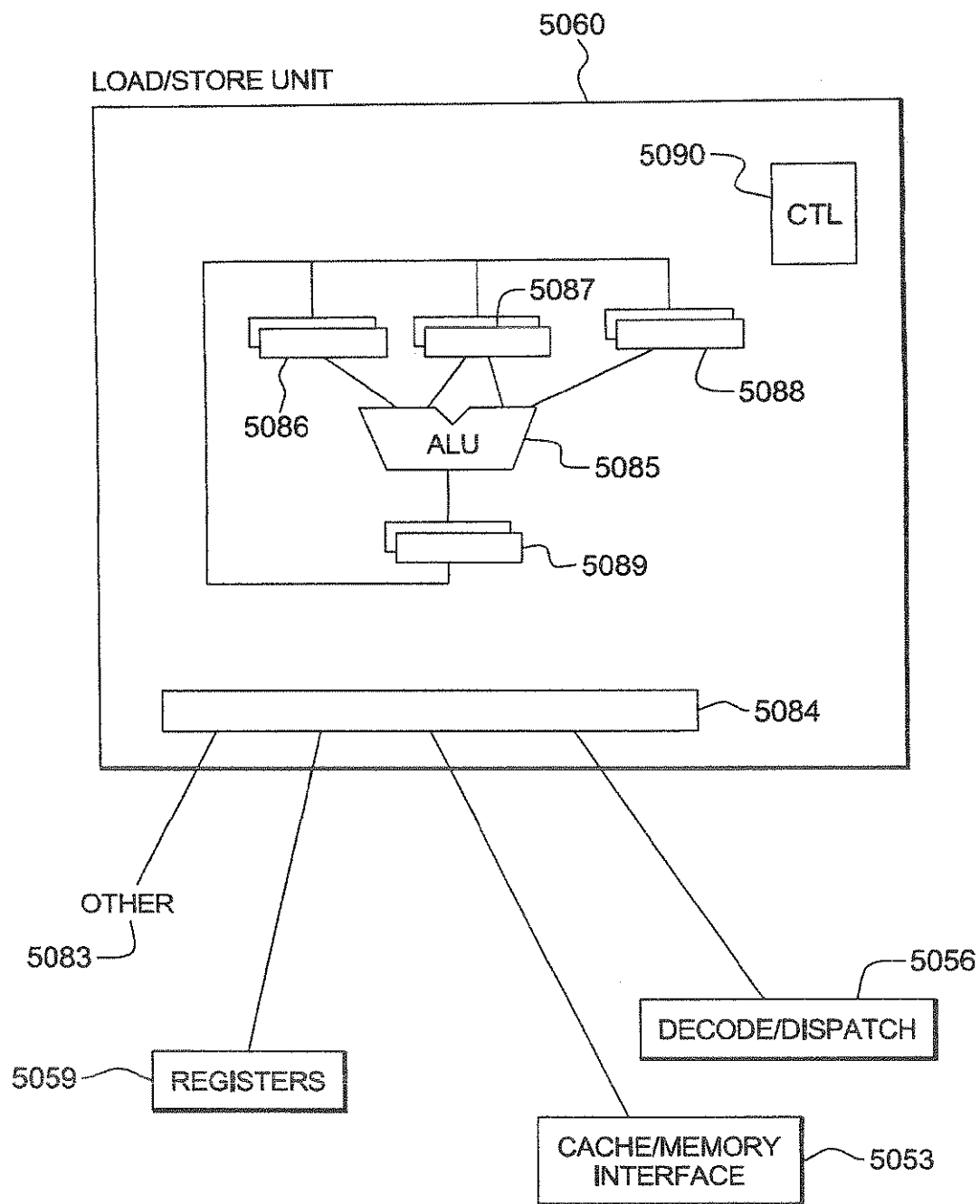


FIG. 17C

21/21

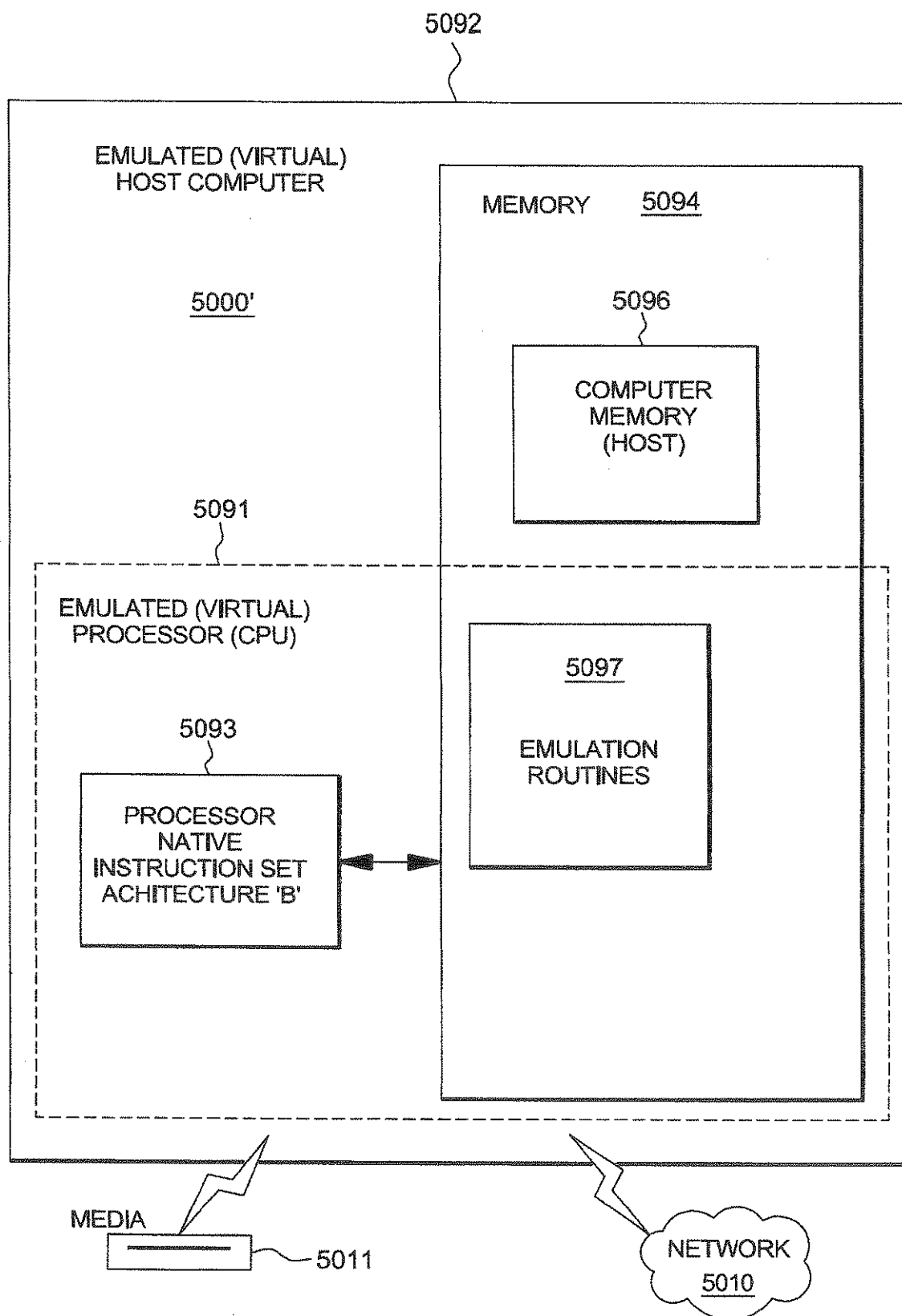


FIG. 18