

Abstract

Disclosed is a non-volatile semiconductor memory device that can reduce the occurrence of false reading operation due to voltage variation at a data reading operation as compared to conventional cases and can also reduce increase in electric power consumption due to voltage variation. This non-volatile semiconductor memory device (1) can reduce the occurrence of false reading operation due to voltage variation at a data reading operation as compared to a conventional case in which a drain side select gate electrode and a source side select gate electrode of different kinds, to which different voltages are likely to be applied, are connected with each other when manufacturing defect occurs, causing voltage variation in the entire non-volatile semiconductor memory device, and can also reduce increase in electric power consumption due to unintended voltage variation.