

Description

The invention relates to predictive coding and decoding and particularly, but not exclusively, to an interframe video coding system employing transform coding.

In a predictive encoding scheme, the receiver constructs a prediction of what the present value of a signal will be based upon its past values. Such schemes therefore generally employ a delay or store stage termed a predictor, which supplies past signal values (possibly weighted) to form a prediction of present signal values.

At the transmitter, a similar prediction is performed, and the difference between the predicted signal values and the actual signal values is encoded and transmitted as a difference signal to the receiver where it is added to the prediction to reconstitute an approximation of the actual signal.

Such systems may be analogue or digital; an example of a digital system is a digital video encoding system.

Video data is highly redundant, and it is therefore known to transmit video data employing an interframe predictor, which may also compensate for motion between frames. At the transmitter end of such a system, the difference signal values may be coded, in blocks of, for example, 8x8 picture elements (pixels), employing a spatial transform, and at the receiver the inverse transform is applied to decode the difference signal.

A commonly used transform is the Discrete Cosine Transform. The mathematical operations needed to perform it cannot be expressed exactly with a finite number of bits. Therefore practical implementations with different internal computing architectures produced, for example, by different manufacturers, can give slightly different results.

An inverse transform stage is located in both the coder and decoder. If these two do not produce exactly the same difference signal values at their outputs then the predictions at the encoder and decoder begin to diverge, and the resulting error becomes visible on the decoded picture.

This problem is tackled by specifying the maximum allowable error with respect to a (notional) very accurate version of the inverse transform.

Tests indicate that the two mean error parameters (the mean error on any pixel, and the mean error overall) are very important as they reflect bias, the presence of which results in a cumulatively increasing divergence between the pictures at the coder and decoder. The overall mean error thus becomes visible, as a steadily increasing or decreasing brightness of a picture block over many frames, or as an increasing colour cast.

Analogous problems occur in coding systems for other types of data (e.g. speech).

According to one aspect of the invention, there is provided a predictive decoder comprising means for processing a difference signal, means for supplying a prediction signal, and means for combining the processed difference signal and the prediction signal to form an output signal dependent thereon, the prediction signal being derived from the output signal so as to depend upon previous portions of the difference signal, characterised in that means are provided for periodically alternating the operation of the decoder between first and second states, in which the cumulative effect of any time-averaged bias caused by the processing means is, respectively, to increase and to deplete the prediction signal, the respective lengths of the periods spent in the first and second states being such as to reduce the tendency of such time-averaged bias error to accumulate in the prediction signal.

This has the advantages of reducing long-term perceptually significant errors in the decoded signal, and thereby requiring lower precision, or granting greater error-immunity in the decoder.

According to other aspects, defined in the sub-claims, corresponding transmitters and systems, and a digital signal processing device useful therein, are provided.

In a preferred embodiment, particularly useful in block transform coding video systems, this invention reduces the mean errors by inverting the polarity of the data into and out of the inverse transform stage at intervals such that any bias is averaged out over a period of time. The periods of inverted and non-inverted operation are preferably substantially equal on average.

Each such block of the picture must, over a period of several successive frames, be subject to both normal and inverted operation. For some coding schemes it may be possible to use alternate modes on alternate frames. However, some coders utilise frame dropping methods, and in these there could be correlation between the coding frame rate and the inversion rate such that the number of times each part of the picture used the normal and inverted modes of the inverse transform would not be substantially equal.

A random or pseudo-random generator is therefore preferably used to control the mode of the inverse transform.

An advantage of the invention is that this inverted mode is internal to the decoding operation and does not affect the data outside it. The technique may therefore be used at either of the coder or the decoder, or both, and no overhead signalling of normal/inverted mode is required.

The invention will now be illustrated, by way of example only, with reference to the accompanying drawings, in which:

- Figure 1 is a simplified block diagram of an

interframe hybrid DCT encoding transmission system according to one aspect of the invention.

Referring to Figure 1, the transmitter end of an interframe predictive video coder receives a video input signal. A subtraction stage 1 subtracts from the input an estimate of what the decoder will predict the input to have been; this estimate is supplied by a predictor 2, comprising a frame store. The difference signal is encoded by a DCT transform stage 3, in 8x8 blocks of pixel interframe samples, and the resulting transform coefficients corresponding to the encoded difference signal are transmitted to the receiver. The contents of the predictor 2 are updated, by supplying the transform coefficients to an inverse transform stage 4, which reconstitutes the difference signal. This is added to the fed-back current contents of predictor 2 in addition stage 5 and the result stored as an updated prediction by predictor stage 2.

These latter stages correspond to the operation of the receiver, where received transform coefficients are inverse transformed in an inverse transformation stage 6 to reconstitute the interframe difference signal which is added to the prediction signal supplied by interframe predictor 7 in addition stage 8, and the resultant reconstituted video is output for display or further processing, and is stored in predictor 7.

Typically, a quantizer will be included at the transmitter following the transform stage 3, and corresponding inverse quantizers preceding the inverse transform stages 4, 6 at either end; these have been omitted for clarity from Figure 1.

This much of the invention is disclosed in, for example, our previous European published patent applications Nos. EP-A-0 301712 and EP-A-0 309280.

A problem arises if the operation of a component (for example the inverse transform stage 6) in the signal path at the receiver generates a mean error different from that correspondingly generated in the local decoding stages at the transmitter. To compensate for the cumulative picture error generated, there are therefore provided in the receiver (and/or the local decoder stages in the transmitter) means for selectively inverting the difference signal prior to the error-generating stage, so that during inverted operation the sign of the error relative to the signal is reversed; referring to Figure 1, one simple method is to provide a pair of switchable invertors 9a, 9b under control of control means 10, bracketing the error-generating (inverse transform) stage 6, so that after re-inversion the transformed signal is of the correct sign but the bias mean error is inverted.

Another method of performing the invention retains invertor 9a upstream of the error-generating stage 6, but instead of positioning invertor 9b upstream of addition stage 8, two further invertor stages are provided; one between addition stage 8 and the output, and one between predictor 7 and addition stage 8; one skilled in the art will appreciate that the

result obtained in this case is mathematically equivalent to that shown in Figure 1. Conveniently, to replace invertor 9b or the two invertors described above, addition stage 8 could be controlled by alternately adding or subtracting the difference signal to or from the predictor signal under the control of control means 10; this reduces the number of mathematical operations involved.

However, it may equally be convenient to implement invertors 9a and 9b (and possibly control means 10) as part of a single digital signal processing (DSP) device with inverse transform stage 6; such a stand-alone device could then simply be a pin-compatible, 'invisible' replacement part.

If the error generating stage 6 is a digital arithmetic unit employing stored constants (for example, an inverse transform stage), an alternative embodiment of the invention provides alternate sets of such stored constants, such that the operation of the stage 6 when employing one set generates a mean error of opposite sign to its operation when employing the other, and the control means 10 in operation alternates periodically the sets employed.

It will be understood that in digital systems, invertor stages 9a, 9b are easily realised without multiplication. In signed binary systems, for example, the invertor merely needs to invert the state of the leading bit (e.g. by performing an exclusive-OR operation with a logical control signal from control means 10).

Control means 10 in a first embodiment simply operates as a bistable counter, alternating the operation of invertors 9a and 9b between inactive and inverting conditions at regular, preferably equal intervals (although, if the magnitude of the mean error in one state is known to be unequal to that in the other, the ratio of the intervals in each state will be made equal to the ratios of the magnitudes).

In another embodiment, useful in encoding video systems utilising frame dropping methods, the control means 10 employs a pseudo-random number generator, producing periods in each mode of equal length when averaged over time.

The technique is equally applicable to dedicated hardware devices (principally to digital devices, but in principle to analogue devices also), and to general purpose or dedicated computers operating under stored program control.

Claims

1. A predictive decoder comprising means for processing a difference signal, means for supplying a prediction signal, and means for combining the processed difference signal and the prediction signal to form an output signal dependent thereon, the prediction signal being derived from the output signal so as to depend upon previous por-



- tions of the difference signal, characterised in that means are provided for periodically alternating the operation of the decoder between first and second states, in which the cumulative effect of any time-averaged bias caused by the processing means is, respectively, to increase and to deplete the prediction signal, the respective lengths of the periods spent in the first and second states being such as to reduce the tendency of such time-averaged bias error to accumulate in the prediction signal.
2. A decoder according to claim 1 in which the means for processing a difference signal performs a digital arithmetic operation upon the difference signal input to the decoder using stored digital constant values, and the decoder includes means for inverting the polarity of the input difference signal relative to the digital constant values in one of said states.
 3. A decoder according to claim 2 in which the means for inverting operates to invert the difference signal prior to the said digital arithmetic operation.
 4. A decoder according to claim 2 in which the means for inverting operates to invert at least one of the stored digital constant values.
 5. A decoder according to claim 2, in which the means for inverting is connected to employ at least one different stored digital constant in each state.
 6. A decoder according to any one of claims 2 to 5, in which the means for processing a difference signal is arranged to perform an inverse transformation operation.
 7. A decoder according to any preceding claim, arranged to supply as an output signal a video signal.
 8. A decoder according to claim 7, in which the means for supplying a prediction signal is a frame store connected to receive the output signal.
 9. A decoder according to any preceding claim, further comprising means for controlling the alternation between the said states so that successive periods in a given state are not all of equal length.
 10. A decoder according to claim 9, in which the means for controlling the alternation is a pseudo-random number generator.
 11. A predictive encoder for producing a coded difference signal for transmission, including a decoder according to any preceding claim connected to receive the coded difference signal, the coded difference signal being produced in dependence upon the difference between the encoder input and the prediction signal.
 12. A transmission system including an encoder or a decoder according to any preceding claim.
 13. A digital signal processing device for a predictive coding system, the device comprising means for processing an incoming coded difference signal to produce an output difference signal and means for alternating the device between a first and second state, the time-average of any bias error in the output signal being of opposite sign in said first and second states, whereby alternating the device periodically between the first and second states reduces the long-term average error in the output signal.
 14. A digital signal processing device according to Claim 13 characterised in that the alternating means comprises two invertors, one of which precedes the processing means and the other of which follows the processing means.

30 Patentansprüche

1. Prädiktiver Decodierer, mit einer Einrichtung, die ein Differenzsignal verarbeitet, einer Einrichtung, die ein Vorhersagesignal liefert, und einer Einrichtung, die das verarbeitete Differenzsignal und das Vorhersagesignal kombiniert, um in Abhängigkeit davon ein Ausgangssignal zu erzeugen, wobei das Vorhersagesignal in der Weise aus dem Ausgangssignal abgeleitet wird, daß es von früheren Abschnitten des Differenzsignals abhängt, dadurch gekennzeichnet, daß Einrichtungen vorgesehen sind, die den Betrieb des Decodierers zwischen ersten und zweiten Zuständen periodisch wechseln, in denen die kumulative Wirkung jeglichen durch die Verarbeitungseinrichtung hervorgerufenen zeitgemittelten systematischen Fehlers das Vorhersagesignal erhöht bzw. erniedrigt, wobei die Längen der in den ersten bzw. in den zweiten Zuständen verbrachten Perioden so bemessen sind, daß die Neigung zu einer Akkumulation eines derartigen zeitgemittelten systematischen Fehlers im Vorhersagesignal reduziert wird.
2. Decodierer nach Anspruch 1, in dem die Einrichtung, die ein Differenzsignal verarbeitet, unter Verwendung von gespeicherten, digitalen konstanten Werten eine digitale arithmetische Ope-



- ration an dem in den Decodierer eingegebenen Differenzsignal ausführt und der Decodierer eine Einrichtung enthält, die in einem der Zustände die Polarität des eingegebenen Differenzsignals relativ zu den digitalen konstanten Werten invertiert.
3. Decodierer nach Anspruch 2, in dem die Invertierungseinrichtung in der Weise arbeitet, daß sie das Differenzsignal vor der digitalen arithmetischen Operation invertiert. 5 10
 4. Decodierer nach Anspruch 2, in dem die Invertierungseinrichtung in der Weise arbeitet, daß wenigstens einer der gespeicherten, digitalen konstanten Werte invertiert wird. 15
 5. Decodierer nach Anspruch 2, in dem die Invertierungseinrichtung so angeschlossen ist, daß sie in jedem Zustand wenigstens eine unterschiedliche, gespeicherte digitale Konstante verwendet. 20
 6. Decodierer nach irgendeinem der Ansprüche 2 bis 5, in dem die Verarbeitungseinrichtung, die ein Differenzsignal erzeugt, so beschaffen ist, daß sie eine inverse Transformationsoperation ausführt. 25
 7. Decodierer nach irgendeinem vorangehenden Anspruch, der so beschaffen ist, daß er als Ausgangssignal ein Videosignal liefert. 30
 8. Decodierer nach Anspruch 7, in dem die Einrichtung, die ein Vorhersagesignal liefert, ein Rahmenspeicher ist, der so angeschlossen ist, daß er das Ausgangssignal empfängt. 35
 9. Decodierer nach irgendeinem vorangehenden Anspruch, der ferner eine Einrichtung enthält, die den Wechsel zwischen den Zuständen in der Weise steuert, daß aufeinanderfolgende Perioden in einem gegebenen Zustand nicht sämtlich gleiche Länge besitzen. 40
 10. Decodierer nach Anspruch 9, in dem die Einrichtung, die den Wechsel steuert, ein Generator für Pseudozufallszahlen ist. 45
 11. Prädiktiver Codierer, der ein codiertes Differenzsignal zum Senden erzeugt, einen Decodierer nach irgendeinem vorangehenden Anspruch enthält und so angeschlossen ist, daß er das codierte Differenzsignal empfängt, wobei das codierte Differenzsignal in Abhängigkeit von der Differenz zwischen dem Codierereingang und dem Vorhersagesignal erzeugt wird. 50 55
 12. Sendesystem, das einen Codierer oder einen Decodierer nach irgendeinem vorangehenden Anspruch enthält. 5
 13. Digitalsignal-Verarbeitungsvorrichtung für ein prädiktives Codierungssystem, wobei die Vorrichtung eine Einrichtung, die ein eingehendes, codiertes Differenzsignal verarbeitet, um ein ausgehendes Differenzsignal zu erzeugen, sowie eine Einrichtung enthält, die die Vorrichtung zwischen einem ersten und einem zweiten Zustand wechselt, wobei das zeitliche Mittel jeglichen systematischen Fehlers im ausgehenden Signal in den ersten bzw. zweiten Zuständen entgegengesetztes Vorzeichen besitzt, wobei der periodische Wechsel der Vorrichtung zwischen den ersten und zweiten Zuständen den Langzeit-Mittelungsfehler im ausgehenden Signal reduziert. 10
 14. Digitalsignal-Verarbeitungsvorrichtung nach Anspruch 13, dadurch gekennzeichnet, daß die Wechseleinrichtung zwei Invertierer enthält, wovon einer der Verarbeitungseinrichtung vorhergeht und der andere der Verarbeitungseinrichtung folgt. 15

Revendications

1. Décodeur prédictif comprenant un moyen destiné à traiter un signal de différence, un moyen destiné à appliquer un signal de prédiction, et un moyen destiné à combiner le signal de différence traité et le signal de prédiction de façon à former un signal de sortie dépendant de ceux-ci, le signal de prédiction étant obtenu à partir du signal de sortie de façon à ce qu'il dépende des parties précédentes du signal de différence, caractérisé en ce qu'un moyen est procuré pour alterner périodiquement le fonctionnement du décodeur entre des premier et second états, dans lequel l'effet cumulatif de toute polarisation moyennée dans le temps provoquée par le moyen de traitement consiste, respectivement, à accroître et à diminuer le signal de prédiction, les longueurs respectives des périodes passées dans les premier et second états étant telles qu'elles réduisent la tendance d'une telle erreur de polarisation moyennée dans le temps à s'accumuler dans le signal de prédiction. 10
2. Décodeur selon la revendication 1 dans lequel le moyen destiné à traiter un signal de différence effectue une différence arithmétique numérique sur l'entrée de signal de différence vers le décodeur en utilisant des valeurs constantes numériques mémorisées et le décodeur comprend un moyen destiné à inverser la polarité du signal de 15



- différence d'entrée par rapport aux valeurs constantes numériques dans l'un desdits états.
3. Décodeur selon la revendication 2 dans lequel le moyen destiné à inverser fonctionne de façon à inverser le signal de différence avant ladite opération arithmétique numérique. 5
 4. Décodeur selon la revendication 2 dans lequel le moyen destiné à inverser fonctionne de façon à inverser au moins l'une des valeurs constantes numériques mémorisées. 10
 5. Décodeur selon la revendication 2, dans lequel le moyen destiné à inverser est relié de façon à utiliser au moins une constante numérique mémorisée différente dans chaque état. 15
 6. Décodeur selon l'une quelconque des revendications 2 à 5, dans lequel ledit moyen de traitement destiné à engendrer un signal de différence est agencé de façon à effectuer une opération de transformation inverse. 20
 7. Décodeur selon l'une quelconque des revendications précédentes, agencé pour appliquer en tant que signal de sortie un signal vidéo. 25
 8. Décodeur selon la revendication 7, dans lequel le moyen destiné à appliquer un signal de prédiction consiste en une mémoire de trame reliée de façon à recevoir le signal de sortie. 30
 9. Décodeur selon l'une quelconque des revendications précédentes, comprenant en outre un moyen destiné à commander l'alternance entre lesdits états de façon à ce que des périodes successives dans un état donné ne soient pas toutes d'égales longueurs. 35
 10. Décodeur selon la revendication 9, dans lequel le moyen destiné à commander l'alternance consiste en un générateur de nombre pseudo-aléatoire. 40
 11. Codeur prédictif destiné à produire un signal de différence codé destiné à l'émission, comprenant un décodeur selon l'une quelconque des revendications précédentes relié de façon à recevoir le signal de différence codé, le signal de différence codé étant produit suivant la différence entre l'entrée du codeur et le signal de prédiction. 45
 12. Système de transmission comprenant un codeur ou un décodeur selon l'une quelconque des revendications précédentes. 50
 13. Dispositif de traitement du signal numérique destiné à un système de codage prédictif, le dispo-

sitif comprenant un moyen destiné à traiter un signal de différence codé entrant, afin de produire un signal de différence de sortie et un moyen pour faire alterner le dispositif entre un premier et second états, la moyenne dans le temps de toute erreur de polarisation du signal de sortie étant de signe opposé dans lesdits premier et second états, d'où il résulte que la mise en alternance du dispositif périodiquement entre les premier et un second état réduit l'erreur moyenne à long terme dans le signal de sortie.

14. Dispositif de traitement de signal numérique selon la revendication 13 caractérisé en ce que le moyen de mise en alternance comprend deux inverseurs dont l'un précède le moyen de traitement et dont l'autre suit le moyen de traitement.