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A selecting electrode drive circuit for a matrix liquid crystal display

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates generally to a matrix type display device and particularly to a selecting electrode drive circuit suitable for use in a matrix liquid crystal display such as a liquid crystal television.

A matrix type liquid crystal display is well known as consisting essentially of two electroded-transparencies separated by a sealed-in liquid crystal material such as a twisted nematic type liquid crystal or a guest-host type liquid crystal. The outer surface of each transparency has a transparent conductive coating in the form of parallel rows or columns. The electroded transparencies face to each other with their row and column electrodes crosswise to each other, thereby forming a rectangular array of intersections of their row and column electrodes. Thus, a matrix results. In operation, a series of pulses at regular intervals are applied to the row electrodes that is selecting electrodes one after another, thus sequentially bringing these selecting electrodes to a given potential for a very short period.

On the other hand, video signals representing a

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piece of visual information to be displayed are applied to the column electrodes that is data electrodes, thereby darkening the liquid crystal at selected intersections enough to form a visible shape.

With a view to extending the life of the liquid crystal used in a matrix type liquid crystal display device, the selecting of the electrodes is performed by alternately using positive-going pulses and negative-going pulses as for instance follows: In interfaced scanning, alternate electrodes are driven by positive-going pulses in one frame and the remaining electrodes by negative-going pulses in the next frame. Otherwise, the selecting is performed by applying alternating pulses at regular intervals to the selecting electrodes one after another.

There has been an ever increasing demand for improving the resolution of a matrix type liquid crystal display device. The resolution of the display will increase with the increase of the number of selecting (row) and data (column) electrodes. The increase of the number of selecting and electrodes, however, will lead to the decrease of the duration of each driving pulse enough to assure that driving pulses cannot bring adjacent selecting electrodes to their active states at the same moment. In order to assure that selected intersections of the liquid are darkened enough to form a visible image, the decrease of pulse dura-

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tion will have to be compensated by increasing the amplitude or height of pulse. As a matter of fact, the amplitude of each driving pulse need be multiplied by the square root of the number of rows or columns.

A selecting electrode drive circuit usually uses C-MOS devices whose breakdown voltage ranges from about 20 to 22 volts. This figure of breakdown voltage of the semi-conductor device limits accordingly the resolution of a matrix type liquid crystal display.

With a view to expanding the limit of resolution beyond the one permitted by the breakdown voltage of semi-conductor devices used in a matrix type display device the object of the present invention is to provide a selecting electrode drive circuit which is capable of providing driving pulses of twice as high amplitude as the breakdown voltage of semi-conductor devices, thus permitting a substantial increase of the number of selecting and data electrodes in the matrix electrode, and hence a corresponding increase of resolution in the matrix type display device.

SUMMARY OF THE INVENTION

In accordance with the present invention a selecting electrode circuit for a matrix liquid crystal display comprises a pulse generator for generating, at an output thereof, a series of regularly spaced reference pulses; a switching circuit for generating output signals from said reference pulses, said switching circuit having two inputs for receiving said series of reference pulses and a level shifted series of said reference pulses respectively; and

a clamping circuit for generating said level-shifted series of reference pulses, said clamping circuit comprising a capacitor connected in a series circuit between said two inputs of said switching circuit, one plate of

said capacitor being connected to said pulse generator output and the other plate of said capacitor being connected to a semi-conductor device, said semi-conductor and device being arranged to alternately earth and isolate from earth said other plate in dependence upon the instantaneous potential at said pulse generator output, thereby to generate said level-shifted series of reference pulses.

The invention also provides a matrix liquid crystal display incorporating such a drive circuit,

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a selecting electrode drive circuit;

Fig. 2 shows a train of reference pulses supplied by a pulses generator and another train of pulses level-shifted by the same amount as the reference pulse amplitude;

Fig. 3(A), 3(B), 3(C), and 3(D), show waveforms of desired drive pulses;

Fig. 4 shows a wiring diagram of an embodiment of a switching circuit;

Fig.5 shows waveforms of signals appearing at different portions of the switching circuit of Fig. 4;

Fig. 6 shows a wiring diagram of another embodiment of a switching circuit;

Fig. 7 shows waveforms of signals appearing at different portions of the switching circuit of Fig.6; and

Figs 8,9, 10,11 and 12 show selecting electrode drive circuits using different sources of electric potential.

Other objects and advantage of the present invention will be understood from the following description of preferred embodiments of the present invention.

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DETAILED DESCRIPTIONS OF THE PREFERRED EMBODIMENTS

Fig. 1 shows a schematically a selecting electrode or sweeping circuit which illustrates the background of the present invention. As shown in the drawing, it comprises a pulse generator 1, a battery or source of electric potential 3 connected to the pulse generator 1 and a switching circuit 5 connected across the battery 3. The voltage Vm of the battery 3 is selected to be equal to the breakdown voltage of C-MOSs used in the switching circuit 5. The height or amplitude Vm of reference pulses provided by the pulse generator 1 is selected to be equal to the voltage of the battery 3 and hence the breakdown voltage of the semiconductor devices used in the switching circuit. With this arrangement a train of reference pulses V_1 (t) are supplied to one (positive) of the two input terminals of the switching circuit 5 by the pulse generator 1. At the same time the train of reference pulses V_1(t) are level-shifted by the same amount as the reference pulse, and the level-shifted pulse signals V_2 are supplied to the other (negative) input terminal of the switching circuit 5. The switching circuit 5 is designed to sample these different waveforms V_1 (t) and V_2 (t) (see Fig.2) and combine the so sampled parts into a desired phase-shifted alternating drive signal V_3 (t) essentially consisting of positive going pulses and negative going pulses (see Figs, 3A, 3B, 3C and 3D)

and 3D).

Specifically, a designed drive pulse signal $V_3(t)$ as shown in the left half of Fig. 3A is built up by selecting as long portions as reference pulse width from the waveforms $V_1(t)$ and $V_2(t)$ in the order of V_1, V_1, V_1, V_2, V_1, V_2 ... and so forth. A desired drive pulse signal as shown in the right half of Fig. 3A is built up by reversing the waveforms $V_1(t)$ and $V_2(t)$ and by selecting so long portions as reference pulse width from these reversed waveforms $\overline{V}_1(t)$ and $\overline{V}_2(t)$ in the order of $\overline{V}_2$, $\overline{V}_2$, $\overline{V}_1$, $\overline{V}_2$ ... and so forth.

In producing a drive pulse signal as shown in Fig. 3B, as long portions as pulse width are selected from the waveforms V_1 and V_2 in the order of V_1, V_1, V_2, V_1, V_1, V_2 ... V_1, V_1, V_2, V_2, V_1, V_2 ..., and the so selected portions are combined one after another.

Desired drive pulse signals as shown in Figs. 3C and 3D are built up by narrowing the width of the pulse signal shown in Fig. 3A by use of clock pulses of high frequency. Thus width narrowed drive pulse signals are effectively used to control the brightness of the visual images as displayed.

Fig. 4 shows an embodiment of a switching circuit arrangement appropriate for the purpose of building a desired drive pulse as shown in Fig. 3A. The switching circuit 5 is shown as consisting essentially of a toggle type flip-flop 51, an EXCLUSIVE-OR gate 52 connected to the

"Q" terminal of the flip-flop 51, a four-bit binary counter 53 connected to the EXCLUSIVE-OR gate 52 and as many selecting units 54, 55, ... as the selecting electrodes of the matrix. These selecting units are connected to the EXCLUSIVE-OR gate 52 and the four-bit binary counter 53. As shown, each selecting unit consists of a decoder 541, 551, ..., an EXCLUSIVE-OR gate 542, 552, ... and an inverter 543, 553... The switching circuit is driven by the reference pulse signal $V_1(t)$ and the level-shifted pulse signal $V_2(t)$ as shown in the Fig. 4. The decoder 541 of the first selecting unit 54 is responsive to the five bit signal consisting of the four bit output (0001) of the counter 53 and the output signal CK'(1) from the EXCLUSIVE-OR gate 52 for providing a negative-going pulse in coincidence with the first reference pulse just counted (see "S", in Fig. 5). Likewise, the decoder 551 of the second selecting unit 55 is responsive to the five bit signal consisting of the four bit output (0001) of the counter 53 and the output signal CK'(0) from the EXCLUSIVE-OR gate 52 for providing a negative-going pulse in coincidence with the inter-pulse space subsequent to the first reference pulse. The decoder of the "n"th selecting unit (not shown) is responsive to the four bit output of the counter (53) and the output signal CK' from the output signal from the EXCLUSIVE-OR gate 53 for providing a negative-going pulse.

Taking the first selecting unit 54 as an example, the output S_1 of the decoder 541 and the signal CK' are given to the EXCLUSIVE-OR gate 542 to produce the output S_2 as shown in Fig. 5. The output S_2 of the EXCLUSIVE-OR gate 542 is inverted by the inverter 543 to produce the output S_3 as shown in Fig. 5. As mentioned above, as the switching circuit is supplied as its driving power source with the reference pulse signal $V_1(t)$ and the level-shifted pulse signal $V_2(t)$, the output OUT1 as shown in Fig. 5 is taken out of the first selecting unit 54. Likewise the output OUT2 also as shown in Fig. 5 is taken out of the second selecting unit 54 half a period of clock signals CK' later.

Fig. 6 shows another embodiment of a switching circuit arrangement for building a desired drive pulse as shown in Fig. 3B. The arrangement of the switching circuit is similar to that of the switching circuit shown in Fig. 4 except that the reset signal R and the clock signal CK are directly applied to the counter 53. In this embodiment, like components are designated by like reference numerals and explanation thereof is omitted.

Fig. 7 shows waveforms of signals appearing at different portions of the switching circuit of Fig. 6. Operation of the circuit is similar to that of the embodiment shown in Fig. 4 and thus the drive signals shown as OUT1 and OUT2 in Fig. 7 can be taken out of the switching

circuit.

Fig. 8 shows a selecting electrode drive circuit having a clamping unit as a source of electric potential according to the present invention.

As shown in the drawing, the clamping unit 3 consists of a capacitor 31 and a diode 32. One plate (left in the drawing) of the capacitor 31 is connected to the positive terminal of the pulse generator 1 and the positive terminal of the switching circuit 5. The other plate (right in the drawing) of the capacitor 31 is connected to the anode of the diode 32 and to the negative terminal of the switching circuit 5. The cathode of the diode 32 is grounded.

In operation, a train of reference pulses V_1 as shown in Fig. 2 are applied to the clamping unit 3, particularly to the capacitor 31 of the clamping unit 3. Assume that a positive going pulse is applied to the capacitor 31, and then an electric current flows to the ground through the capacitor 31 and the diode 32, thereby charging the capacitor 31 to as high a potential Vm as the crest of the reference pulse. When the reference pulse disappears, the potential of the left plate of the capacitor 31 descends to zero, or the potential of the ground, and consequently the right plate of the capacitor 31 descends to -Vm, thereby causing the diode 32 to be backward biased. Thus, a train

of pulses which are level-shifted by the same amount as the amplitude or height of the reference pulses (broken lines in Fig. 2), result.

As earlier described, the switching circuit 5 functions to sample these reference pulses V_1 and level-shifted pulses V_2 and combine the sampled portions for providing desired train of alternating pulses V_3 at the output terminal of the switching circuit 5. Then, the switching circuit 5 works with the voltage Vm applied thereacross, providing pulses whose peak-to-peak amplitude is twice as large as Vm.

Fig. 9 shows another selecting electrode drive circuit having a similar clamping unit 3. As shown in the drawing the clamping unit 3 has extra capacitor 31' and diode 32'. These extra elements are connected in the symmetrical relation with the capacitor 31 and the diode 32 with respect to the input terminals of the switching circuit 5 and the ground, thereby making equal the impedance Z_{PG} as viewed from the positive terminal of the switching circuit 5 and the ground towards the pulse generator 1 and the impedance Z_{NG} as viewed from the negative terminal of the switching circuit 5 and the ground. Because otherwise, the absolute value of the crest of the positive-going pulse would be different from that of the negative-going pulse. The clamping unit 3 works in the same way as that of the

sequential drive circuit of Fig. 8.

Fig. 10 shows still another selecting electrode drive circuit having a clamping unit as a source of electric potential. The clamping unit 3 uses a switching transistor in place of a clamping diode, thereby reducing the voltage drop across the clamping element (for instance, about 0.6 volts for a silicon diode if used) to a possible minimum (about 0.01 volts).

As shown in Fig. 10, the clamping unit 3 essentially consists of a switching transistor 33 whose collector and emitter electrodes are connected to the negative terminal of the switching circuit 5 and the ground, respectively. A clamping capacitor 31 connected between the collector electrode of the transistor 33 and the positive terminal of the pulse generator 1, a bias resistor 35 connected between the emitter electrode and the base electrode of the transistor 33, a dc-blocking capacitor connected to the joint between the resistor 35 and the base electrode of the transistor 33, and an inverter 36 connected between the capacitor 34 and the positive terminal of the pulse generator 1.

In operation assume that a positive-going pulse is applied both to the inverter 36 and the clamping capacitor 31. Then, the positive-going pulse is inverted by the inverter 36, and the resultant negative-going pulse is applied to the base electrode of the transistor 33 after passing

through the capacitor 34, thereby putting the transistor 33 in its conductive state, and causing the capacitor 31 to be charged with electricity to as high a potential as the crest of Vm the positive-going pulse. Then, the first positive-going pulse disappears at the input terminal of the inverter 36 to bring the transistor 33 in its non-conductive state. The left plate of the clamping capacitor 31 is at the ground potential, and consequently the right plate of the clamping capacitor descends to -Vm. Thus, a train of pulses level-shifted by the same amount as the amplitude or height of the reference pulse are applied to the negative terminal of the switching circuit 5 while a train of reference pulses are applied to the positive terminal of the switching circuit 5.

Fig. 11 shows a modification of the clamping unit of the selecting electrode drive circuit of Fig. 10. Specifically, it contains a symmetric counterpart to the switching structure of the clamping unit of Fig. 10 for the purpose of impedance balancing as viewed from the positive and negative terminals of the switching circuit 5 towards the pulse generator 1.

Finally, Fig. 12 shows a selecting electrode drive circuit using still another clamping unit 3 as a source of electric potential according to the present invention. As shown, the clamping unit 3 essentially consists of a clamp-

ing capacitor 31 connected between the negative terminal of the switching circuit 5 and the positive terminal of the pulse generator 1, an inverter 37 connected to the ground at its input terminal and across the switching circuit 5, and a field effect transistor 38 whose source, gate and drain electrodes are connected to the negative terminal of the switching circuit 5, the output terminal of the inverter 37 and the ground, respectively.

In operation, if a positive-going pulse of the reference pulses generated by the pulse generator 1 is applied to the inverter 37, then the transistor 38 becomes conductive, so that the clamping capacitor 31 is charged to as high a potential as the crest of the applied positive-going pulse. When the first positive-going pulse of the reference pulses disappears, the transistor 38 is brought into non-conductive state by the inverter 37 and then the left plate of the clamping capacitor 31 will be at the ground potential and consequently the potential of the right plate of the clamping capacitor 31 descends to -Vm. Thus, a train of pulses as level-shifted by the same amount as the amplitude or height of the reference pulse are applied to the negative terminal of the switching circuit 5 while a train of reference pulses are applied to the positive terminal of the switching circuit.

It is to be understood that, although the invention

has been described in connection with particular embodiments, the invention should not be limited thereto and can be subjected to various changes and modifications without departing from the scope of the invention.

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CLAIMS:

1. A selecting electrode drive circuit for a matrix liquid crystal display, comprising:

a pulse generator for generating, at an output thereof, a series of regularly spaced reference pulses;

a switching circuit for generating output signals from said reference pulses, said switching circuit having two inputs for receiving said series of reference pulses and a level shifted series of said reference pulses respectively; and

a clamping circuit for generating said level-shifted series of reference pulses, said clamping circuit comprising a capacitor connected in a series circuit between said two inputs of said switching circuit, one plate of said capacitor being connected to said pulse generator output and the other plate of said capacitor being connected to a semi-conductor device, said semi-conductor and device being arranged to alternately earth and isolate from earth said other plate in dependence upon the instantaneous potential at said pulse generator output, thereby to generate said level-shifted series of reference pulses.

2. A drive circuit as claimed in claim 1 wherein said semi-conductor device comprises a diode where anode is connected to said other plate and where caltrode is connected to earth.

3. A drive circuit as claimed in claim 1 wherein said semi-conductor device comprises a transistor where main electrodes are connected between said other plate and earth, and whose control electrode is coupled to the output of an inverter.

4. A drive circuit as claimed in any preceding claim wherein a further capacitor is included in said series circuit, connected at one plate thereof to said first-mentioned capacitor, further semi-conductor device being connected

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between earth and the other plate of said further capacitor and being correspondingly poled to said first mentioned semi-conductor device so as to from a balanced circuit, whereby both inputs of said switching circuit experience the same pulse generator output impedance.

5. A drive circuit as claimed in claim 3 wherein said inverter is connected across said inputs of said switching circuit, the input of said inverter is connected to ground, and said transistor is a field-effect transistor where source, gate and drain electrodes are connected to said other plate of said capacitor, the output of said inverter and ground, respectively,

6. A drive circuit as claimed in claim 3, or claim 4 as dependent on claim 3, wherein the or each said transistor is a bipolor transistor whose bare is coupled via a coupling capacitor to an inverter output, the corresponding inverter input being connected to the pulse generator output.

7. A selecting electrode drive circuit for a matrix liquid crystal display, substantially as described hereinabove with reference to any of Figures 8 to 12 in conjunction with eigher Figures 4 and 5 or Figures 6 and 7 of the accompanying drawings.

8. A matrix liquid crystal display incorporating a selecting electrode drive circuit as claimed in any preceding claim.