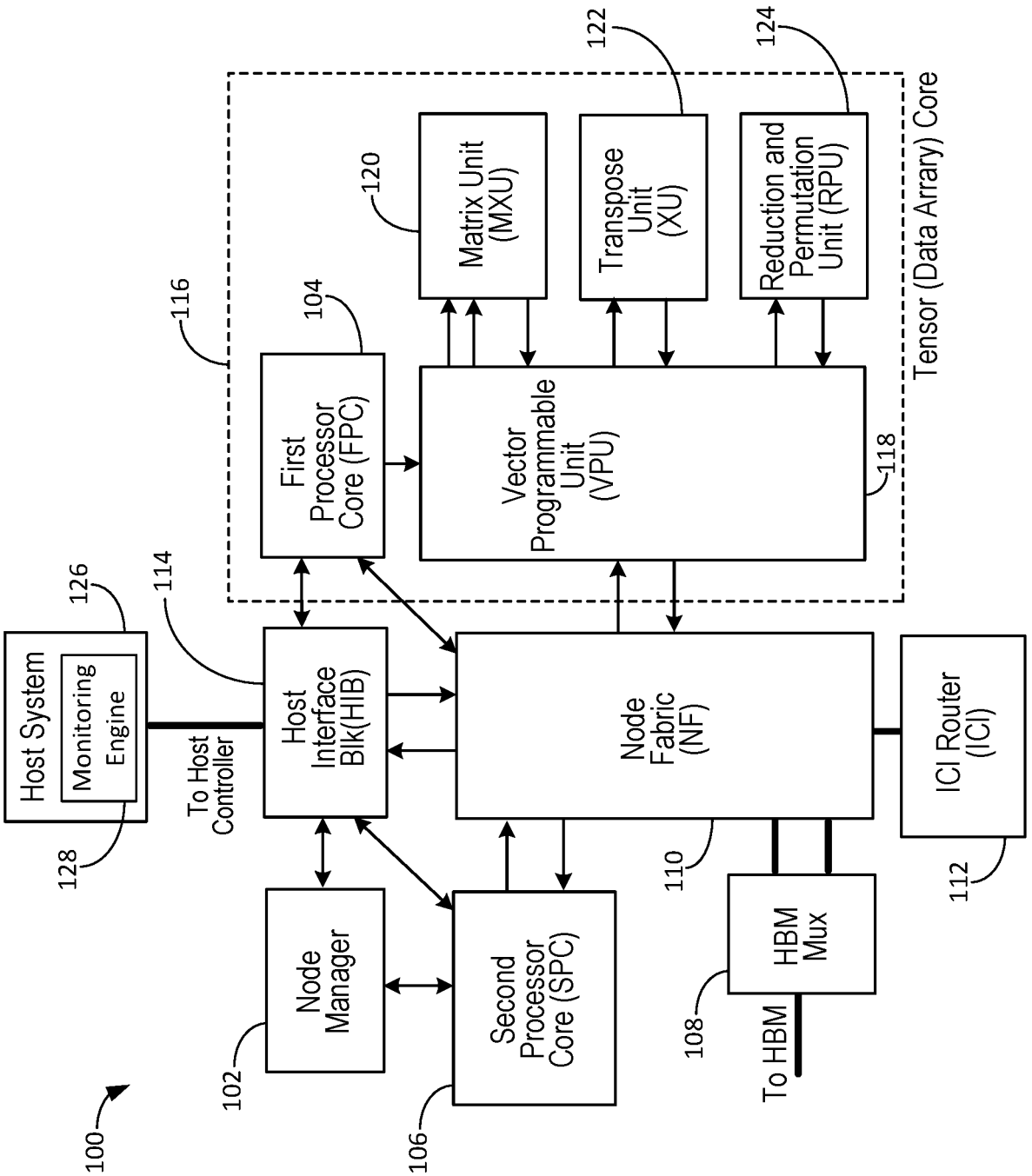

100
102
Node Manager
104
First Processor Core (FPC)
106
Second Processor Core (SPC)
108
HBM Mux
To HBM
110
Node Fabric (NF)
112
ICI Router (ICI)
114
Host Interface Blk(HIB)
To Host Controller
116
Tensor (Data Arrary) Core
118
Vector Programmable Unit (VPU)
120
Matrix Unit (MXU)
122
Transpose Unit (XU)
124
Reduction and Permutation Unit (RPU)
126
Host System
Monitoring Engine
128

FIG. 1

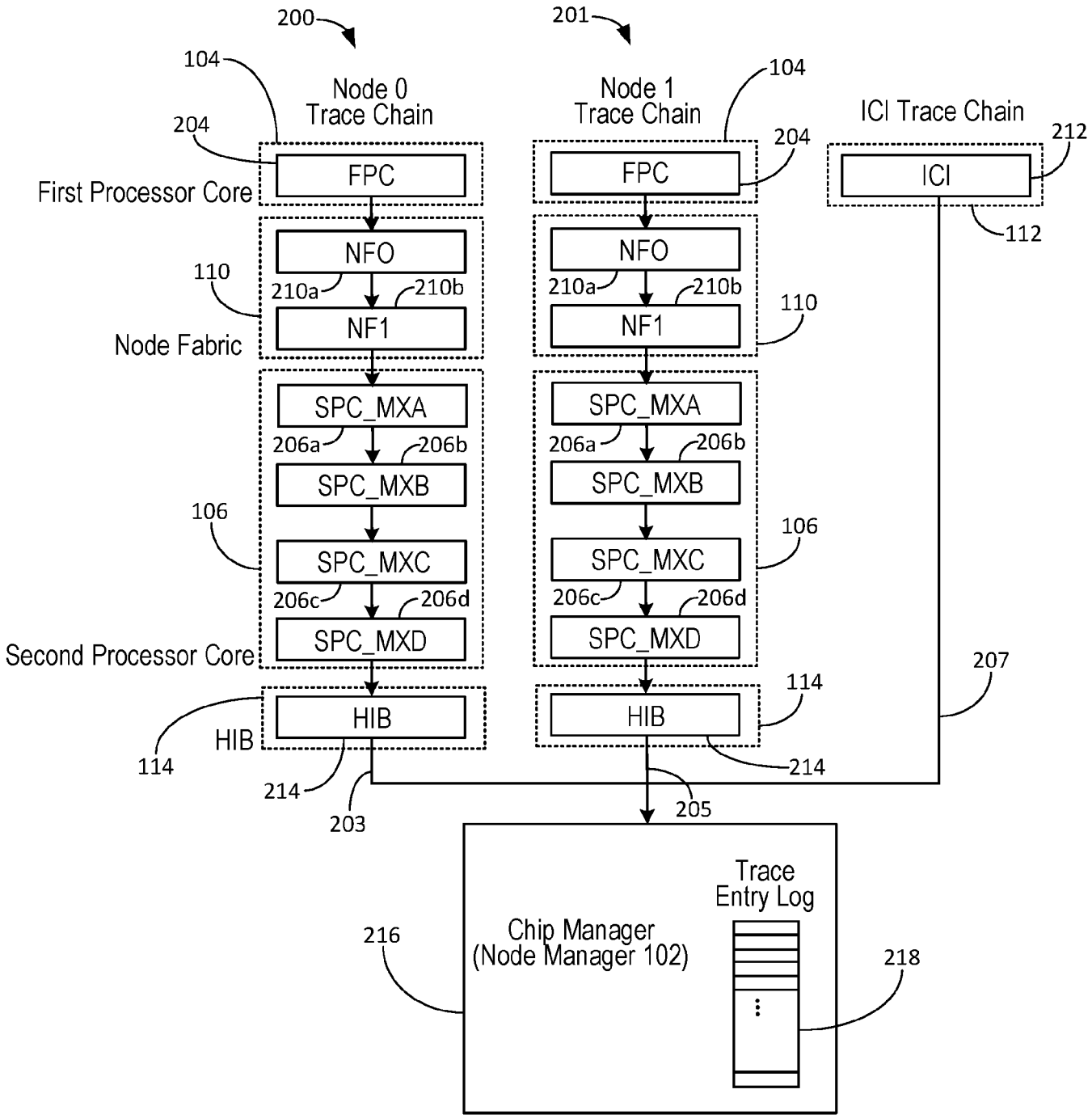
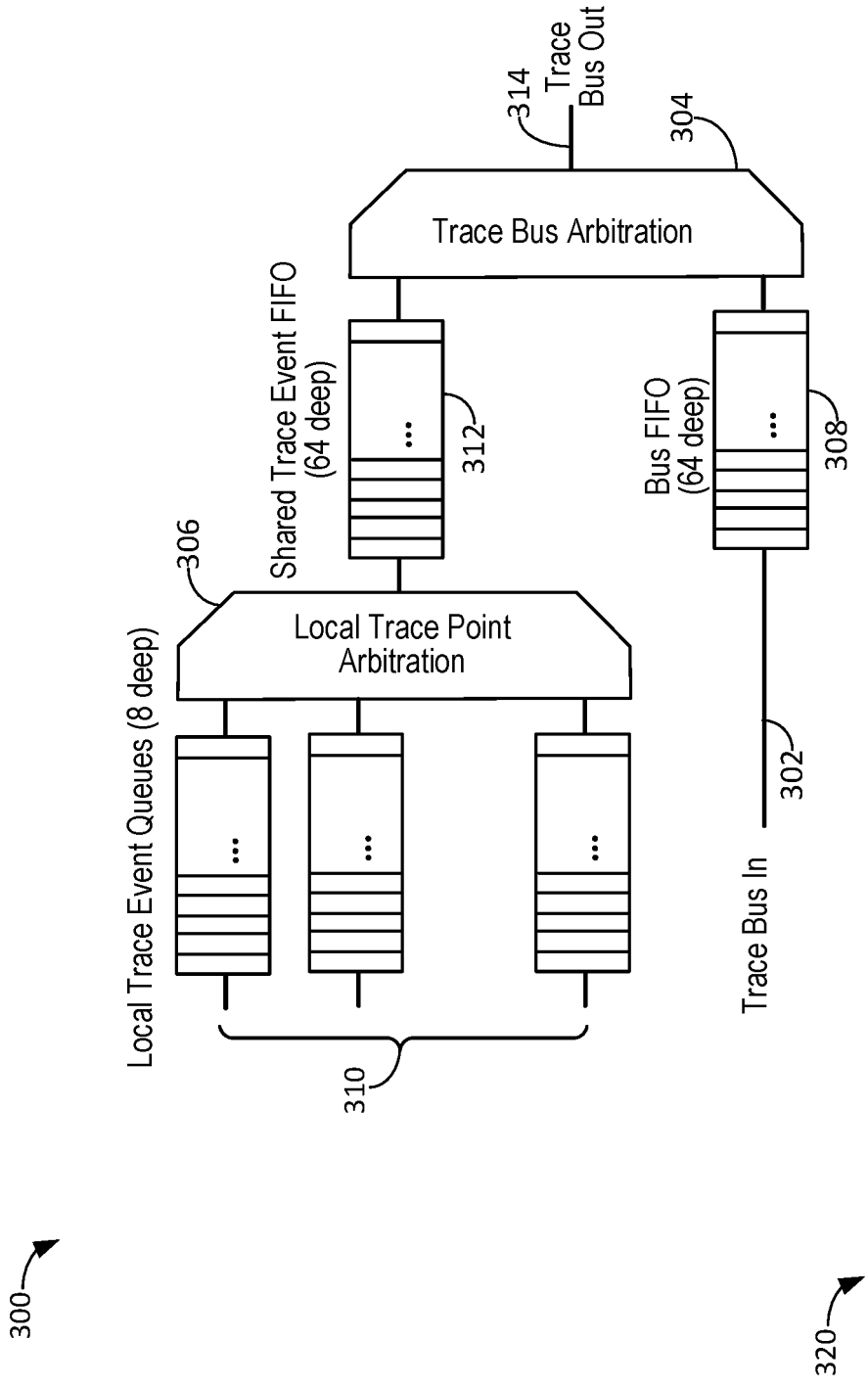

200
201
104
Node 0
Trace Chain
204
FPC
First Processor Core
NFO
110
210a
210b
NF1
Node Fabric
SPC_MXA
206a
206b
SPC_MXB
106
SPC_MXC
206c
206d
SPC_MXD
Second Processor Core
HIB
114
214
203
205
Node 1
Trace Chain
ICI Trace Chain
212
ICI
112
207
Trace
Entry Log
Chip Manager
(Node Manager 102)
216
218

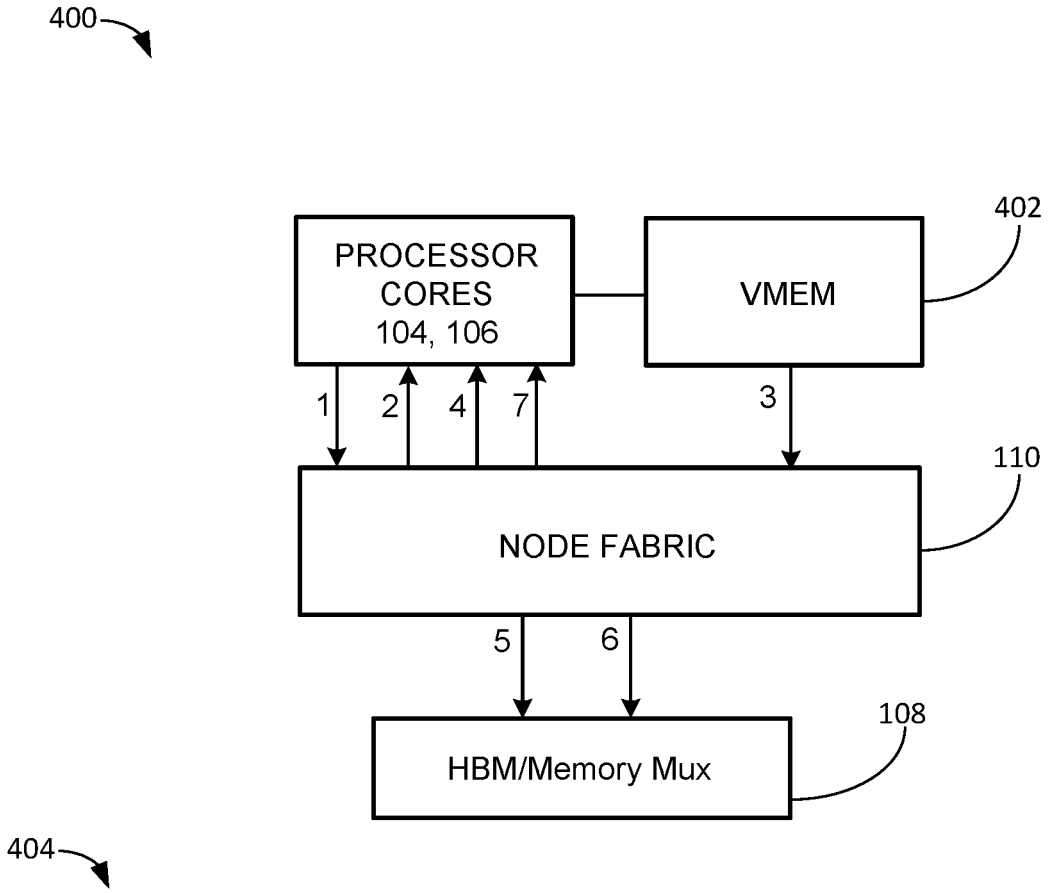
FIG. 2



Time	Trace ID	Source	Destination	Component(s)	Trace Event	Size	Latency
09:01.13	000001	0x00F100	0x00F200	FPC → FPC	DMA	128 bytes	9µs
09:05.27	000002	0x00F300	0x00F400	FPC → SPC	DMA	256 bytes	.023ms
09:12.35	000003	0x00F500	0x00F600	SPC → NF	DMA (issued)	512 bytes	.xxx secs
09:12.49	000003	0x00F600	0x00F700	NF → HBM	DMA (executed)	512 bytes	.xxx secs
09:12.58	000003	0x00F700	0x00F800	NF → FPC	DMA (complt)	512 bytes	.xxx secs

320
322
324

FIG. 3



STEP	OPERATION
1	INITIAL DMA REQUEST; TRACEPOINT IN NODE FABRIC
2	READ CMD: NF ASKS CORE TO TRANSFER DATA; TRACEPOINT IN NF
3	READ COMPLETE: NO TRACEPOINT IN NF HERE!
4	READ RESOURCE UPDATE: SYNC FLAG UPDATE IN CORE; TRACEPOINT IN FPC
5	WRITE CMD: NF NOTIFIES HBM; TRACEPOINT IN NF
6	WRITE COMPLETE: TRACEPOINT IN NF
7	WRITE RESOURCE UPDATE: SYNCH FLAG UPDATES IN FPC; TRACEPOINT IN FPC

FIG. 4

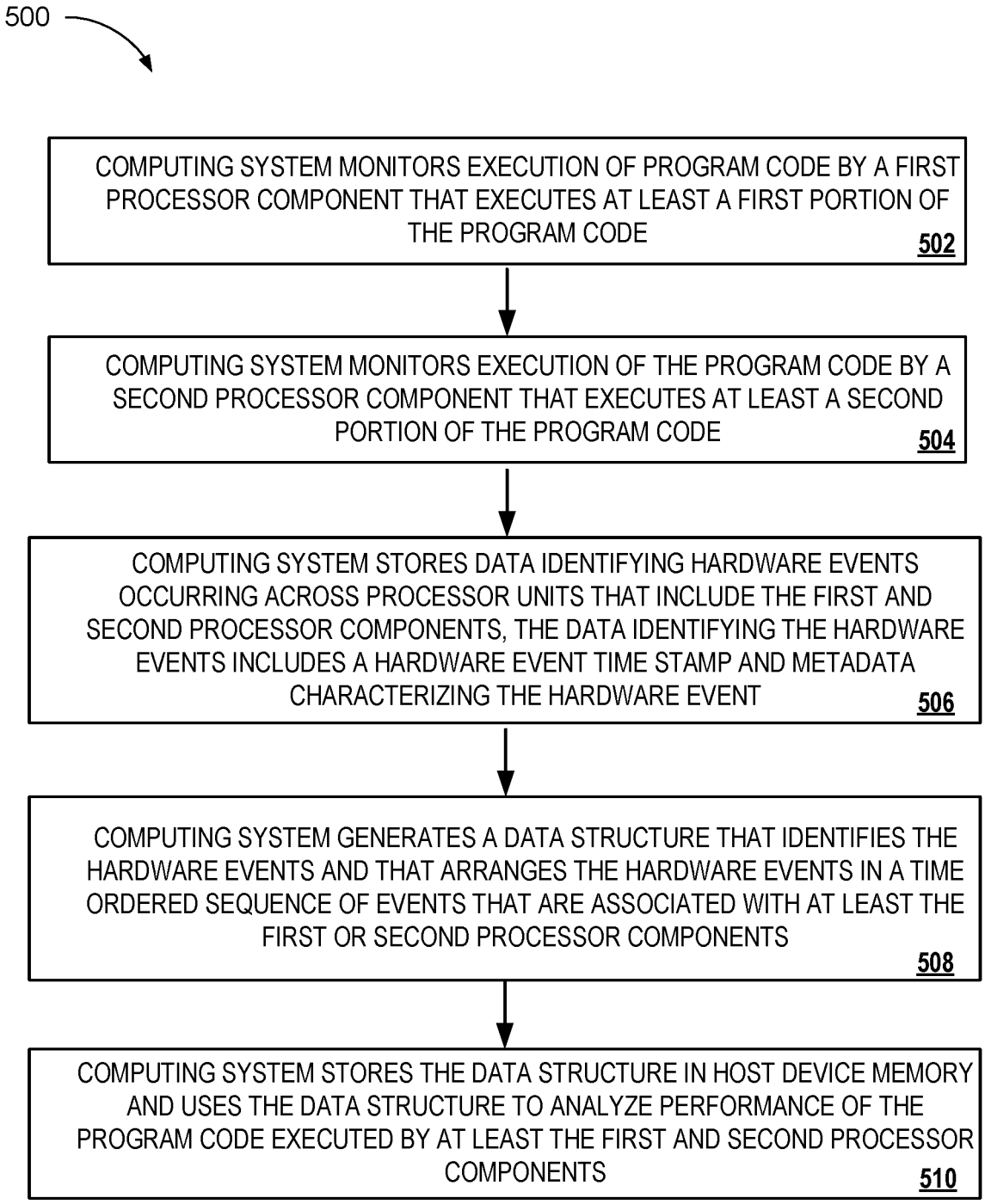

500
COMPUTING SYSTEM MONITORS EXECUTION OF PROGRAM CODE BY A FIRST PROCESSOR COMPONENT THAT EXECUTES AT LEAST A FIRST PORTION OF THE PROGRAM CODE
502
COMPUTING SYSTEM MONITORS EXECUTION OF THE PROGRAM CODE BY A SECOND PROCESSOR COMPONENT THAT EXECUTES AT LEAST A SECOND PORTION OF THE PROGRAM CODE
504
COMPUTING SYSTEM STORES DATA IDENTIFYING HARDWARE EVENTS OCCURRING ACROSS PROCESSOR UNITS THAT INCLUDE THE FIRST AND SECOND PROCESSOR COMPONENTS, THE DATA IDENTIFYING THE HARDWARE EVENTS INCLUDES A HARDWARE EVENT TIME STAMP AND METADATA CHARACTERIZING THE HARDWARE EVENT
506
COMPUTING SYSTEM GENERATES A DATA STRUCTURE THAT IDENTIFIES THE HARDWARE EVENTS AND THAT ARRANGES THE HARDWARE EVENTS IN A TIME ORDERED SEQUENCE OF EVENTS THAT ARE ASSOCIATED WITH AT LEAST THE FIRST OR SECOND PROCESSOR COMPONENTS
508
COMPUTING SYSTEM STORES THE DATA STRUCTURE IN HOST DEVICE MEMORY AND USES THE DATA STRUCTURE TO ANALYZE PERFORMANCE OF THE PROGRAM CODE EXECUTED BY AT LEAST THE FIRST AND SECOND PROCESSOR COMPONENTS
510

FIG. 5