METHODS FOR FORMING NARROW VERTICAL PILLARS AND INTEGRATED CIRCUIT DEVICES HAVING THE SAME

Technical Field

[0001] This invention relates generally to integrated circuit fabrication and, more particularly, to processes for forming thin vertical pillars and to the resultant integrated circuit devices, which may include phase change memory cells.

Background

[0002] As a consequence of many factors, including demand for increased portability, computing power, memory capacity and energy efficiency, the density of electrical features in integrated circuits is continuously increasing. To facilitate this scaling, the sizes of these electrical features are constantly being decreased.

[0003] The trend of decreasing feature size is evident, for example, in memory circuits or devices such as read only memory (ROM), random access memory (RAM), flash memory, resistive memory, etc. Examples of resistive memories include phase change memory, programmable conductor memory, and resistive random access memory (RRAM). To take one example, resistive memory devices may include arrays of cells organized in a cross point architecture. In this architecture, the memory cells may include a cell stack having a storage element, e.g., a phase change element, in series with a select device, e.g., a switching element such as an ovonic threshold switch (OTS) or diode, between a pair of conductive lines, e.g., between an access line and a data/sense line. The memory cells are located at the intersections of a word line and bit line and may be "selected" via application of appropriate voltages to those lines. Decreasing the sizes of the memory cells may increase cell density and/or memory device performance.

[0004] Accordingly, there is a continuing need for methods for providing integrated circuit features having small sizes.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The invention will be better understood from the Detailed Description of the Preferred Embodiments and from the appended drawings, which are meant to illustrate

and not to limit embodiments of the invention. It will be appreciated that the drawings are not necessarily to scale, nor are features in the same drawing necessarily on the same scale as other features.

[0006] Figure 1 shows schematic, cross-sectional side and top-down views of a partially fabricated integrated circuit.

[0007] Figure 2 shows schematic, cross-sectional side and top-down views of the partially fabricated integrated circuit of Figure 1 after forming mandrels on a first level and forming spacers along sidewalls of the mandrels.

[0008] Figure 3 shows schematic, cross-sectional side and top-down views of the partially fabricated integrated circuit of Figure 2 after filling gaps at sides of the spacers.

[0009] Figure 4 shows schematic, cross-sectional side and top-down views of the partially fabricated integrated circuit of Figure 3 after recessing spacers to form an open spacer volume and forming, e.g., depositing, a material in the open spacer volume.

[0010] Figure 5 shows schematic, cross-sectional side and top-down views of the partially fabricated integrated circuit of Figure 4 after forming mandrels on a second level and forming spacers along sidewalls of the mandrels.

[0011] Figure 6 shows schematic, cross-sectional side and top-down views of the partially fabricated integrated circuit of Figure 5 after filling gaps at sides of the spacers on the second level.

[0012] Figure 7 shows schematic, cross-sectional side and top-down views of the partially fabricated integrated circuit of Figure 6 after removing the spacers on the second level thereby forming an open spacer volume on the second level and also removing exposed material in the spacer volume on the first level.

[0013] Figure 8 shows schematic, cross-sectional side and top-down views of the partially fabricated integrated circuit of Figure 7 after forming, e.g., depositing, material in the open volume on the second level.

[0014] Figure 9 shows schematic, cross-sectional side and top-down views of the partially fabricated integrated circuit of Figure 8 after defining free-standing stacks.

[0015] Figure 10 shows a schematic, perspective view of a memory cell.

[0016] Figure 11 shows a cross-sectional top-down view the memory cell of Figure 10.

DETAILED DESCRIPTION

[0017] Embodiments disclosed herein have application to and encompass various types of integrated circuits and related apparatus. For example, while not limited to memory devices, some embodiments may be applied to memory devices, including resistive memories, such as phase change memory. It will be appreciated that phase change memory (PCM) exploits the ability of some materials to assume two or more stable resistance states. For example, memory cells may be formed with phase change materials that may assume stable crystalline and amorphous states, which have different electrical resistivities. In some cases, the crystalline state can have a lower resistivity than the amorphous state. The difference in resistivity can be used to store information; for example, the different resistance states may be used to represent different binary states (e.g., "1" states or "0" states). In some configurations, a phase change memory cell may be stably placed in more than two states, with each state having a different resistivity, thereby allowing the cell to store more information than a binary state cell.

[0018] The state of the phase change memory in a memory cell may be changed by application of an electrical signal to the cell. Without being limited by theory, phase change materials are understood to change state by the application of heat, with different levels of heat causing transitions to different states. Thus, the electrical signal can provide energy to a heating element proximate the phase change material (e.g., a resistive heating wire adjacent the phase change material), thereby causing the heating device to generate heat, which causes the phase change material to change state. It will be appreciated that the quantity of heat that is desired determines the amount of energy supplied to the heater, and that quantity of heat is at least partly determined by the amount of phase change material present in a phase change memory cell.

[0019] In some embodiments, an integrated circuit may be formed having narrow, vertically-extending openings filled with material, such as phase change material and/or a heating element. To form these openings, crossing lines of sacrificial material, e.g., spacers,

are formed on different vertical levels. The lines on a level may be substantially parallel, while the lines on different levels cross one another. The lines of material can be formed by deposition processes that allow the formation of very thin pillars, e.g., pillars with widths less than the minimum resolution of photolithography processes used to define other features in the integrated circuit. Material at the intersection of the lines is selectively removed to form openings, which have dimensions determined by the widths of the lines and, thus, can have dimensions less than that formed by photolithography. The openings can be filled with material to form a pillar of the material. For example, phase change material and/or a conductive material for forming a heating element can be deposited in the openings. Electrodes can be provided above and below the opening to allow electrical connection to other circuitry (e.g., bit lines and word lines).

[0020] As described herein, various embodiments allow the formation of openings or pillars, which may be exceptionally narrow and uniform. These openings or pillars can provide benefits in various applications. For example, they can allow the formation of integrated circuits with exceptionally small features. In some embodiments, the amount of phase change material in a memory cell may be reduced relative to forming the cell with processes such as photolithography. Reducing the amount of phase change material present may decrease the sizes of the memory cell, and the smaller amount of material to be heated may decrease the power requirements of the heater for the memory cell. This can lower overall heat levels in a memory device containing arrays of memory cells, improving reliability and reducing the possibility that heating a particular memory cell may disturb the state of neighboring memory cells. In addition, the ancillary electrical connections and devices used to supply power to the heater can be made smaller and/or denser, and/or allowed to supply lower power levels, which may further facilitate device scaling and/or increase device reliability.

[0021] Reference will now be made to the Figures in which like numbers refer to like parts throughout.

[0022] Figures 1 – 9 illustrate a process flow for forming an integrated circuit with pillars, according to some embodiments. For all of Figures 1 – 9, the center illustration is a cross-sectional top-down view, the left-most illustration is a view of a cross-section taken

along the Y-axis shown in the top-down view, and the right-most illustration is a cross-section taken along the X-axis shown in the top-down view.

[0023] With reference to Figure 1, schematic, cross-sectional side and top-down views of a partially fabricated integrated circuit are shown. The partially fabricated integrated circuit includes a substrate 100, which may have various constituent features. For example, the substrate 100 may include a vertically extending structure 110, which may be formed of conductive material and may be an electrode in some embodiments. Examples of conductive materials include metals, e.g., tungsten, and metal silicides, e.g., a cobalt silicide such as $CoSi_2$. Other electrodes may be formed above the electrode 110 and, consequently, the electrode 110 may be referred to as a lower electrode. The electrode 110 may be surrounded by dielectric material 120. The electrode 110 and dielectric material 120 may be disposed over various other structures (not shown), including, for example, underlying conductive interconnects. The illustrated substrate 100 may be part of a semiconductor wafer.

[0024] With reference to Figure 2, schematic, cross-sectional side and top-down views are shown of the partially fabricated integrated circuit of Figure 1 after forming mandrels on a first level and forming spacers along sidewalls of the mandrels. It will be appreciated that mandrels 130 may serve as placeholders to set the position of spacers 140. While a plurality of mandrels 130 may be provided across the substrate 100, a single mandrel 130 is shown for ease of illustration and discussion. Mandrel 130 may be formed by forming, e.g., depositing, a layer of mandrel material over the substrate 100 and patterning that layer of mandrel material. The layer of mandrel material may be patterned by various methods, including photolithography. For example, a photoresist layer may be deposited over the layer of mandrel material, a pattern may be formed in the photoresist layer by photolithography, and that pattern may subsequently be transferred to the layer of mandrel material to form the illustrated mandrel 130.

[0025] It will be appreciated that the mandrel 130 may be part of the final integrated circuit structure and, as a result, the material forming the mandrels 130 may be chosen by considering the properties desired for the mandrel 130 in that final structure. For example, the mandrel 130 may be a dielectric material to provide electrical isolation of later-

formed features. Examples of dielectric materials include oxides or nitrides, for example silicon oxide or silicon nitride. In some embodiments, the dielectric material is a silicon oxide.

[0026] With continued reference to Figure 2, spacers 140 having a width t1 may be formed along sidewalls of the mandrels 130. In some embodiments, the spacers 140 may be formed by blanket depositing a layer of spacer material over the mandrels 130 and substrate 100. The layer of spacer material may be deposited by various deposition processes, including vapor deposition processes, such as chemical vapor deposition (CVD) and atomic layer deposition (ALD). The spacer layer may be etched using a directional etch, thereby preferentially removing horizontally extending expanses of material to leave spacers 140 at the sides (e.g, contacting) the mandrel 130. Consequently, in some embodiments, the thickness of the spacer layer determines the width t1 of the spacers 140, with the thickness of the layer being substantially equal to the width t1. In some embodiments, the spacer 140 may function as electrode contacts in the final integrated circuit structure. In some other embodiments, the spacer 140 may be formed of a material that allows it to function as a switch, e.g., an ovonic threshold switch (OTS), in the final integrated circuit structure. Examples of materials for forming the spacers 140 to provide OTS functionality include compounds formed of the following combinations of elements: As-Te-I, $TiAsSe_2$, $TiAsTe_2$, Si-Te-As-Ge, Si-Te-As-Ge-P, Al-As-Te, Al-Ge-As-Te, $Te_{39}As_{36}Si_{17}Ge_7P$, $As_{40}Te_{(60-x)}In_x$ (where $5<x<16.5$), $As_{35}Te_{(65-x)}In_x$ (where $12.5<x<21.5$), $As_{30}Te_{(70-x)}$ (where $12.5<x<21.5$), and $Ge_{20}Te_{(80-x)}Pb_x$ (where $2<x<8$).

[0027] As noted herein, in some embodiments, ALD may be used to deposit exceptionally thin and uniform layers of spacer material, thereby forming exceptionally narrow spacers. In some embodiments, the spacers 140 can have a width t1 of about 40 nm or less, about 25 nm or less, about 10 nm or less, or about 5 nm or less. In some embodiments, the width t1 may be about 2 nm or less. In some embodiments, the spacer layer can have low non-uniformity. For example, the thickness non-uniformity may be about 5% or less, about 2%, about 1% or less, or about 0.5% or less. Examples of spacer materials include Al_2O_3, HfO_2, ZrO_2, Ta_2O_5, La_2O_3, TiO_2, V_2O_5, TiN, ZrN, CrN, TiAlN, AlTiN, Ru, Pd, Ir, Pt, Rh, Co, Cu, Fe, and Ni.

[0028] With reference to Figure 3, cross-sectional side and top-down views are shown of the partially fabricated integrated circuit of Figure 2 after filling gaps 150 at sides of the spacers 140. It will be appreciated that the features in the cross-sectional views shown in Figure 3 and in the other figures may be repeated across the substrate 100, such that gaps 150 are defined between the spacers 140 and a neighboring spacer and mandrel (not shown). In some embodiments, the gaps 150 may be filled by forming, e.g., depositing, filler material 160 into the gaps 150. The deposited filler material 160 may overfill the gaps 150, and then be planarized. In some embodiments, planarization may include removing material forming peaks on the upper surface of the partially fabricated integrated circuit, e.g., by performing a chemical mechanical polishing (CMP) process to remove excess filler material 160 and/or other material on the upper surface.

[0029] The volume occupied by the spacers 140 between the filler material 160 and the mandrels 130 may be referred to as a spacer volume. The spacers 140 may then be selectively recessed to form an opening, e.g. a trench, in the spacer volume, thereby providing a spacer volume that is partially open.

[0030] With reference to Figure 4, schematic, cross-sectional side and top-down views are shown of the partially fabricated integrated circuit of Figure 3 after recessing spacers 140 to form an open spacer volume and forming, e.g., depositing, a material 170 in the open spacer volume. It will be appreciated that the open spacer volume may be filled with the material 170, e.g., a dielectric material, which may then be planarized, e.g., by CMP. Examples of dielectric materials include oxides and nitrides, such as silicon oxide or silicon nitride. In some embodiments, the dielectric material is a silicon nitride.

[0031] With reference to Figure 5, schematic, cross-sectional side and top-down views are shown of the partially fabricated integrated circuit of Figure 4 after forming mandrels 230 on a second level and forming spacers 240 along sidewalls of the mandrels 230. The spacers 240 have a width t2. The mandrels 230 and spacers 240 may be formed by processes and using materials such as those discussed herein with respect to mandrels 130 and spacers 140 (Figure 2), respectively. For example, the spacers 240 may be formed by blanket depositing a layer of spacer material and then directionally etching that layer to form the spacers 240. The thickness of the layer of spacer material may determine the width t2. In

some embodiments, the width t2 may be about 40 nm or less, about 25 nm or less, about 10 nm or less, or about 5 nm or less. As seen in the center top-down view, the spacers 240 may extend along an axis crossing the axis along which the spacers 140 extend and the points of intersection of the crossing axes may be vertically aligned with the underlying electrodes 110. As illustrated, in some embodiments, as seen in a top-down view, the spacers 240 may extend substantially perpendicular to the spacers 140. The spacers 240 may be formed directly over and in contact with the underlying material 170.

[0032] After forming the spacers 240, gaps 250 may be present at their sides. It will be appreciated that the features in the cross-sectional views shown in Figure 5 may be repeated across the substrate 100, such that the gaps 250 are defined between the spacers 240 and a neighboring spacer and mandrel (not shown). In some embodiments, the gaps 250 may be filled by forming, e.g., depositing, filler material 260, which may overfill the gaps 250, and then planarizing the upper surface of the resulting structure. In some embodiments, planarization may include removing material forming peaks on the upper surface, e.g., by performing a chemical mechanical polishing (CMP) process to remove excess filler material and/or other material on the upper surface. Figure 6 shows schematic, cross-sectional side and top-down views of the partially fabricated integrated circuit of Figure 5 after filling gaps at sides of the spacers on the second level and planarizing the exposed upper surface.

[0033] The spacers 240 may subsequently be selectively removed to form trenches in the volume formerly occupied by the spacers 240 between the mandrels 230 and filler 260. The trenches expose portions of the underlying material 170 (Figure 4) filling the spacer volume in the first level. This exposed material 170 may be selectively removed. Figure 7 shows schematic, cross-sectional side and top-down views of the partially fabricated integrated circuit of Figure 6 after removing the spacers 240 on the second level and removing exposed material 170 in the spacer volume on the first level, thereby forming an opening 262 (e.g., trench) on the second level, which extends downwards to form an open volume on the first level. That open volume may then be filled with material and the corresponding filled volume may be referred to as the volume 264, which may take the form of a vertically elongated volume or channel. The spacers 240 (Figure 6) and exposed material 170 may be removed by exposure to one or more etches. In some embodiments, a

wet etch may be used to selectively remove the spacers 240 and a directional etch may be used to selectively remove exposed material 170. In some other embodiments, a single directional etch may be used to remove the spacers 240 and exposed material 170, depending upon whether the single directional etch provides sufficient selectivity for etching both those features. As shown in Figure 7's top-down view, the narrow volume 264 may be defined at the intersection of the spacers 240 (Figure 6) and exposed material 170.

[0034] In some embodiments, the etch processes use to form the volume 264 can provide a volume with more uniform sidewalls than those formed by photolithography. For example, the edge roughness of the sidewalls may be less than 3 nm, less than about 2 nm, or less than about 1 nm.

[0035] Figure 8 shows schematic, cross-sectional side and top-down views of the partially fabricated integrated circuit of Figure 7 after forming, e.g., depositing, material 270 in the open volume 262 (Figure 7) on the second level. As illustrated, the material 270 may also extend into the narrow volume 264 (Figure 7) on the first level. In some embodiments, the material 270 may be a material which provides a desired electrical functionality in the narrow volume 264. In some embodiments, the material 270 is a material that may exist stably in one or more states. For example, the material 270 may be a phase change material. Examples of phase change materials include chalcogenide materials, such as those formed from germanium (Ge), antimony (Sb), and tellurium (Te), and various combinations thereof. Examples of materials include binary compounds with one or more of these elements (e.g., GeTe, Ge-Sb, In-Se, Sb-Te, Ge-Sb, Ga-Sb, In-Sb, As-Te, and Al-Te); ternary compounds with one or more of these elements (e.g., Ge-Sb-Te, Te-Ge-As, In-Sb-Te, Te-Sn-Se, Ge-Se-Ga, Bi-Se-Sb, Ga-Se-Te, Sn-Sb-Te, and In-Sb-Ge); and quaternary compounds with one or more of these elements (e.g., Te-Ge-Sb-S, Te-Ge-Sn-O, Te-Ge-Sn-Au, Pd-Te-Ge-Sn, In-Se-Ti-Co, Ge-Sb-Te-Pd, Ge-Sb-Te-Co, Sb-Te-Bi-Se, Ag-In-Sb-Te, Ge-Sb-Se-Te, Ge-Sn-Sb-Te, Ge-Te-Sn-Ni, Ge-Te-Sn-Pd, and Ge-Te-Sn-Pt). It will be appreciated that the ratios of the various elements are not listed in the examples above and may be varied to achieve phase change behavior with multiple stable states. An example of a phase change material is $Ge_2Sb_2Te_5$. In some embodiments, the phase change material 270 is deposited such that it

overflows the volume 264 and excess material may be removed, e.g., by CMP, so that it stays substantially completely within the volume 264.

[0036] With reference to Figure 9, an upper electrode 280 may be formed on a third level over the material 270 and the resulting structure may be masked to define free-standing, spaced-apart stacks 290; Figure 9 shows schematic, cross-sectional side and top-down views of the partially fabricated integrated circuit of Figure 8 after defining the free-standing stacks 290. The upper electrode 280 may be formed by blanket depositing a layer of conductive material. A mask may then be formed over the resulting structure and the mask may be patterned (e.g., by photolithography) to form a pattern corresponding the free-standing stacks 290. The layers of material that make up the free-standing stacks 290 are subsequently subjected to one or more directional etches selective for those materials, thereby defining the free-standing stacks 290. As illustrated, the conductive material 270 and 140 take the form of plates after the free-standing stacks 290 are formed. As also illustrated, these plates may be elongated along crossing axes.

[0037] In some embodiments, a dielectric material may be deposited between the stacks 290 to electrically isolate those stacks from one another. In some embodiments, the dielectric material between the stacks 290 is the same material as the dielectric material 170. In some other embodiments, the dielectric material between the stacks 290 is different from the dielectric material 170.

[0038] It will be appreciated that each of the free-standing stacks 290 may constitute a memory cell 290. Figure 10 shows a schematic, perspective view of the memory cell 290. The memory cell 290 may be a phase change memory cell in which the material 270 is a phase change material. One of the top or bottom electrodes 280, 110 may provide current to the cell 290, while the other electrode 280, 110 provides a drain. The phase change material 270 and spacer 140 on the second and first levels, respectively, provide electrical contacts to the top and bottom electrodes 280, 110, respectively. Current passing through the material 270 in the relatively small volume 264 can cause resistive or joule heating, which may heat and change the state of portion 270a of the phase change material 270 in the narrow volume 264. As noted herein, the state may be selected based upon the amount of energy (and resulting heat) applied to the material in the volume 264. It will be appreciated that, in

some embodiments, other materials, e.g., adhesion layers, may be disposed between various materials in the stack 290, e.g., between the phase change material 270 and the top electrode 280.

[0039] In some other embodiments, a separate heater may be used to heat the phase change material 270. For example, the spacers 140 may be formed of a material with electrical resistivity sufficient to heat and to change the state of the phase change material 270. Examples of materials for such a heater include W, Ni, Pt, TiN, TiW, TaN, TaSiN, TiSiN, and NbN. These materials may be originally-deposited during formation of the spacers 140, or may be deposited into the spacer volume after removing the originally-formed spacers.

[0040] Figure 11 shows a cross-sectional top-down view the memory cell of Figure 10. As noted herein, the narrow volume 264 is defined at the intersection of the spacers 140 and 240, which each define a spacer volume into which other materials 170, 270 may be deposited. Thus, those other materials may then serve to set the dimensions of the openings 264. For example, as illustrated in Figure 11, the widths of the narrow volume 264 are defined by the intersection of the material 170 (e.g., a dielectric material) filling the spacer volume on the first level, and the material 270 (e.g., a phase change material) filling the spacer volume on the second level. Consequently, the cross-sectional dimensions of the volume 264 may be equal to the widths t1 and t2 of the spacer volumes on the first and second levels, respectively. Thus, the volume 264 and the material within it may extend substantially the entire width of the spacer volumes. For example, the volume 264 may extend the entire width of the laterally elongated region formed by the dielectric material 170. In some embodiments, as seen in a top-down view, the resulting volume 264 may substantially be in the shape of a parallelogram, including, for example, a rhomboid shape, examples of which include a rectangular or square shape. It will be appreciated that the corners of the shape may be rounded, e.g., because etches used in pattern formation may form rounded corners, while the general orientation of the sidewalls to one another may correspond substantially to the shape of a parallelogram and thus be said to be substantially to the shape of a parallelogram.

[0041] The memory cell 290 may form part of various devices utilizing memory. For example, the memory cell 290 may be used in personal computers, portable memory sticks, solid state drives (SSDs), digital cameras, cellular telephones, portable music players, movie players, and other electronic devices.

[0042] It will be appreciated that various processes and/or structures described herein may be omitted, repeated, combined with other processes or other altered. In some embodiments, one or both of the electrical contacts 140, 270 (Figure 10) may be omitted. This may be accomplished, for example, by removing all material above the level of the volume 264 after filling that volume. For example, phase change material 270 and other material above the top of the volume 264 may be removed by CMP after forming the structure of Figure 8. The lower electrical contact 140 may be omitted by completely removing the spacer 140 after forming the structure of Figure 3.

[0043] In some other embodiments, the processing involved with forming the particular structures of Figure 4 may be omitted. For example, after forming the structure of Figure 3, spacers 240 (Figure 5) may be formed directly over that illustrated structure and the volume 264 may be formed by removing the spacer 240 and the part of the spacer 140 exposed by the removal of the spacer 240. Material (e.g., phase change material) may then be deposited into the resulting open volume.

[0044] It will be appreciated that where conductive material fills the narrow openings 264, the filler in the opening may be referred to as a conductive line or wire. While discussed with reference to phase change memories and materials, the openings 264 may be filled with other materials. For example, other conductive materials may fill the openings 264 to form electrical fuses, resistive switching memory (e.g., RRAM), or other structures benefitting from thin wire structures.

[0045] It will be understood that the invention can take the form of various embodiments, some of which are discussed above and below.

[0046] In some embodiments, a method of forming an integrated circuit includes forming a first level mandrel on a first level over a substrate. A first set of spacers is formed along sidewalls of the first level mandrel. A first level filler material is deposited at sides of spacers of the first set of spacers, the first level filler material and the first level mandrels

defining a first level spacer volume therebetween. A second level mandrel on a second level is formed above the first level mandrel and the first level spacer volume, the second level mandrel crossing a width of the first level mandrel. A second set of spacers is formed along sidewalls of the second level mandrel. A second level filler material is deposited at sides of spacers of the second set of spacers. The second set of spacers is selectively removed to expose portions of the first level spacer volume. The exposed material in the first level spacer volume is selectively removed to form openings on the first level. The openings are filled and an upper electrode is formed on a third level over the second level, the upper electrode extending directly over one or more of the filled openings on the first level.

[0047] In some embodiments, filling the opening comprises forming a phase change material in the opening. Selectively removing the second set of spacers may define trenches between the second level mandrels and the second level filler material, wherein filling the openings also fills the trenches with phase change material. The method may further comprise removing the phase change material outside of the openings before forming the top electrode. The top electrode may electrically contact the phase change material filling the trenches and phase change material forms a part of a phase change memory cell. The method may further comprise providing a bottom electrode underlying the first set of spacers, wherein the first set of spacers are formed of a conductor and electrically interconnect the phase change material in the openings to the bottom electrodes.

[0048] In some embodiments, the method may further comprise recessing spacers of the first set of spacers after forming the first level filler material and before forming the second level mandrel, thereby defining trenches in the first level spacer volume; and forming a dielectric material in the trenches, wherein selectively removing the exposed material removes portions of the dielectric material.

[0049] In some embodiments, forming the first set or second set of spacers comprises: blanket depositing a layer of spacer material on the first or the second level mandrel; and subjecting the layer of spacer material to a directional etch to define the first or second set of spacers.

[0050] In some other embodiments, a method for forming an integrated circuit includes providing a first set of spaced-apart lines of sacrificial material separated by

dielectric material. A second set of spaced-apart lines of sacrificial material separated by dielectric material is provided, the second set of spaced-apart lines crossing and contacting tops of lines of the first set of spaced apart lines. The second set of spaced-apart lines and the portions of the first set of spaced-apart lines at the intersection of the first and second sets of spaced apart lines are selectively removed. An electrode is formed over a remainder of the first set of spaced apart lines.

[0051] In some embodiments, the integrated circuit is a phase change memory and selectively removing the second set of spaced-apart lines and the portions of the first set of spaced-apart lines may define openings at the intersection of the first and second sets of spaced apart lines, and the method further comprises: filling the openings with a phase change material. The method may further comprise, after filling the openings, etching material around the opening to define free-standing memory cell stacks separated by open space, wherein each stack comprises an opening filled with the phase change material. The method may further comprise, depositing dielectric material in the space separating the stacks. The dielectric material in the space separating the stacks may be different from dielectric material separating the first set of spaced-apart lines of sacrificial material.

[0052] In yet other embodiments, an integrated circuit includes a memory cell. The memory cell includes a bottom electrode; an upper electrode; and a conductive line in a channel extending vertically between the bottom and upper electrodes. The conductive line has a cross-section substantially in the shape of a parallelogram as seen in a top down view. Each side of the parallelogram may have a length of about 40 nm or less.

[0053] In some embodiments, a width of the conductive line, as seen from a top down view, is defined by a width of a spacer volume. The length may be about 25 nm or less in some embodiments. The line edge roughness may be about 3 nm or less. In some embodiments, the integrated circuit may further comprise a phase change material disposed in the channel and extending between the conductive line and the upper electrode. The conductive line may comprise a resistive heater. The resistive heater may include a material chosen from the group consisting of W, Ni, Pt, TiN, TiW, TaN, and NbN. In some embodiments, the cross-section may be substantially in the shape of a square.

[0054] In other embodiments, an integrated circuit includes a memory cell. The memory cell has a bottom electrode; an upper electrode; and a conductive wire extending vertically between the bottom and upper electrode. The conductive wire is disposed within a discrete, laterally elongated insulating region. The conductive wire extends across an entire width of the insulating region.

[0055] In some embodiments, a cross-section of the insulating region may have a parallelogram shape as seen in a top down view. In some embodiments, the conductive wire may be at least partly formed of phase change material.

[0056] In yet other embodiments, a memory device includes a memory cell. The memory cell includes a lower electrode; a vertically-extending lower conductive plate above and electrically connected to the lower electrode; a vertically-extending conductive wire above and electrically connected to the lower conductive plate; a vertically-extending upper conductive plate above and electrically connected to the wire; and an upper electrode above and electrically connected to the vertically-extending second conductive plate. The upper and lower conductive plates are elongated into crossing directions. In some embodiments, the conductive wire may comprise a phase change material.

[0057] Accordingly, although certain embodiments are described herein, other embodiments that are apparent to those of ordinary skill in the art, including embodiments that do not provide all of the features and/or advantages set forth herein, are also encompassed by this invention. Accordingly, the scope of the present invention is defined only by reference to the appended claims.

CLAIMS

1. A method of forming an integrated circuit, comprising:

forming a first level sacrificial structure on a first level over a substrate;

forming a first set of spacers along sidewalls of the first level sacrificial structure;

forming a first level filler material at sides of spacers of the first set of spacers, the first level filler material and the first level sacrificial structures defining a first level spacer volume therebetween;

forming a second level sacrificial structure on a second level above the first level sacrificial structure and the first level spacer volume, the second level sacrificial structure crossing a width of the first level sacrificial structure;

forming a second set of spacers along sidewalls of the second level sacrificial structure;

forming a second level filler material at sides of spacers of the second set of spacers;

selectively removing the second set of spacers to expose portions of the first level spacer volume;

selectively removing the exposed material in the first level spacer volume to form openings on the first level;

filling the openings; and

forming a top electrode on a third level over the second level, the electrode extending directly over one or more of the filled openings on the first level.

2. The method of Claim 1, wherein filling the opening comprises forming a phase change material in the opening.

3. The method of Claim 2, wherein selectively removing the second set of spacers defines trenches between the second level sacrificial structures and the second level filler material, wherein filling the openings also fills the trenches with phase change material.

4. The method of Claim 3, further comprising removing the phase change material outside of the openings before forming the top electrode.

5. The method of Claim 3, wherein the top electrode electrically contacts the phase change material filling the trenches and phase change material forms a part of a phase change memory cell.

6. The method of Claim 2, further comprising providing a bottom electrode underlying the first set of spacers, wherein the first set of spacers are formed of a conductor and electrically interconnect the phase change material in the openings to the bottom electrodes.

7. The method of Claim 1, further comprising:

recessing spacers of the first set of spacers after forming the first level filler material and before forming the second level sacrificial structure, thereby defining trenches in the first level spacer volume; and

forming a dielectric material in the trenches,

wherein selectively removing the exposed material removes portions of the dielectric material.

8. The method of Claim 1, wherein forming the first set or second set of spacers comprises:

blanket depositing a layer of spacer material on the first or the second level sacrificial structure; and

subjecting the layer of spacer material to a directional etch to define the first or second set of spacers.

9. A method for forming an integrated circuit, comprising:

providing a first set of spaced-apart lines of sacrificial material separated by dielectric material;

providing a second set of spaced-apart lines of sacrificial material separated by dielectric material, the second set of spaced-apart lines crossing and contacting tops of the first set of spaced apart lines;

selectively removing the second set of spaced-apart lines and portions of the first set of spaced-apart lines at the intersection of the first and second sets of spaced apart lines; and

forming an electrode over a remainder of the first set of spaced apart lines.

10. The method of Claim 9, wherein the integrated circuit is a phase change memory and wherein selectively removing the second set of spaced-apart lines and the portions of the first set of spaced-apart lines defines openings at the intersection of the first and second sets of spaced apart lines, further comprising:

filling the openings with a phase change material.

11. The method of Claim 10, further comprising, after filling the openings, etching material around the opening to define free-standing memory cell stacks separated by open space, wherein each stack comprises an opening filled with the phase change material.

12. The method of Claim 11, further comprising depositing dielectric material in the space separating the stacks.

13. The method of Claim 12, wherein the dielectric material in the space separating the stacks is different from dielectric material separating the first set of spaced-apart lines of sacrificial material.

14. An integrated circuit, comprising:

a memory cell, comprising:

a bottom electrode associated with a first set of spaced-apart lines of sacrificial material that interconnect with the bottom electrode;

an upper electrode associated with a second set of spaced-apart lines of sacrificial material, wherein the second set of spaced-apart lines cross and contact a portion of the first set of spaced-apart lines; and

a conductive line in a channel extending vertically between the bottom and upper electrodes,

the conductive line having a cross-section including a remainder portion of the first set of spaced-apart lines present after a removal of the second set of spaced-apart lines and a removed portion of the first set of spaced-apart lines at the cross-section.

15. The integrated circuit of Claim 14, wherein a width of the conductive line, as seen from a top down view, is defined by a width of a spacer volume.

16. The integrated circuit of Claim 14, wherein the cross-section is substantially in a shape of a parallelogram, a side of the parallelogram having a length of about 25 nm or less.

17. The integrated circuit of Claim 14, wherein line edge roughness is about 3 nm or less.

18. The integrated circuit of Claim 14, further comprising a phase change material disposed in the channel and extending between the conductive line and the upper electrode.

19. The integrated circuit of Claim 18, wherein the conductive line comprises a resistive heater.

20. The integrated circuit of Claim 19, wherein the resistive heater includes a material chosen from the group consisting of W, Ni, Pt, TiN, TiW, TaN, TaSiN, TiSiN, and NbN.

21. The integrated circuit of Claim 14, wherein the cross-section is substantially in the shape of a square.

22. An integrated circuit, comprising:

a memory cell, comprising:

a bottom electrode;

an upper electrode; and

a conductive wire extending vertically between the bottom and upper electrodes, the conductive wire disposed within a discrete, laterally elongated insulating region, the conductive wire extending across an entire width of the insulating region,

wherein a cross-sectional area at a height of the conductive wire includes a remainder portion of a first set of spaced-apart lines associated with the bottom electrode, the remainder portion being present after a removal of a second set of spaced-apart lines associated with the upper electrode and a removed portion of the first set of spaced-apart lines at the height.

23. The integrated circuit of Claim 22, wherein a cross-section of the insulating region has a parallelogram shape as seen in a top down view.

24. The integrated circuit of Claim 22, wherein the conductive wire is at least partly formed of phase change material.

25. A memory device, comprising:

a memory cell, the memory cell comprising:

a lower electrode;

a vertically-extending lower conductive plate above and electrically connected to the lower electrode;

a vertically-extending conductive wire above and electrically connected to the lower conductive plate;

a vertically-extending upper conductive plate above and electrically connected to the wire; and

an upper electrode above and electrically connected to the vertically-extending upper conductive plate, the upper and lower conductive plates elongated into crossing directions,

wherein a cross-sectional area at a height of the conductive wire includes a remainder portion of a first set of spaced-apart lines associated with the bottom electrode, the remainder portion being present after a removal of a second set of spaced-apart lines

associated with the upper electrode and a removed portion of the first set of spaced-apart lines at the height.

26. The memory device of Claim 25, wherein the conductive wire comprises a phase change material.