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- (71) Applicant (*for all designated States except US*): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, M/S: RNB-4-150, Santa Clara, California 95052 (US).
- (72) Inventor; and  
(71) Applicant : LEE, Kyu Oh [KR/US]; 400 North Coronado #1076, Chandler, Arizona 85224 (US).
- (72) Inventors; and  
(75) Inventors/Applicants (*for US only*): HLAD, Mark S. [US/US]; 3131 South Kimberlee Way, Chandler, Arizona 85286 (US). SALAMA, Islam A. [US/US]; 4435 East Cherry Hills Drive, Chandler, Arizona 85249 (US). ROY, Mihir K. [IN/US]; 900 North Rural Road, #1079, Chandler, Arizona 85226 (US). WU, Tao [CN/US]; 971 East Beechnut Drive, Chandler, Arizona 85249 (US). LIU, Yueli [CN/US]; 2651 East Vermont Court, Gilbert, Arizona 85295 (US).
- (74) Agents: BERNADICOU, Michael A. et al.; Blakely, Sokoloff, Taylor & Zafinan LLP, 1279 Oakmead Parkway, Sunnyvale, California 94085-4040 (US).
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(54) Title: DEVICE PACKAGING WITH SUBSTRATES HAVING EMBEDDED LINES AND METAL DEFINED PADS

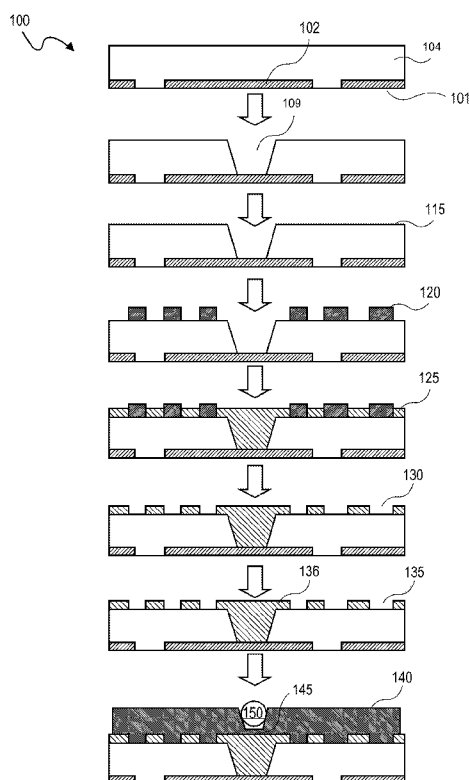


FIG. 1

(57) Abstract: Package substrates enabling reduced bump pitches and package assemblies thereof. Surface-level metal features are embedded in a surface-level dielectric layer with surface finish protruding from a top surface of the surface-level dielectric for assembly, without solder resist, to an IC chip having soldered connection points. Package substrates are fabricated to enable multiple levels of trace routing with each trace routing level capable of reduced minimum trace width and spacing.



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