SEMICONDUCTOR PACKAGES AND METHODS OF PACKAGING SEMICONDUCTOR DEVICES

BACKGROUND

[0001] Ball grid array (BGA) packages, thermal leadless array (TLA) packages and leadframe-based packages, such as high density leadframe array (HLA) packages, are popular packaging solutions for high I/O devices in the industry. However, existing BGA, TLA and leadframe-based packages suffer from several disadvantages. For example, BGA may offer high pin counts, however, the cost for producing BGA is relatively costly and the thermal performance of the BGA packages requires improvement. On the other hand, there is a need to increase the robustness and reliability of the TLA packages, for example, in terms of lead pull strength and die pad drop, etc. While leadframe-based packages, such as HLA, provide an economical alternative, the process for producing HLA packages is not easy and the package level reliability is limited.

[0002] From the foregoing discussion, there is a desire to provide an improved package having very thin package profile, higher I/O counts, fine pitch and flexible routings and with enhanced electrical and thermal performance. It is also desirable to provide simplified methods to produce a reliable package with relatively low cost and which can be flexibly customizable according to design requirements.

SUMMARY

[0003] Embodiments relate generally to semiconductor packages. In one embodiment, a method for forming a semiconductor package is disclosed. The method includes providing a package substrate having first and second major surfaces. The package substrate includes a base substrate having a mold material and a plurality of interconnect structures including via contacts extending through the first to the second major surface of the package substrate. A die having conductive contacts on its first or second surface is provided. The conductive contacts of the die

are electrically coupled to the interconnect structures. A cap is formed over the package substrate to encapsulate the die.

[0004] In another embodiment, a semiconductor package is presented. The semiconductor package includes a package substrate having first and second major surfaces. The package substrate includes a base substrate having a mold material and a plurality of interconnect structures including via contacts extending through the first to the second major surface of the package substrate. A die having conductive contacts on its first or second surfaces is disposed on the package substrate. The conductive contacts of the die are electrically coupled to the interconnect structures. A cap is disposed over the package substrate and encapsulates the die.

[0005] These embodiments, along with other advantages and features herein disclosed, will become apparent through reference to the following description and the accompanying drawings. Furthermore, it is to be understood that the features of the various embodiments described herein are not mutually exclusive and can exist in various combinations and permutations.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] In the drawings, like reference characters generally refer to the same parts throughout the different views. Also, the drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments of the present invention are described with reference to the following drawings, in which:

[0007] Figs. 1-3 show various embodiments of a semiconductor package;

[0008] Figs. 4-9 show various other embodiments of a semiconductor package;

[0009] Figs. 10a-j, Figs. 11a-d, Figs. 12a-f, Figs. 13a-f, Figs. 14a-e, Figs. 15a-h and Figs. 16a-g show various embodiments of a method for forming a semiconductor package; and

[0010] Figs. 17-18 show top views of a first surface of various embodiments of a package substrate.

DESCRIPTION

[0011] Embodiments relate to semiconductor packages and methods for forming a semiconductor package. The packages are used to package one or more semiconductor dies or chips. For the case of more than one die, the dies may be arranged in a planar arrangement, vertical arrangement, or a combination thereof. The dies, for example, may include memory devices, logic devices such as mixed signal logic devices, communication devices, RF devices, optoelectronic devices, digital signal processors (DSPs), microcontrollers, system-on-chips (SOCs) as well as other types of devices or a combination thereof. Such packages may be incorporated into electronic products or equipment, such as phones, computers as well as mobile and mobile smart products. Incorporating the packages into other types of products may also be useful.

[0012] Figs. 1-3 show simplified cross-sectional views of different embodiments of a semiconductor package. The semiconductor package 100, as shown in Fig. 1, includes a package substrate 101. The package substrate includes first and second major surfaces. The first major surface 103a, for example, may be referred to as the top surface and the second major surface 103b, for example, may be referred to as the bottom surface. Other designations for the surfaces may also be useful. In one embodiment, the first major surface of the package substrate includes first and second regions. The first region 105a, for example, is a die or chip region on which a die is mounted and the second region 105b, for example, is a non-die region. In one embodiment, the non-die region surrounds the die region. The die region, for example, may be disposed in a central portion of which the die is mounted and a non-die region which is outside of the die region. The die region, for example, may be concentrically disposed within the periphery of the package substrate. Other configurations of die and non-die regions may also be useful.

[0013] In one embodiment, the package substrate includes a base substrate 106 and a plurality of via contacts 107 extending from the first to the second major surface of the package substrate. In one embodiment, the base substrate includes a mold compound, such as molding epoxy resin material. The base substrate may be formed of other suitable types of substrate materials. The base substrate, for example, may be sufficiently thin or may include any suitable thickness, depending on manufacturing capabilities. The base substrate includes first and second major surfaces 106a-b, defining the first and second major surfaces of the package substrate. The base substrate, in one embodiment, is a patterned or predefined mold substrate having a plurality of cavities or vias 119 accommodating the plurality of via contacts.

[0014] The via contacts, in one embodiment, are formed of a single conductive material. For example, the via contacts may be formed of copper. Other suitable types of conductive materials may also be useful. The via contacts, in another embodiment, may be formed of two or more conductive materials, forming a multi-layered stack. The multi-layered stack, for example, may include copper, nickel, gold, silver, alloys, or a combination thereof. Other suitable types of conductive materials may also be useful. The via contacts may have tapered or straight profiles. The via contacts, for example, are held together and surrounded by the base substrate. The via contacts, as shown, are isolated from each other by the base substrate. It is understood that via contacts may also be disposed at the peripheries of the package substrate.

[0015] The via contacts include first and second surfaces 107a-b. The second surface 107b of the via contacts, in one embodiment, is substantially coplanar with the second surface 106b of the base substrate. In another embodiment, the second surface of the via contacts is non-coplanar with the second surface of the base substrate. For example, the second surface of the via contacts may be above or below the second surface of the base substrate.

[0016] In one embodiment, an adhesive 120 is disposed on the first surface 106a of the base substrate. The adhesive, for example, includes a UV sensitive laminate material or a thermal

sensitive laminate material. Other suitable types of adhesive material may also be used. The adhesive may be in different forms. For example, the adhesive may be a tape, a liquid or a paste.

[0017] In one embodiment, conductive traces 130 and connection pads 132 are disposed on the adhesive layer 120 over the base substrate and the first surface 107a of the via contacts. The conductive traces 130 and connection pads 132 are coupled to the via contacts forming interconnects of the package substrate which are coupled to die pads of a die. The conductive traces and connection pads, in one embodiment, are formed of the same conductive material as the via contacts, such as copper. In another embodiment, the conductive traces and connection pads may be formed of a different material than the via contacts. The conductive traces and connection pads, for example, may be formed of a monolithic conductive material. Other suitable types of conductive material may also be useful. The thickness of the conductive traces or connection pads, for example, may be as low as about 10μm. Other suitable thicknesses may also be useful.

[0018] An insulating layer 140 may optionally be disposed in between the conductive traces. The insulating layer, for example, isolates the conductive traces. The insulating layer, for example, includes a dielectric material such as a solder mask or inorganic insulating film material. Other suitable types of dielectric material may also be used.

[0019] In one embodiment, an adhesive layer 150 may be used to mount a die 110 to the package substrate. The die can be a semiconductor die or chip. The die includes first and second major surfaces. The first surface 110a, for example, is an inactive surface of the die and the second surface 110b is an active surface of the die. Other designations for the surfaces of the die may also be useful. The active surface, for example, includes openings (not shown) in a final passivation layer to expose conductive die pads/contacts (not shown). The surfaces of the die pads, for example, are substantially coplanar with the second major surface of the die. Providing surfaces of the conductive pads which are not coplanar with the second major surface of the die

may also be useful. The die pads provide connections to the circuitry of the die. The die pads, for example, are formed of a conductive material, such as copper, aluminum, gold, nickel or alloys thereof. Other types of conductive material may also be used for the die pads. The pattern of the die pads may be one or more rows disposed at the periphery of the active surface. Other pad patterns may also be useful.

[0020] The inactive surface of the die is mounted to the die region of the package substrate with the use of the adhesive layer 150. The adhesive layer, for example, may include an adhesive paste or die attach film, such as tape. Other types of adhesive, such as epoxy, may also be useful. In one embodiment, wire bonds 112 are provided to couple the die pads on the die to the conductive traces. The wire bonds create electrical connection between the conductive traces of the package substrate and die pads on the die.

[0021] In one embodiment, a cap 190 is disposed on top of the package substrate, encapsulating the die and the wire bonds. The cap serves to protect the die from the environment. For example, the cap may protect the die from moisture. The cap, for example, is formed of an encapsulation material. The encapsulation material, for example, may include molding epoxy resin material. Other suitable types of encapsulation materials may also be useful.

[0022] The cap includes first and second major surfaces 190a-b. The first surface 190a, for example, may be the top surface and the second surface 190b may be the bottom surface. Other designations for the surfaces of the cap may also be useful. In one embodiment, the cap surrounds and covers the die and the wire bonds. The bottom surface of the cap 190b, in one embodiment, may contact the conductive traces 130, connection pads 132, insulating layer 140 and the adhesive 120 of the package substrate. As shown in Fig. 1, the second surface of the cap is separated from the base substrate of the package substrate by the conductive traces 130, connection pads 132 and insulating layer 140.

[0023] Package contacts 160 are disposed on the second surface of the via contacts. The package contacts, for example, are spherical shaped structures or balls. The package contacts protrude from the bottom surface of the package substrate. Providing package contacts which do not protrude from the bottom surface of the package substrate, such as solder lands, may also be useful. The package contact is formed of a conductive material. The package contacts, for example, can be formed from solder. Various types of solder can be used to form the package contacts. For example, the solder can be a lead-based or non lead-based solder. Other types of conductive materials may also be used to form the package contacts.

[0024] The package contacts provide external access to the die via the conductive traces, via contacts and die pads. The package may be electrically coupled to an external device (not shown), such as a circuit board, by the package contacts.

[0025] Fig. 2 shows another embodiment of a semiconductor package 200. The semiconductor package 200 is similar to that described in Fig. 1. For example, the package substrate 101 includes a plurality of via contacts 107 held together and surrounded by the base substrate 106. An adhesive 120 is disposed on the first surface of the base substrate and package contacts 160 are disposed on the second surface 107b of the via contacts, similar to that described in Fig. 1. As such, common elements may not be described or described in detail.

[0026] In one embodiment, conductive traces 230 and connection pads 232 are disposed on the adhesive 120 over the base substrate and the first surface 107a of the via contacts. The conductive traces 230 and connection pads 232, in one embodiment, are formed of the same conductive material as the via contacts, such as copper. In another embodiment, the conductive traces and connection pads may be formed of a different material than the via contacts. The conductive traces and connection pads, for example, may be formed of a monolithic conductive material. Other suitable types of conductive material may also be useful. The thickness of the

conductive traces or connection pads, for example, may be as low as about 10μm. Other suitable thicknesses may also be useful.

[0027] In one embodiment, a flip chip 220 is mounted on the die region of the package substrate, as shown in Fig. 2. The flip chip, for example, includes inactive and active surfaces 220a-b. Die contacts 270 are disposed on the active surface 220b of the die. The connection pads 232, in one embodiment, are disposed in the die region of the package substrate. The connection pads 232, as shown, are configured to match the pattern of the die contacts of the flip chip. The conductive traces 230 and connection pads 232 thus couple the die contacts of the flip chip to the via contacts of the package substrate. The conductive traces and connection pads and the via contacts form interconnect structures of the package substrate. An underfill (not shown), such as an epoxy-based polymeric material, may be provided in the space between the die and package substrate. Alternatively, no underfill is provided between the die and package substrate.

[0028] In one embodiment, a cap 190 is disposed on top of the package substrate, encapsulating the flip chip. The cap serves to protect the flip chip from the environment. The cap, for example, is formed of an encapsulation material. The encapsulation material, for example, may include molding epoxy resin material. Other types of encapsulation materials may also be useful.

[0029] In one embodiment, the cap covers and surrounds the flip chip and the die contacts. The second surface 190b of the cap, in one embodiment, contacts the adhesive 120 on the base substrate 106 of the package substrate and/or the first surface 107a of the via contacts. As shown in Fig. 2, the second surface 190b of the cap is separated from the base substrate of the package substrate by the adhesive 120 on the base substrate.

[0030] In another embodiment, the cap surrounds the sides of the flip chip, leaving the inactive surface 220a of the flip chip exposed as shown in Fig. 3. As such, the first surface 190a of the cap is substantially coplanar with the inactive surface of the flip chip. By providing a cap

which does not cover the inactive surface of the die helps improves the heat dissipation from the die. External heat sink (not shown) may also be attached to the inactive surface of the die to further improve heat dissipation.

[0031] As described in the embodiments of Figs. 1-3, the second surface of the cap is separated from the base substrate of the package substrate by the adhesive and/or the conductive traces and connection pads. Moreover, as presented, the package substrate includes a plurality of via contacts held together and surrounded by the base substrate. As such, the via contacts will not be detached easily. This allows for improved robustness and reliability, such as enhanced lead pull strength, die pad drop, etc., relative to other types of packages, such as thermal leadless array (TLA). The use of molding material as the material for the base substrate also provides a cost saving solution relative to laminate base substrates. Furthermore, the second surface of the via contacts, in one embodiment, is disposed below or recessed with respect to the second surface of the base substrate. Such configuration is advantageous as it provides recesses or pockets for better receiving of package contacts. The package substrate, as described for example in Fig. 1, includes via contacts in the die and non-die regions. As such, the package substrate serves as fan-in and fan-out redistribution structure for the die contacts, enabling redistributed external package connections. The semiconductor package, as described in Fig. 3 may have improved thermal performance as the inactive surface of the flip is exposed for dissipating heat. Moreover, such configuration also allows for inclusion of additional heat sink or heat spreader to further enhance heat dissipation.

[0032] Figs. 4 and 5 show various other embodiments of a semiconductor package. The semiconductor packages 400-500 of Figs. 4 and 5 are similar to that described in Fig. 1. For example, the package substrate 101 includes a plurality of via contacts 107 held together and surrounded by the base substrate 106. An adhesive 120 is disposed on the first surface of the base substrate and package contacts 160 are disposed on the second surface 107b of the via

contacts, similar to that described in Fig. 1. As such, common elements may not be described or described in detail.

[0033] In one embodiment, the package substrate includes further interconnect level 170. The package substrate includes a plurality of conductive studs 172 or 272 over the via contacts as shown in Figs. 4 and 5. The conductive studs, for example, may be formed over the center of the via contacts. The studs, for example, may also be formed over the via contacts at regions other than the center region of the via contacts. In one embodiment, the conductive studs 272 include a single layer as shown in Fig. 5. The conductive studs 272, in one embodiment, include the same conductive material as the via contacts. For example, the conductive studs include a copper layer. Other suitable types of conductive material such as different than the material of the via contacts may also be useful. The width and thickness of the conductive studs 272 are smaller than or equal to the width and thickness of the via contacts. Other suitable widths and thicknesses may also be useful.

[0034] In another embodiment, the conductive studs 172 may be formed of two or more conductive materials, forming a multi-layered stack as shown in Fig. 4. The multi-layered stack, for example, may include copper, nickel or a combination thereof. Other types of conductive materials may also be useful. The multi-layered stack, for example, includes a first conductive layer 172_1 and a second conductive layer 172_2 below the first conductive layer. The multi-layered stack may include more than two layers. In one embodiment, the second conductive layer 172_2 contacts the via contacts. The second conductive layer 172_2, for example, includes a copper layer while the first conductive layer 172_1 includes a nickel layer. Other suitable types of conductive materials may also be useful. The width and thickness of the conductive studs 172 are smaller than or equal to the width and thickness of the via contacts. Other suitable widths and thicknesses may also be useful.

[0035] In one embodiment, the package substrate further includes an insulating layer 174 or 274 disposed over the adhesive 120 on the base substrate 106 and the first surface 107a of the via contacts, filling the spaces between the conductive studs 172 or 272 as shown in Figs. 4-5. The insulating layer 174 or 274 provides insulation between the conductive studs. In one embodiment, the insulating layer includes a dielectric material such as solder mask or inorganic insulating film. The insulating layer, in one embodiment, includes a material different than that of the base substrate. Other types of dielectric materials, such as the same as the material of the base substrate, may also be useful. As shown in Figs. 4-5, the insulating layer 174 or 274 is formed around the conductive studs 172 or 272. The thickness of the insulating layer 174 or 274, for example, may be substantially the same as or lesser than the thickness of the conductive studs 172 or 272.

[0036] In one embodiment, conductive traces 130 and connection pads 132 are disposed on the insulating layer 174 and top surfaces of the conductive studs. The conductive traces 130 or connection pads 132 may be extended from the side surfaces of the conductive studs 172 or 272. In cases where the conductive studs 172 include a multi-layered stack, the conductive traces 130 or connection pads 132 may extend from the two or more layers of the multi-layered stack of the conductive studs 172. The conductive traces 130 and connection pads 132, in one embodiment, are formed of the same material as the conductive studs, such as copper as shown in Fig. 5. Other types of conductive material, such as materials different than that of the conductive studs as shown in Fig. 4, may also be useful. The thickness of the conductive traces, for example, may be as low as about 10μm. In one embodiment, the conductive traces are electrically coupled to the conductive studs which are coupled to the via contacts forming interconnects of the package substrate as shown in Figs. 4-5.

[0037] A die 110 is mounted to the package substrate by an adhesive layer 150, similar to that described in Fig. 1. For example, wire bonds 112 are provided to couple the die pads on the

die to the conductive traces 130 at the non-die region of the package substrate which are coupled to the conductive studs 172 or 272 and to the via contacts 107 as shown in Figs. 4-5. As such, features of the die will not be described or described in detail.

[0038] In one embodiment, a cap 190 is formed over the insulating layer 174 or 274, encapsulating the die 110 and the wire bonds 112. In one embodiment, the cap surrounds and covers the die and the wire bonds. The second surface 190b of the cap, in one embodiment, contacts the insulating layer 174 or 274 and/or the conductive traces 130. As shown in Figs. 4-5, the second surface 190b of the cap is separated from the base substrate 106 of the package substrate by the adhesive 120 and the insulating layer 174 or 274.

[0039] Figs. 6-7 show various other embodiments of a semiconductor package. The semiconductor packages 600-700 are similar to that described in Figs. 4-5. As such, common elements may not be described or described in detail.

[0040] In one embodiment, conductive traces 230 and connection pads 232 are disposed on the insulating layer 174 or 274. The thickness of the conductive traces and connection pads, for example, is about 10μm. The conductive traces and connection pads are electrically coupled to the conductive studs 172 or 272 which are coupled to the via contacts 107 forming interconnects of the package substrate. The conductive traces and connection pads, in one embodiment, are disposed in the die region of the package substrate.

[0041] In one embodiment, a flip chip 220 similar to that described in Figs. 2-3 is mounted on the die region of the package substrate, as shown in Figs. 6-7. Die contacts 270, for example, are disposed on the active surface 220b of the die. The connection pads 232, as shown, are configured to match the pattern of the die contacts of the flip chip. The conductive traces 230 and connection pads 232 thus couple the die contacts 270 of the flip chip to the conductive studs 172 or 272 and to the via contacts 107 of the package substrate.

[0042] A cap 190 is formed over the insulating layer 174 or 274, encapsulating the flip chip. The cap serves to protect the flip chip from the environment. In one embodiment, the cap covers and surrounds the flip chip and the die contacts. The second surface of the cap 190b, in one embodiment, contacts the insulating layer 174 or 274 and/or the conductive traces 230 and connection pads 232. As shown in Figs. 6-7, the second surface 190b of the cap is separated from the base substrate of the package substrate by the insulating layer 174 or 274 and the adhesive 120 on the base substrate.

[0043] In another embodiment, the cap surrounds the sides of the flip chip, leaving inactive surface of the flip chip exposed (not shown). As such, the first surface 190a of the cap is coplanar with the top or inactive surface of the flip chip. External heat sink may also be attached to the inactive surface of the die to further improve heat dissipation.

[0044] The embodiments described with respect to Figs. 4-7 include some or all advantages as described with respect to Figs. 1-3. As such, these advantages will not be described or described in detail. The package substrate as described in the embodiments of Figs. 4-7 includes further interconnect level which includes conductive studs. The width of the conductive studs in one embodiment, as described, is smaller than the width of the via contacts. The conductive studs as described need not be formed at the center of the via contacts and its smaller width relative to the via contacts provide allowance for more traces, leading to more flexible and efficient routability of traces. Moreover, electrical resistance is lowered particularly where the interconnect structure of the package substrate, including the conductive traces, studs and via contacts, is formed of a single low electrical resistance material, such as copper. This further enhances the performance of the semiconductor packages.

[0045] Figs. 8-9 show various other embodiments of a semiconductor package. The semiconductor packages 800-900 are similar to that described in Figs. 1-3 and 4-7. As such, common elements may not be described or described in detail.

[0046] In one embodiment, the package substrate 301 includes a base substrate 306 and a plurality of via contacts 307 extending from the first to the second major surface of the package substrate. The base substrate 306, in one embodiment, includes a mold compound, such as molding epoxy resin material. The via contacts 307 are formed of a conductive material. For example, the via contacts may be formed of a monolithic conductive material. The conductive material, for example, includes copper. Other suitable types of conductive materials may also be useful. The via contacts 307 are held together and isolated from each other by the base substrate 306. Package contacts 160 are disposed on the second surface 307b of the conductive via contacts.

[0047] In one embodiment, via contacts 307 are disposed at the peripheries 301c-d of the package substrate. As shown in Figs. 8-9, side surfaces 307c-d of the conductive via contacts at the peripheries of the package substrate are exposed. In one embodiment, the first and second surfaces 307a-b of the via contacts and first and second surfaces 306a-b of the base substrate are substantially coplanar with each other. Providing first and second surfaces of the via contacts which are non-coplanar with first and second surfaces of the base substrate may also be useful.

[0048] In one embodiment, the package substrate includes further interconnect level. The package substrate includes a plurality of conductive studs 372 or 472 over and coupled to the via contacts 307 as shown in Figs. 8-9. The conductive studs 372 or 472, in one embodiment, are disposed in the die and non-die regions of the package substrate. The conductive studs 372 or 472, in one embodiment, may also be provided on the via contacts 307 at the periphery 301d of the package substrate. As such, side surfaces 372c or 472c of the conductive studs disposed over the via contacts at the periphery of the package substrate are exposed.

[0049] In one embodiment, the conductive studs 472 include a single layer as shown in Fig. 9. The conductive studs 472, in one embodiment, include the same conductive material of the via contacts. For example, the conductive studs include copper. Other suitable types of

conductive material such as different than the material of the via contacts may also be useful. The width and thickness of the conductive studs 472 are lesser than or equal to the width and thickness of the via contacts. Other suitable widths and thicknesses may also be useful.

[0050] In another embodiment, the conductive studs 372 may be formed of two or more conductive materials, forming a multi-layered stack as shown in Fig. 8. The multi-layered stack, for example, may include copper, nickel or a combination thereof. Other types of conductive materials may also be useful. The multi-layered stack, for example, includes a first conductive layer 372_1 and a second conductive layer 372_2 below the first conductive layer. The multi-layered stack may include more than two layers. In one embodiment, the second conductive layer 372_2 contacts the via contacts. The second conductive layer 372_2, for example, includes a nickel layer while the first conductive layer 372_1 includes a copper layer. Other suitable types of conductive materials may also be useful. The first and second conductive layers may include any suitable thicknesses and conductive materials, depending on the desired electrical properties to suit the required applications.

[0051] In one embodiment, the package substrate further includes an insulating layer 374 or 474 disposed over the top surfaces of the via contacts and the base substrate, filling the spaces between the conductive studs 372 or 472 as shown in Figs. 8-9. The insulating layer provides insulation between the conductive studs. In one embodiment, the insulating layer includes a dielectric material, such as solder mask or inorganic insulating film. The insulating layer, in one embodiment, includes a material different than that of the base substrate. Other types of dielectric materials may also be useful. As shown in Figs. 8-9, the insulating layer is formed around the conductive studs. The thickness of the insulating layer 374 or 474, for example, may be substantially the same as or lesser than the thickness of the conductive studs 372 or 472.

[0052] In one embodiment, conductive traces 130 and connection pads 132 are disposed on the insulation layer 374 or 474 as shown in Figs. 8-9. The conductive traces 130 or connection

pads 132 may be extended from the side surfaces of the conductive studs 372 or 472. In cases where the conductive studs 372 include a multi-layered stack, the conductive traces 130 or connection pads 132 may extend from the two or more layers of the multi-layered stack of the conductive studs 372. The conductive traces 130 and connection pads 132, in one embodiment, are formed of the same material as the conductive studs, such as copper. Other types of conductive material, such as materials different than that of the conductive studs, may also be useful. The thickness of the conductive traces, for example, may be as low as about 10μm. In one embodiment, the conductive traces 130 and the connection pads 132 are electrically coupled to the conductive studs 372 or 472 which are coupled to the via contacts 307 forming interconnects of the package substrate as shown in Figs. 8-9.

[0053] A die 110 is mounted to the package substrate by an adhesive layer 150, similar to that described in Fig. 1. For example, wire bonds 112 are provided to couple the die pads on the die to the conductive traces 130 at the non-die region of the package substrate which are coupled to the conductive studs 372 or 472 and to the via contacts 307 as shown in Figs. 8-9. As such, features of the die will not be described or described in detail.

[0054] In one embodiment, a cap 190 is formed over the insulating layer 374 or 474, encapsulating the die 110 and the wire bonds 112. In one embodiment, the cap surrounds and covers the die and the wire bonds. The second surface 190b of the cap, in one embodiment, contacts the insulating layer 374 or 474 and/or the conductive traces 130. As shown in Figs. 8-9, the second surface 190b of the cap is separated from the base substrate 306 of the package substrate by the insulating layer 374 or 474.

[0055] The semiconductor packages, as shown in Figs. 8-9, include a wire bonded die. In another embodiment, the semiconductor packages may include a flip chip die, similar to that described in Figs. 2-3 and 6-7. It is understood that modifications may be made to form

conductive bumps as already described for the flip chip applications. As such, common elements may not be described or described in detail.

[0056] The embodiments described with respect to Figs. 8-9 include some or all advantages as described with respect to Figs. 1-7. As such, these advantages will not be described or described in detail. The package substrate as described in the embodiments of Figs. 8-9 includes further advantages. For example, the interconnect structures of the package substrate, including the via contacts, conductive studs and conductive traces, are disposed at the peripheries of the package substrate. As such, side surfaces of the interconnect structures at the peripheries of the package substrate are exposed. Such configuration improves the thermal performance of the package.

[0057] The embodiments, as described in Figs. 1-9, show a semiconductor package having a wire bonded type of die or a flip chip type of die. It is understood that other suitable types of dies, such as TSV type of dies and microelectromechanical systems chips, may also be useful. The semiconductor packages, as illustrated in Figs. 1-9, include a single die. It is understood that the semiconductor package, may also include a die stack (not shown). The die stack includes x number of dies, where x is ≥ 2. In addition, it is understood that the dies of the die stack may be the same size or type. Providing a die stack having chips which are different types and/or sizes is also useful.

[0058] Figs. 10a-j show an embodiment of a method for forming a semiconductor package. A first mold chase 1201 and a second mold chase 1203 are provided as shown in Fig. 10a. The first mold chase, in one embodiment, includes a cavity 1205 while the second mold chase, in one embodiment, is prepared with a plurality of protrusions 1207 and cavities 1209 in between the protrusions. In another embodiment, the first mold chase is prepared with a plurality of protrusions and cavities in between the protrusions while the second mold chase includes a cavity. As shown in Fig. 10a, a plurality of protrusions are predefined on a first surface 1203a of

the second mold chase. The height of the protrusions may be varied, for example, depending on a desired thickness of a package substrate to be formed later. Other suitable dimensions for the height of the protrusion may also be useful. In one embodiment, the protrusions include straight sidewalls. In other embodiments, the protrusions may include tapered sidewalls. Providing other sidewall profiles for the protrusions may also be useful. The first and second mold chases, when assembled, form upper and lower cavities which define the shape of a base substrate of a package substrate to be formed later.

[0059] A substrate material is dispensed into the mold chase assembly, filling the spaces or cavities between the first and second mold chases to form a molded structure 1215. In one embodiment, the substrate material includes a mold compound, such as molding epoxy resin material. Providing other suitable types of substrate materials may also be useful. After molding, the molded structure 1215 is separated from the mold chases as shown in Fig. 10b. The molded structure, as shown, includes a base 1217 and a plurality of protruded portions 1206 with cavities or vias 1219 in between the protruded portions. The cavities may have tapered or straight profiles, depending on the sidewall profiles of the protrusions of the mold chase as discussed above. The size of the cavities may be varied, for example, depending on a desired size of via contacts to be formed later

[0060] The process continues to remove portions of the molded structure. In one embodiment, the base of the molded structure is removed, leaving the protruded portions as shown in Fig. 10c. The protruded portions of the molded structure after the thinning process may be referred to as the base substrate 106 of a package substrate. The base substrate, for example, is a patterned or predefined mold substrate having a plurality of cavities or vias 119 accommodating a plurality of via contacts. The base of the molded structure, in one embodiment, is removed by grinding. Other suitable techniques may also be used to thin the

molded structure to a suitable thickness, depending on the desired thickness of a package substrate.

[0061] In another embodiment, a temporary carrier (not shown) may optionally be provided. For example, the molded structure may optionally be attached to the temporary carrier during thinning of the molded structure in cases where the molded structure is thin. In cases where the molded structure is sufficiently thick, the temporary carrier is not needed during the thinning process. The temporary carrier, for example, should be sufficiently rigid to serve as a support during the removal or thinning process. By way of a non-limiting example, the temporary carrier may be a metal carrier. Various suitable types of materials may be used to form the temporary carrier.

[0062] In one embodiment, a conductive carrier 1230 is provided as shown in Fig. 10d. The conductive carrier, for example, serves as a base for forming via contacts in the cavities 119 of the base substrate while forming part of the interconnect structures of the package substrate. In one embodiment, the conductive carrier includes a copper carrier. In another embodiment, the conductive carrier may include a multi-layered metal carrier, such as NiAu. Other suitable types of conductive carrier may also be useful.

[0063] In one embodiment, an adhesive layer 1220 is provided on a first surface 1230a of the conductive carrier 1230 to facilitate attachment of the base substrate 106 to the conductive carrier. The adhesive layer, for example, includes a UV sensitive laminate material or thermal sensitive laminate material. The adhesive layer can be any type of adhesive that provides bonding of the base substrate to the first surface of the conductive carrier. The adhesive layer may be in different forms. For example, the adhesive layer may be a tape, a liquid or a paste. The adhesive layer may be provided on the conductive carrier using various techniques. The technique employed may depend on the type or form of the adhesive. For example, a tape adhesive may be provided on the conductive carrier by lamination, a paste adhesive may be

provided on the conductive carrier by printing while a liquid adhesive may be provided on the conductive carrier by spin-coating. Other suitable types of techniques may also be employed.

[0064] Referring to Fig. 10d, a first surface 106a of the base substrate, in one embodiment, is attached to the first surface 1230a of the conductive carrier with the use of the adhesive layer 1220 as described above. The base substrate is attached to the conductive carrier using any suitable techniques according to the equipment and the type of adhesive used.

[0065] In another embodiment, the conductive carrier 1230 prepared with the adhesive 1220 on its first surface 1230a as described above is provided immediately after forming the molded structure 1215 and prior to thinning the molded structure. In such situation, the molded structure is attached to the first surface of the conductive carrier with the use of the adhesive. Thinning process is performed to remove portions of the molded structure. As such, the conductive carrier may have sufficient thickness to also serve as a support carrier during thinning of the molded structure as well as serving as the base for forming via contacts in the cavities of the base substrate while forming part of the interconnect structures of the package substrate.

[0066] The process continues to remove exposed portions of the adhesive layer. In one embodiment, exposed portions of the adhesive layer may be removed by a patterning process. The patterning of the adhesive layer may be performed with the help of a patterned mask layer. Patterning of the adhesive layer can be achieved by any suitable etching techniques. For example, a patterned etch mask (not shown), such as a photoresist, is provided over the second surface 106b of the base substrate. Alternatively, the base substrate 106 may serve as an etch mask. An etch may be performed using the etch mask to remove portions of the adhesive layer unprotected by the etch mask. As shown in Fig. 10e, portions of the adhesive layer in the cavities 119 between the protruded portions of the base substrate are removed. As such, portions of the first surface of the conductive carrier in the cavities between the protruded portions are exposed. The etch, for example, may be wet etch or dry etch. Other suitable techniques may

also be employed to remove portions of the adhesive layer. The adhesive 120 which contacts the first surface 106a of the base substrate remains.

[0067] After patterning the adhesive layer, the mask is removed. The mask, for example, may be removed by ashing. Other techniques for removing the mask may also be useful.

[0068] Referring to Fig. 10f, the process continues to form via contacts 107 of the package substrate. As shown, the via contacts are formed in the cavities or vias 119 between the protruded portions. In one embodiment, the via contacts may be copper or copper alloy. The via contacts, in one embodiment, are formed by plating. For example, electrochemical or electroless plating may be employed to form the via contacts. The conductive carrier thus serves as the base or substrate for the electroplating process. The via contacts, in one embodiment, may be formed by a single plated layer. In other embodiments, the via contacts may be formed by multiple plated layers, forming a multi-layered stack via contacts. The multi-layered stack, for example, may include copper, nickel, gold, silver, alloys, or a combination thereof. Other suitable methods for forming the via contacts and suitable types of conductive materials, including plating materials, may also be useful. In some embodiments, seed layers may be used prior to forming the conductive via contacts.

[0069] The second surface 107b of the via contacts, in one embodiment, are substantially coplanar with the second surface 106b of the base substrate. In another embodiment, the second surface 107b of the via contacts are non-coplanar with the second surface of the base substrate as shown in Fig. 10f. For example, the second surface of the via contacts may be above or below the second surface of the base substrate. Providing the second surface of the via contacts below the second surface of the base substrate may be advantageous as such configuration provides recesses or pockets for better receiving of package contacts at a later processing stage.

[0070] The process continues to form conductive traces 130 and connection pads 132 of the package substrate as shown in Fig. 10g. In one embodiment, the conductive traces 130 and

connection pads 132 of the package substrate are formed by patterning the conductive carrier 1230. Patterning of the conductive carrier may be performed with the help of a patterned masked layer. Patterning of the conductive carrier can be achieved by any suitable etching techniques. For example, a patterned etch mask (not shown), such as photoresist, is provided over the second surface 1230b of the conductive carrier. An etch may be performed using the etch mask to remove portions of the conductive carrier unprotected by the etch mask. The etch, for example, may be an isotropic etch, such as a wet etch. An anisotropic etch, such as reactive ion etch (RIE) may be used. Other techniques for patterning the conductive carrier may also be useful. The thickness of the conductive traces 130 or connection pads 132, for example, is about 10μm. The conductive traces and connection pads, as shown, are coupled to the via contacts 107 to form interconnect structures of the package substrate.

[0071] After patterning the conductive carrier, the mask is removed. The mask, for example, may be removed by ashing. Other techniques for removing the mask may also be useful.

[0072] An insulating layer 140 may optionally be provided, covering and filling the spaces between the conductive traces 130 and connection pads 132 as shown in Fig. 10h. The insulating layer isolates the conductive traces and connection pads. In one embodiment, the insulating layer includes a dielectric material such as solder mask or inorganic insulating film. The insulating layer, for example, may be formed by molding or lamination technique. Other types of dielectric materials and techniques may also be useful for forming the insulating layer.

[0073] The package substrate 101 as formed includes a base substrate 106 having interconnect structures. The package substrate, as shown, includes interconnect structures having via contacts 107 and conductive traces 130 in a die region 105a and a non-die region 105b of the package substrate.

[0074] Referring to Fig. 10i, a die or a semiconductor chip 110 which includes circuit components is attached to the die region of the package substrate. The circuit components

include, for example, transistors, resistors, capacitors and interconnections to form an IC. A final passivation layer (not shown) may be formed over the die. The final passivation layer includes openings (not shown) to expose die pads/contacts (not shown). The surface of the die which includes the openings to the die pads may be referred to as the active surface 110b of the die. In one embodiment, an adhesive layer 150 may be used to mount the die to the die region of the package substrate. For example, the inactive surface 110a of the die is mounted to the package substrate with the use of the adhesive layer. The adhesive layer, for example, may include an adhesive paste or die attach film, such as tape. Other types of adhesive, such as epoxy, may also be useful. In one embodiment, wire bonds 112 are formed to create electrical connection between the conductive traces on the package substrate and die pads on the die.

[0075] Referring to Fig. 10i, a cap 190 is formed on the package substrate. For example, an encapsulation material is dispensed to encapsulate the die and the wire bonds. In one embodiment, the encapsulation material includes a mold compound, such as molding epoxy resin material. Providing other types of encapsulation materials may also be useful. The cap includes first and second major surfaces 190a-b. In one embodiment, the second surface 190b of the cap contacts the adhesive 120 over the base substrate 106 and/or the conductive traces 130. As shown, the second surface 190b of the cap is separated from the base substrate by the adhesive and/or the conductive traces.

[0076] The cap, in one embodiment, is formed by transfer molding techniques. Encapsulation material, such as a mold compound, is dispensed into the mold assembly to form the cap. After molding, the molded die is separated from the mold. Other suitable types of techniques for forming the cap may also be useful. For example, the cap may also be formed by printing or compression molding.

[0077] The process continues by forming package contacts 160 coupled to the via contacts 107, as shown in Fig. 10j. For example, the package contacts are formed on the second surface

107b of the via contacts. The package contacts, for example, may include spherical shaped structures or balls arranged in grid pattern to form a BGA type package. As such, a semiconductor package such as that shown in Fig. 1 is formed. The package contacts are formed of a conductive material. The package contacts, for example, can be formed from solder. Various types of solder can be used to form the package contacts. For example, the solder can be a lead-based or non lead-based solder.

[0078] In some embodiments, other types of package contacts are coupled to the via contacts. For example, the package contacts may include contacts which do not protrude from the bottom surface of the package substrate. Providing package contacts which do not protrude from the bottom surface of the package substrate, such as solder lands, may also be useful. The package contacts may be formed of materials other than solder or using other techniques.

[0079] The process as described with respect to Figs. 10a-j is suitable for wire bonded type of die or chip packages. The process may also be useful for other types of dies, including flip chip applications. Figs. 11a-d show another embodiment of a process for forming a semiconductor package. The process is similar to that described in Figs. 10a-j. As such, common elements may not be described or described in detail.

[0080] Referring to Fig. 11a, a partially processed package substrate is provided. The partially processed package substrate is at the stage of processing as described in Fig. 10f. For example, via contacts 107 of the package substrate are formed. The via contacts are formed in the cavities or vias between the protruded portions. The via contacts, in one embodiment, are formed by process and materials similar to that described in Fig. 10f. For example, the via contacts may include single or multiple plated layers. The via contacts as formed is similar to that as described in Fig. 10f. As such, the features of the via contacts will not be described or described in detail.

[0081] The process continues to form conductive traces 230 and connection pads 232 of the package substrate as shown in Fig. 11b. In one embodiment, the conductive traces 230 and connection pads 232 of the package substrate are formed by patterning the conductive carrier 1230. Patterning of the conductive carrier may be performed with the help of a patterned masked layer. Patterning of the conductive carrier can be achieved by any suitable etching techniques. For example, a patterned etch mask (not shown), such as photoresist, is provided over the conductive carrier. An etch may be performed using the etch mask to remove portions of the conductive carrier unprotected by the etch mask. The etch, for example, may be an isotropic etch, such as a wet etch. An anisotropic etch, such as reactive ion etch (RIE) may be used. Other techniques for patterning the conductive carrier may also be useful. The thickness of the conductive traces 230 or connection pads 232, for example, is about 10μm. The conductive traces and connection pads, as shown, are coupled to via contacts to form interconnect structures of the package substrate. The conductive carrier is patterned to form conductive traces and connection pads coupled to the via contacts in the package substrate and are coupled to the die contacts of a flip chip later.

[0082] After patterning the conductive carrier, the mask is removed. The mask, for example, may be removed by ashing. Other techniques for removing the mask may also be useful.

[0083] The package substrate as formed includes a base substrate 106 having interconnect structures. The package substrate, as shown, includes interconnect structures having via contacts 107 and conductive traces 230 in a die region and a non-die region of the package substrate.

[0084] Referring to Fig. 11c, a flip chip 220 having die contacts 270 on an active surface 220b of the die is mounted onto the die region 105a. The connection pads 232, in the case of a flip chip application, are disposed in the die region of the package substrate. The connection pads 232, as shown, are configured to match the pattern of the die contacts 270 of the flip chip. An underfill (not shown), such as an epoxy-based polymeric material, may be provided in the

space between the flip chip and the package substrate. Alternatively, no underfill is provided between the flip chip and the package substrate.

[0085] A cap 190 is formed on the package substrate. For example, an encapsulation material is dispensed to encapsulate the flip chip. For example, an encapsulation material is dispensed to fill the spaces between the die contacts and cover the inactive surface of the flip chip. In one embodiment, the encapsulation is a mold compound, such as molding epoxy resin material. Providing other types of encapsulation materials may also be useful.

[0086] The cap, in one embodiment, is formed by transfer molding techniques. Encapsulation material, such as a mold compound, is dispensed into the mold assembly, surrounding the sides and covering the inactive surface of the flip chip to form the cap as shown in Fig. 11d. After molding, the molded die is separated from the mold. Other suitable types of techniques for forming the cap may also be useful. For example, the cap may also be formed by printing or compression molding.

[0087] In another embodiment, the cap is formed by a film assisted transfer molding technique. For example, a film is placed against contours of a mold (not shown). In one embodiment, when the package substrate and the die are placed against the mold, the film contacts the inactive surface of the flip chip. The cap surrounds the sides of the flip chip, leaving the inactive surface of the flip chip exposed to form a semiconductor package similar to that shown in Fig. 3. As such, the first surface of the cap is substantially coplanar with the inactive surface of the flip chip. By providing a cap which does not cover the inactive surface of the die helps improves the heat dissipation from the die. External heat sink may also be attached to the inactive surface of the die to further improve heat dissipation.

[0088] The process continues by forming package contacts 160 coupled to the conductive via contacts, as shown in Fig. 11d. For example, the package contacts are formed on the second surface 107b of the via contacts of the package substrate, similar to that described in Fig. 10j. As

such, common features will not be described or described in detail. A semiconductor package such as that shown in Fig. 2 or 3 is formed.

[0089] The processes, as described with respect to Figs. 10a-j and Figs. 11a-d, result in advantages. For example, the via contacts, in one embodiment, are formed by plating. The use of plating technique provides flexibility in terms of controlling the height of the via contacts with respect to the surface of the base substrate. For example, the plating technique enables second surface of the via contacts to be substantially coplanar or non-coplanar, including protruding or recessed, with respect to the second surface of the base substrate. Providing the second surface of the via contacts which is disposed below or recessed with respect to the second surface of the base substrate is further advantageous as it provides recesses or pockets for better receiving of package contacts. Furthermore, the conductive traces, for example, are formed by an etch process. Etch process, for example, presents a relatively low cost solution for forming conductive traces relative to other techniques.

[0090] Moreover, as presented, the package substrate includes a plurality of via contacts held together and surrounded by the base substrate. As such, the via contacts will not be detached easily. This allows for improved robustness and reliability, such as enhanced lead pull strength, die pad drop, etc., relative to other types of packages, such as thermal leadless array (TLA). The package substrate as formed includes via contacts in the die and non-die regions. As such, the process enables formation of package substrate which serves as fan-in and fan-out redistribution structure for the die, enabling redistributed, fan-in and fan out external package connections. The semiconductor package, as described in an alternative embodiment of Fig. 11d, may have improved thermal performance as the inactive surface of the flip is exposed for dissipating heat. Moreover, such configuration also allows for inclusion of additional heat sink or heat spreader to further enhance heat dissipation.

[0091] Figs. 12a-f show another embodiment of a process for forming a semiconductor package. The process is similar to that described in Figs. 10a-j and Figs. 11a-d. Referring to Fig. 12a, a partially processed package substrate is provided. The partially processed package substrate is at the stage of processing as described in Fig. 10c. For example, portions of the molded structure are removed based on the techniques as already described or other suitable techniques, leaving the protruded portions. The protruded portions of the molded structure after the thinning process may be referred to as the base substrate 106 of a package substrate as described in Fig. 10c. The base substrate includes a plurality of cavities 119 as shown in Fig. 12a. As such, common elements may not be described or described in detail.

[0092] Referring to Fig. 12b, a conductive carrier or leadframe 1430 is provided. The conductive carrier, for example, may serve as part of the interconnect structures of the package substrate. The conductive carrier, in one embodiment, includes a multi-layered stack. In one embodiment, the conductive carrier includes first, second and third conductive layers. Providing other number of layers of conductive layer to form the multi-layered stack may also be useful.

[0093] In one embodiment, the first conductive layer 1431 includes a copper layer. The first conductive layer includes first and second major surfaces 1431a-b. The first conductive layer, for example, is sufficiently thick to support the structure. The second conductive layer 1433 having first and second major surfaces 1433a-b is provided over the first major surface 1431a of the first conductive layer 1431. The second conductive layer 1433, in one embodiment, includes a nickel layer. The third conductive layer 1435 having first and second major surfaces 1435a-b is formed over the first major surface 1433a of the second conductive layer. In one embodiment, the third conductive layer includes the same material as the first conductive layer. For example, the third conductive layer includes copper. Providing the third conductive layer with different material than the first conductive layer may also be useful. The second conductive layer, in one embodiment, includes different material than the third conductive layer. Any other suitable

types of materials may be used for the second conductive layer so long as it provides etch selectivity between the second and third conductive layers. Other suitable types of materials may also be used for the first, second and third conductive layers.

[0094] In one embodiment, the second and third conductive layers are formed by plating. For example, electrochemical or electroless plating may be employed to form the second and third conductive layers. The first conductive layer of the conductive carrier thus also serves as a base or substrate for the electroplating process for forming the second conductive layer while the second conductive layer serves as a base or substrate for the electroplating process for forming the third conductive layer. Other suitable types of techniques may also be employed for forming the second and third conductive layers. The second conductive layer, for example, is sufficiently thin if it is of high electrical resistance, such as nickel. Other suitable thicknesses may also be useful. The thickness of the third conductive layer, for example, may be varied to a desired thickness of conductive traces and connection pads to be formed later.

[0095] In one embodiment, an adhesive layer 1220 is provided on a first surface 1430a of the conductive carrier to facilitate attachment of the base substrate 106 to the conductive carrier. For example, an adhesive layer is provided over the second surface 1435a of the third conductive layer 1435. The adhesive layer, for example, includes a UV sensitive laminate material or thermal sensitive laminate material. Any other suitable types of adhesive material may also be used. The adhesive layer can be any type of adhesive that provides bonding of the base substrate to the first surface of the conductive carrier. The adhesive layer may be in different forms. For example, the adhesive layer may be a tape, a liquid or a paste. The adhesive layer may be provided on the conductive carrier using various techniques. The technique employed may depend on the type or form of the adhesive. For example, a tape adhesive may be provided on the conductive carrier by lamination, a paste adhesive may be provided on the conductive carrier

by printing while a liquid adhesive may be provided on the conductive carrier by spin-coating. Other suitable types of techniques may also be employed.

[0096] Referring to Fig. 12b, a first surface 106a of the base substrate, in one embodiment, is attached to the first surface 1430a of the conductive carrier with the use of the adhesive layer 1220 as described above. The base substrate is attached to the conductive carrier using any suitable techniques according to the equipment and the type of adhesive used.

[0097] The process continues to remove exposed portions of the adhesive layer 1220 as shown in Fig. 12c. In one embodiment, portions of the adhesive layer may be removed by a patterning process. The patterning of the adhesive layer may be performed with the help of a patterned mask layer. Patterning of the adhesive layer can be achieved by any suitable etching techniques. For example, a patterned etch mask (not shown), such as a photoresist, is provided over the second surface 106b of the base substrate. Alternatively, the base substrate 106 may be used as an etch mask. An etch may be performed using the etch mask to remove portions of the adhesive layer unprotected by the etch mask. As shown in Fig. 12c, portions of the adhesive layer in the cavities 119 between the protruded portions of the base substrate are removed. As such, portions of the first surface 1435a of the third conductive layer 1435 in the cavities between the protruded portions are exposed. The etch, for example, may be wet etch or dry etch. Other suitable techniques may also be employed to remove portions of the adhesive layer. The adhesive 120 which contacts the first surface 106a of the base substrate remains.

[0098] After patterning the adhesive layer, the mask is removed. The mask, for example, may be removed by ashing. Other techniques for removing the mask may also be useful.

[0099] Referring to Fig. 12d, the process continues to form via contacts 107 of the package substrate. As shown, the via contacts are formed in the cavities or vias 119 between the protruded portions. The via contacts, in one embodiment, are formed by process and materials similar to that described in Fig. 10f. For example, the via contacts may include single or

multiple plated layers. As such, the via contacts as formed are similar to that as described in Fig. 10f. As such, feature of the via contacts will not be described or described in detail.

[00100] The process continues by removing the first and second conductive layers 1431 and 1433 of the conductive carrier as shown in Fig. 12e. In one embodiment, the first and second conductive layers of the conductive carrier are removed by an etch process. The etch process, in one embodiment, includes a two-step etch process. The first etch, for example, removes the first conductive layer 1431. Thus, the second conductive layer serves as an etch stop or barrier layer during the removal of the first conductive layer. The second etch, for example, removes the second conductive layer 1433. Since the second and third conductive layers include different materials, the second etch stops on the second surface 1435b of the third conductive layer. As such, the third conductive layer will not be overetched during the removal of the second conductive layer. The etch process, such as chemistry and other parameters, may be tailored to selectively remove the desired material with respect to the other material. Other suitable types of techniques may also be employed to remove the first and second conductive layers.

[00101] In one embodiment, the process continues to form conductive traces 130 and connection pads 132 of the package substrate as shown in Fig. 12f$_i$. In one embodiment, the conductive traces and connection pads of the package substrate are formed by patterning the remaining third conductive layer 1435. Patterning of the third conductive layer may be performed with the help of a patterned masked layer. Patterning of the third conductive layer can be achieved by any suitable etching techniques. For example, a patterned etch mask (not shown), such as photoresist, is provided over the second surface 1435b of the third conductive layer. An etch may be performed using the etch mask to remove portions of the third conductive layer unprotected by the etch mask. The etch, for example, may be an isotropic etch, such as a wet etch. An anisotropic etch, such as reactive ion etch (RIE) may be used. Other techniques for patterning the third conductive layer may also be useful. As shown in Fig. 12f$_i$, the thickness of

the third conductive layer defines the thickness of the conductive traces and connection pads formed. The conductive traces and connection pads, as shown, are coupled to the via contacts 160 to form interconnect structures of the package substrate.

[00102] After patterning the third conductive layer, the mask is removed. The mask, for example, may be removed by ashing. Other techniques for removing the mask may also be useful.

[00103] An insulating layer may optionally be provided, covering and filling the spaces between conductive traces and connection pads, similar to that described in Fig. 10h. A die which includes circuit components similarly described in Fig. 10i is attached to the die region of the package substrate. The process continues, as similarly described in Fig. 10i and onwards. As such, these process steps will not be described or described in detail. The process continues until a package similar to that shown in Fig. 1 is formed.

[00104] In another embodiment, conductive traces 230 and connection pads 232 of the package substrate are formed after removing the first and second conductive layers 1431 and 1433 of the conductive carrier 1430 as shown in Fig. $12f_{ii}$. The conductive traces and connection pads of the package substrate, for example, are formed by patterning the third conductive layer 1435. Patterning of the third conductive layer is similar to that described with respect to Fig. 11b. As shown in Fig. $12f_{ii}$, the thickness of the third conductive layer defines the thickness of the conductive traces and connection pads formed. The connection pads formed in the die region of the package substrate, as shown, are coupled to via contacts to form interconnect structures of the package substrate. The third conductive layer is patterned to form conductive traces and connection pads coupled to the via contacts and are coupled to the die contacts of a flip chip later.

[00105] After forming the conductive traces and connection pads, a flip chip 220 having die contacts on an active surface of the die is mounted onto the die region, similar to that described

with respect to Fig. 11c. The process continues, as similarly described in Fig. 11c and onwards. As such, these process steps will not be described or described in detail. The process continues until a package similar to that shown in Fig. 2 or Fig. 3 is formed.

[00106] The embodiment described with respect to Figs. 12a-f includes some or all advantages as described with respect to Fig. 10a-j and Figs. 11a-d. As such, these advantages will not be described or described in detail. The embodiment, as described with respect to Figs. 12a-f results in additional advantages. The base substrate, as described are formed from using molding techniques. The thickness of the base substrate, for example, may be defined by the height of the protrusions on the mold chase. Thus, such method provides flexibility and allows base substrate or package substrate of various thicknesses to be formed.

[00107] In addition, the second and third conductive layers, such as nickel and copper layer, in one embodiment, are plated onto the first conductive layer to form the conductive carrier for better handling. For example, the second conductive layer, such as nickel, acts as a barrier during the removal of the first conductive layer. As such, the third conductive layer and the via contacts will not be overetched during the removal of the first conductive layer.

[00108] As described, the third conductive layer of the conductive carrier in Figs. 12a-f which is used for forming the conductive traces is formed by plating. This allows better control of the thickness of the conductive traces. For example, conductive traces with finer or thinner profile can be formed. The conductive traces having thinner profile requires a shorter etching time, resulting in easier process control and reduces the risk of over-etching into the via contacts. Moreover, the plating technique does not require tight control of the flatness of the carrier.

[00109] Figs. 13a-f show another embodiment of a process for forming a semiconductor package. The process is similar to that described in Figs. 10a-j, Figs. 11a-d and Figs. 12a-f. As such, common elements may not be described or described in detail.

[00110] Referring to Fig. 13a, a partially processed package substrate is provided. The partially processed package substrate is at the stage of processing as described in Fig. 12d. For example, conductive carrier 1430 is provided and via contacts 107 are formed in the cavities or vias 119 between the protruded portions. The conductive carrier is formed by process and materials as described in Fig. 12b while conductive via contacts, in one embodiment, are formed by process and materials similar to that described in Fig. 10f. As such, feature of the conductive carrier 1430 and via contacts 107 will not be described or described in detail.

[00111] Referring to Fig. 13b, the process continues by removing the first conductive layer 1431 of the conductive carrier 1430. In one embodiment, an etch process may be performed to remove the first conductive layer. Other techniques for removing the first conductive layer may also be useful. The etch, for example, removes the first conductive layer and stops at the second surface 1433b of the second conductive layer. As such, the second conductive layer serves as an etch stop layer.

[00112] In one embodiment, the process continues to form further interconnect level of the package substrate. The process continues to form conductive studs 172 over and couple to the via contacts as shown in Fig. 13c. In one embodiment, portions of the second and third conductive layers 1433 and 1435 are removed to form the conductive studs 172. In one embodiment, the second and third conductive layers of the conductive carrier 1430 are patterned to create a pattern which defines the conductive studs 172 with spaces 1519 in between the conductive studs as shown in Fig. 13c. The conductive studs, for example, may be formed over the center of the via contacts. Forming the conductive studs over regions other than the center of the via contacts may also be useful. Patterning of the second and third conductive layers of the conductive carrier may be performed with the help of a patterned masked layer. Patterning of the second and third conductive layers can be achieved by any suitable etching techniques. For example, a patterned etch mask (not shown), such as photoresist, is provided over the first

conductive layer 1431. A two-step etch process may be performed using the etch mask to remove portions of the second and third conductive layers unprotected by the etch mask. The first etch, for example, removes portions of the second conductive layer 1433 unprotected by the mask. Thus, the third conductive layer 1435 serves as an etch stop layer during the removal of the portions of the second conductive layer. The second etch, for example, removes portions of the third conductive layer 1435 unprotected by the mask. The second etch, for example, stops at the adhesive 120 on the base substrate. Other techniques for patterning the second and third conductive layers may also be useful.

[00113] The conductive studs as formed, in one embodiment, include a multi layered stack as shown in Fig. 13c. The width and thickness of the conductive studs as formed, for example, may be less than or equal to the width and thickness of the via contacts. Other suitable widths may also be useful. The thickness of the conductive studs, as shown, corresponds to the thickness of the second and third conductive layers of the conductive carrier.

[00114] An insulating layer 174 is provided, covering and filling the spaces between the conductive studs 172 as shown in Fig. 13d. The insulating layer provides insulation between the conductive studs. In one embodiment, the insulating layer includes a dielectric material such as solder mask or inorganic insulating film. The insulating layer, for example, may be formed by molding or lamination technique. Other types of dielectric materials and techniques for forming the insulation layer may also be useful. As shown in Fig. 13d, the insulation layer is formed around the conductive stud, exposing the first surface 172a of the conductive studs. The thickness of the insulating layer, for example, may be substantially the same as or lesser than the thickness of the conductive studs.

[00115] Referring to Fig. 13e, the process continues to form conductive traces 130 and connection pads 132. In one embodiment, the conductive traces and connection pads are formed of a material different than that of the conductive studs. Other types of conductive materials,

such as the same as the conductive studs, may also be useful. The conductive traces and connection pads, in one embodiment, are formed by plating. For example, electrochemical or electroless plating may be employed to form the conductive traces and connection pads. The first conductive layer of the conductive studs thus also serves as a base or substrate for the electroplating process. Other suitable methods for forming the conductive traces and connection pads may also be used. The thickness of the conductive traces or connection pads, for example, may be as low as about 10μ. As shown, the conductive traces are formed over the insulating layer 174 and top surfaces of the conductive studs in the die and non-die regions of the package substrate and are electrically coupled to the conductive studs 172. The conductive traces 130 may be extended from the side surfaces of the conductive studs 172. In cases where the conductive studs 172 include a multi-layered stack, the conductive traces 130 may extend from the two or more layers of the multi-layered stack of the conductive studs 172.

[00116] A die 110 which includes circuit components similarly described in Fig. 10i is attached by an adhesive layer 150 to the die region of the package substrate. The process continues, as similarly described in Fig. 10i and onwards. As such, these process steps will not be described or described in detail. The process continues until a package as shown in Fig. 13f$_i$ similar to that shown in Fig. 4 is formed.

[00117] In another embodiment, conductive traces 230 and connection pads 232 of the package substrate are formed after forming the insulating layer 174 as described in Fig. 13d. In one embodiment, the conductive traces and connection pads are formed of a material different than that of the conductive studs. Other types of conductive materials, such as the same as the conductive studs, may also be useful. The conductive traces and connection pads, in one embodiment, are formed by plating. For example, electrochemical or electroless plating may be employed to form the conductive traces and connection pads. The first conductive layer of the conductive studs thus also serves as a base or substrate for the electroplating process. Other

suitable methods for forming the conductive traces and connection pads may also be used. The thickness of the conductive traces or connection pads, for example, may be as low as about 10μm. As shown, the conductive traces and connection pads are formed over the insulating layer 174 in the die region of the package substrate and are electrically coupled to the conductive studs 172. The conductive traces and connection pads are coupled to the conductive studs and are coupled to die contacts 270 of a flip chip later.

[00118] After forming the conductive traces and connection pads, a flip chip 220 having die contacts 270 on an active surface of the die is mounted onto the die region, similar to that described with respect to Fig. 11c. The process continues, as similarly described in Fig. 11c and onwards. As such, these process steps will not be described or described in detail. The process continues until a package as shown in Fig. $13f_{ii}$ similar to that shown in Fig. 6 is formed.

[00119] Figs. 14a-e show another embodiment of a process for forming a semiconductor package. The process is similar to that described in Figs. 10a-j, Figs. 11a-d, Figs. 12a-f and Figs. 13a-f. As such, common elements may not be described or described in detail.

[00120] Referring to Fig. 14a, a partially processed package substrate is provided. The partially processed package substrate is at the stage of processing as described in Fig. 13b. For example, via contacts 107 are formed in the cavities or vias between the protruded portions and the first conductive layer 1431 of the conductive carrier 1430 is removed.

[00121] The process continues to remove the second conductive layer 1433. In one embodiment, an etch process may be performed to remove the second conductive layer. Since the second and third conductive layer include different materials, the etch for example, stops at the second surface 1435b of the third conductive layer, exposing the surface of the third conductive layer. Other techniques for removing the second conductive layer may also be useful.

[00122] Referring to Fig. 14b, the process continues to form further interconnect level 170 of the package substrate. The process continues to form conductive studs 272 over the conductive via contacts. The process continues to form conductive studs 272 over the via contacts as shown in Fig. 14b. In one embodiment, portions of the third conductive layer 1435 are removed to form the conductive studs. In one embodiment, the third conductive layers of the conductive carrier are patterned to create a pattern which defines the conductive studs 272 with cavities or vias 1619 in between the conductive studs as shown in Fig. 14b. Patterning of the third conductive layer of the conductive carrier may be performed with the help of a patterned masked layer. Patterning of the third conductive layer can be achieved by any suitable etching techniques. For example, a patterned etch mask (not shown), such as photoresist, is provided over the third conductive layer. An etch process may be performed using the etch mask to remove portions of the third conductive layer unprotected by the etch mask. Other techniques for patterning the second and third conductive layers may also be useful. As shown in Fig. 14b, portions of the third conductive layer unprotected by the mask are removed.

[00123] The conductive studs 272, as formed, include a single conductive layer. The width and thickness of the conductive studs as formed, for example, may be lesser than or equal to the width and thickness of the via contacts. Other suitable widths may also be useful. The thickness of the conductive studs, as shown, corresponds to the thickness of the third conductive layer 1435.

[00124] An insulating layer 274 is provided, covering and filling the spaces between the conductive studs 272 as shown in Fig. 14c. The insulating layer provides insulation between the conductive studs. In one embodiment, the insulating layer includes a dielectric material such as solder mask or inorganic insulating film. The insulating layer, for example, may be formed by molding or lamination technique. Other types of dielectric materials and techniques for forming the insulation layer may also be useful. As shown in Fig. 14c, the insulating layer is formed

around the conductive stud, exposing the first surface 272a of the conductive studs. The thickness of the insulating layer 274, for example, may be substantially the same as or lesser than the thickness of the conductive studs 272.

[00125] The process continues to form conductive traces 130 and connection pads 132 over the insulating layer 274 and which are coupled to the conductive studs 272. In one embodiment, the conductive traces 130 and connection pads 132 are formed of the same material of the conductive studs 272, such as copper. Other types of conductive materials, such as different than the conductive studs, may also be useful. The conductive traces and connection pads, in one embodiment, are formed by plating. For example, electrochemical or electroless plating may be employed to form the conductive traces and connection pads. The conductive studs 272 thus also serve as a base or substrate for the electroplating process. Other suitable methods for forming the conductive traces may also be used. The thickness of the conductive traces or connection pads, for example, may be as low as about 10μm. As shown, the conductive traces are formed over the insulating layer 274 and top surface of the conductive studs in the die and non-die regions of the package substrate and are electrically coupled to the conductive studs 272. The conductive traces 130 may be extended from the side surfaces of the conductive studs 272.

[00126] Referring to Fig. $14e_i$, a die 110 which includes circuit components similarly described in Fig. 12i is attached by an adhesive layer 150 to the die region of the package substrate. The process continues, as similarly described in Fig. 10i and onwards. As such, these process steps will not be described or described in detail. The process continues until a package as shown in Fig. $14e_i$ similar to that shown in Fig. 5 is formed.

[00127] In another embodiment, conductive traces 230 and connection pads 232 of the package substrate are formed after forming the insulating layer 274 as described in Fig. 14c. In one embodiment, the conductive traces and connection pads are formed of the same material of the conductive studs 272, such as copper. Other types of conductive materials, such as the

different than the conductive studs, may also be useful. The conductive traces and connection pads, in one embodiment, are formed by plating. For example, electrochemical or electroless plating may be employed to form the conductive traces and connection pads. The conductive studs 272 thus also serve as a base or substrate for the electroplating process. Other suitable methods for forming the conductive traces and connection pads may also be used. The thickness of the conductive traces or connection pads, for example, may be as low as about 10μm. As shown, the conductive traces are formed over the insulating layer 274 and top surface of the conductive studs 272 in the die region of the package substrate and are electrically coupled to the conductive studs 272. The conductive traces and connection pads are coupled to the conductive studs 272 and are coupled to die contacts 270 of a flip chip later.

[00128] After forming the conductive traces and connection pads, a flip chip 220 having die contacts 270 on an active surface of the die is mounted onto the die region, similar to that described with respect to Fig. 11c. The process continues, as similarly described in Fig. 11c and onwards. As such, these process steps will not be described or described in detail. The process continues until a package similar to that shown in Fig. 7 is formed.

[00129] The embodiments described with respect to Figs. 13a-f and Figs. 14a-e include some or all advantages as described with respect to Fig. 10a-j, Figs. 11a-d and Figs. 12a-f. As such, these advantages will not be described or described in detail. The embodiments, as described with respect to Figs. 13a-f and Figs. 14a-e result in further advantages. The embodiments of Figs. 13a-f and Figs. 14a-e include formation of further interconnect level of the package substrate. The further interconnect level includes conductive studs. The width of the conductive studs, as described, is smaller than the width of the via contacts. The conductive studs as described need not be formed at the center of the via contacts and its smaller width relative to the via contacts provide allowance for more traces, leading to more flexible and efficient routability of traces.

[00130] Furthermore, conductive traces of the embodiments as described in Figs. 13a-f and Figs. 14a-e are formed by plating. Such technique allows fine pitch traces to be formed, resulting in thinner packages. The second conductive layer, in the embodiment described in Figs. 14a-e, may be removed after removing the first conductive layer. This allows the conductive stud to be formed of a single material which is the same material as the via contacts. Resistance is lowered particularly where the interconnect structure of the package substrate, including the conductive traces, studs and via contacts, is formed of a single material. This further enhances the performance of the semiconductor packages. Moreover, the conductive studs as described in the embodiment of Figs. 14a-e have thinner profile. This enables further thinner packages to be formed.

[00131] Figs. 15a-h show another embodiment of a process for forming a semiconductor package. The process include similar process to that described in Figs. 10a-j, Figs. 11a-d, Figs. 12a-f and Figs. 13a-f and Figs. 14a-e. As such, common processes may not be described or described in detail. Referring to Fig. 15a, a conductive carrier 1430 is provided. The conductive carrier 1430 is similar to that described in Fig. 12b. The materials, thickness and process for forming the conductive carrier are similar to that described in Fig. 12b. As such, common elements may not be described or described in detail. In one embodiment, the conductive carrier also serves as via contacts in the package substrate while forming part of the interconnect structures of the package substrate as will be described later.

[00132] The process continues to remove portions of the first conductive layer 1431. In one embodiment, the first conductive layer 1431 of the conductive carrier 1430 is patterned to create a pattern which defines the via contacts 307 of the package substrate with cavities or vias 1719 in between the via contacts. Patterning of the first conductive layer of the conductive carrier may be performed with the help of a patterned masked layer. Patterning of the first conductive layer can be achieved by any suitable etching techniques. For example, a patterned etch mask (not

shown), such as photoresist, is provided over the conductive carrier. An etch may be performed using the etch mask to remove portions of the first conductive layer unprotected by the etch mask. The etch, for example, may be an isotropic etch, such as a wet etch. An anisotropic etch, such as reactive ion etch (RIE) may be used. Since the first and second conductive layers include different materials, the etch for example, stops at the second surface 1433b of the second conductive layer 1433, exposing the surface of the second conductive layer. As such, the second conductive layer serves as an etch stop layer. Other techniques for patterning the first conductive layer may also be useful.

[00133] After patterning the first conductive layer, the mask is removed. The mask, for example, may be removed by ashing. Other techniques for removing the mask may also be useful.

[00134] The process continues by forming a substrate material over the conductive carrier. In one embodiment, a substrate material is dispensed over the conductive carrier and filling the cavities 1719 between the via contacts 307. In one embodiment, the substrate material is a mold compound, such as molding epoxy resin material. Providing other suitable types of substrate material may also be useful.

[00135] The substrate material, in one embodiment, is formed by transfer molding technique. Mold material, for example, is dispensed into the mold assembly, filling the cavities in between the via contacts. After molding, the molded structure is separated from the mold. Other suitable types of techniques for forming the substrate material may also be useful. For example, the substrate material may also be formed by printing, film assisted molding or compression molding.

[00136] The process continues to remove portions of the molded structure. In one embodiment, excessive portions of the mold material over the first conducive layer are removed. In one embodiment, excessive portions of the mold material over the first conductive layer are

removed by grinding. Other suitable techniques may also be used to remove excessive portions of the mold material. In one embodiment, grinding process is performed to remove the excess portions of the mold material and stops at the second surface 307b of the via contacts, leaving the mold material in between the via contacts as shown in Fig. 15c. The mold materials which remain in between the conductive via contacts after the grinding process may be referred to as the base substrate of the package substrate. The mold materials also serve as insulating layer providing electrical isolation between adjacent via contacts.

[00137] In one embodiment, the process continues to form further interconnect level of the package substrate. The process continues to form conductive studs 372 over the via contacts. In one embodiment, portions of the second and third conductive layers are removed to form the conductive studs 372. In one embodiment, the second and third conductive layers 1433 and 1435 of the conductive carrier are patterned to create a pattern which defines the conductive studs with spaces 1739 in between the conductive studs as shown in Fig. 15d. Patterning of the second and third conductive layers of the conductive carrier may be performed with the help of a patterned masked layer. Patterning of the second and third conductive layers can be achieved by any suitable etching techniques. For example, a patterned etch mask (not shown), such as photoresist, is provided over the third conductive layer. A two-step etch process may be performed using the etch mask to remove portions of the second and third conductive layers unprotected by the etch mask. The first etch, for example, removes portions of the third conductive layer 1435 unprotected by the mask. Thus, the second conductive layer 1433 serves as an etch stop layer during the removal of the portions of the third conductive layer 1435. The second etch, for example, removes portions of the second conductive layer 1433 unprotected by the mask. The second etch, for example, stops at the first surface 307a of the conductive via contacts. Other techniques for patterning the second and third conductive layers may also be useful.

[00138] The conductive studs 372 as formed, in one embodiment, include a multi layered stack $372_{1\text{-}2}$ as shown in Fig. 15d. The width and thickness of the conductive studs as formed, for example, may be less than or equal to the width and thickness of the via contacts. Other suitable widths may also be useful. The thickness of the conductive studs, as shown, corresponds to the thickness of the second and third conductive layers of the conductive carrier.

[00139] An insulating layer 374 is provided, covering and filling the spaces between the conductive studs 372 as shown in Fig. 15e. The insulating layer provides insulation between the conductive studs. In one embodiment, the insulating layer includes a dielectric material such as solder mask or inorganic insulating film. The insulating layer, for example, may be formed by molding or lamination technique. Other types of dielectric materials and techniques for forming the insulation layer may also be useful. As shown in Fig. 15e, the insulation layer is formed around the conductive studs, exposing the first surface 372a of the conductive studs. The thickness of the insulating layer 374, for example, may be substantially the same as or lesser than the thickness of the conductive studs 372.

[00140] The process continues to form conductive traces 130 and connection pads 132 of the package substrate as shown in Fig. 15f. In one embodiment, the conductive traces 130 and connection pads 132 are formed of the same material as the conductive studs. Other types of conductive materials, such as different than the conductive studs, may also be useful. The conductive traces 130 and connection pads 132, in one embodiment, are formed by plating. For example, electrochemical or electroless plating may be employed to form the conductive traces and connection pads. The first conductive layer 372_1 and/or the second conductive layer 372_2 of the conductive studs 372 thus also serve as a base or substrate for the electroplating process. Other suitable methods for forming the conductive traces and connection pads may also be used. The thickness of the conductive traces or connection pads, for example, may be as low as about 10μm. As shown, the conductive traces are formed over the insulating layer 374 and top

surface of the conductive studs 372 in the die and non-die regions of the package substrate and are electrically coupled to the conductive studs 372. The conductive traces 130 may be extended from the side surfaces of the conductive studs 372. In cases where the conductive studs 372 include a multi-layered stack, the conductive traces 130 may extend from the two or more layers of the multi-layered stack of the conductive studs 372.

[00141] A die 110 which includes circuit components similarly described in Fig. 10i is attached by an adhesive layer 150 to the die region of the package substrate as shown in Fig. 15g. The process continues, as similarly described in Fig. 10i and onwards. As such, these process steps will not be described or described in detail. The process continues until a package as shown in Fig. 15h similar to that shown in Fig. 8 is formed.

[00142] Figs. 16a-g show another embodiment of a process for forming a semiconductor package. The process include similar processes to that described in Figs. 10a-j, Figs. 11a-d, Figs. 12a-f and Figs. 13a-f, Figs. 14a-e and Figs. 15a-h. As such, common elements may not be described or described in detail. Referring to Fig. 16a, a partially processed package substrate is provided. The partially processed package substrate is at the stage of processing as described in Fig. 15c. For example, mold material, for example, remains in the cavities in between the via contacts 307. The mold materials which remain in between the via contacts after the grinding process may be referred to as the base substrate 306 of the package substrate. The mold materials also serve as insulating layer providing electrical isolation between adjacent via contacts.

[00143] The process continues by removing the second and third conductive layers 1433 and 1435 of the conductive carrier as shown in Fig. 16b. In one embodiment, the second and third conductive layers of the conductive carrier is removed by an etch process. The etch process, for example, may be a two-step etch process. The first etch, for example, removes the third conductive layer 1435. Thus, the second conductive layer 1433 serves as an etch stop layer

during the removal of the third conductive layer 1435. The second etch, for example, removes the second conductive layer 1433. The second etch, for example, stops at the first surface 307a of the via contacts. Other suitable types of techniques may also be employed to remove the second and third conductive layers.

[00144] Referring to Fig. 16c, the process continues to form further interconnect level for the package substrate. In one embodiment, an insulating layer 474 is provided over the first surface 307a of the via contacts and the base substrate 306a as shown in Fig. 16c. In one embodiment, the insulating layer includes a photosensitive dielectric material such as a UV sensitive laminate. The thickness of the insulating layer 474 defines the thickness of conductive studs 472 to be formed later. The insulating layer, for example, may be formed by molding or lamination technique. Other types of dielectric materials and deposition techniques may also be useful for forming the insulation layer.

[00145] The process continues to remove portions of the insulating layer. In one embodiment, the insulating 474 layer is patterned to create cavities 1819 which define the locations where conductive studs 472 of the package substrate are to be formed as shown in Fig. 16c. The width of the cavities, for example, is smaller than the width of the via contacts. Patterning of the insulating layer may be performed with the help of a patterned masked layer. Patterning of the insulating layer can be achieved by any suitable etching techniques. For example, a patterned etch mask (not shown), such as photoresist, is provided over the insulating layer. An etch may be performed using the etch mask to remove portions of the insulating layer unprotected by the etch mask. The etch, for example, may be an isotropic etch, such as a wet etch. An anisotropic etch, such as reactive ion etch (RIE) may be used. Other techniques for patterning the insulating layer may also be useful.

[00146] The process continues to form conductive studs 472 over the via contacts 307 as shown in Fig. 16d. In one embodiment, the conductive studs 472 may be formed of a single

conductive material. The conductive studs, for example, may include the same material as the via contacts. In another embodiment, the conductive studs may be formed of two or more conductive materials, forming a multi-layered stack. The multi-layered stack, for example, may include copper, nickel or a combination thereof. Other types of conductive materials may also be useful.

[00147] In one embodiment, the conductive studs 472 are formed by plating. For example, electrochemical or electroless plating may be employed to form the conductive studs. Thus, one or more layer may be plated to form the conductive studs. The first surface 307a of the via contacts thus also serves as a base or substrate for the electroplating process. Other suitable methods for forming the conductive studs may also be used. The thickness of the conductive studs, for example, may be about the same as or lower than the thickness of the insulating layer 474.

[00148] The process continues to form conductive traces and connection pads of the package substrate as shown in Fig. 16e. In one embodiment, the conductive traces 130 and connection pads 132 are formed of the same material as the conductive studs. Other types of conductive materials, such as different than the conductive studs, may also be useful. The conductive traces 130 and connection pads 132, in one embodiment, are formed by plating. For example, electrochemical or electroless plating may be employed to form the conductive traces and connection pads. The first surface 472a of the conductive studs thus also serves as a base or substrate for the electroplating process. Other suitable methods for forming the conductive traces and connection pads may also be used. The thickness of the conductive traces or connection pads, for example, may be as low as about 10μm. As shown, the conductive traces and connection pads are formed over the insulating layer 474 and top surface of the conductive studs in the die and non-die regions of the package substrate and are electrically coupled to the conductive studs 472.

[00149] A die 110 which includes circuit components similarly described in Fig. 10i is attached by an adhesive layer 150 to the die region of the package substrate as shown in Fig. 16f. The process continues, as similarly described in Fig. 10i and onwards. As such, these process steps will not be described or described in detail. The process continues until a package as shown in Fig. 16g similar to that shown in Fig. 9 is formed.

[00150] The embodiments described with respect to Figs. 15a-h and Figs. 16a-g include some or all advantages as described with respect to Fig. 10a-j, Figs. 11a-d, Figs. 12a-f, Figs. 13a-f and Figs. 14a-e. As such, these advantages will not be described or described in detail. The embodiments, as described with respect to Figs. 15a-h and Figs. 16a-g result in further advantages. For example, the second conductive layer acts as a barrier during the removal of portions of the first conductive layer to form the via contacts. As such, the thickness of the via contacts may be varied depending on the thickness of the first conductive layer as provided. Moreover, the via contacts as described in the embodiments of Figs. 15a-h and Figs. 16a-g are formed by an etch process. Such technique offers a less costly solution to form via contacts relative to other techniques.

[00151] The embodiments as described in Figs. 15a-h and Figs. 16a-g allows the interconnect structures, including the via contacts, conductive studs and conductive traces, to be formed at the peripheries of the package substrate. As such, the side surfaces of the interconnect structures at the peripheries of the package substrate are exposed. Such configuration improves the thermal performance of the package or may be used as castellation leads for clip connections.

[00152] The embodiments as described in Figs. 10a-j, Figs. 11a-d, Figs. 12a-f, Figs. 13a-f Figs. 14a-e, Figs. 15a-h and Figs. 16a-g provide flexibility and are customizable based on design requirements. For example, for application where larger pitch is desired, for example, solder joint pin applications, etching process may be employed. On the other hand, for applications which require smaller pitch and high density line/space area (e.g., conductive traces), plating

process may be used. The line/space pitch formed by plating process is advantageous as it is finer and more stable.

[00153] Figs. 17-18 show top views of a first surface of various embodiments of a package substrate. For example, Fig. 17 shows top view of a first surface of the embodiments as described in Figs. 1-3. As shown in Fig. 17, depending on the capability of chemical etching technique, one conductive trace is able to pass between two via contacts within a pitch A. Fig. 18, on the other hand, shows top view of a first surface of the embodiments as described in Figs. 4-9. Referring to Fig. 18, the package substrate includes conductive studs. For the same pitch A, the conductive studs enable at least two or more traces to pass between two via contacts, depending on the width of the conductive studs. Moreover, the conductive studs need not be positioned at the center of the via contacts, resulting in more flexible and efficient routability of traces.

[00154] The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The foregoing embodiments, therefore, are to be considered in all respects illustrative rather than limiting the invention described herein.

What is claimed is:

CLAIMS

1. A method for forming a semiconductor package comprising:

providing a package substrate having first and second major surfaces, wherein the package substrate comprises a base substrate having a mold material and a plurality of interconnect structures including via contacts extending through the first to the second major surface of the package substrate, wherein providing the package substrate comprises

providing a conductive carrier having first, second and third conductive layers, wherein the first conductive layer is patterned to define a pattern which defines the via contacts of the package substrate and a plurality of cavities and the second conductive layer serves as an etch stop layer while patterning the first conductive layer, and

wherein the via contact comprises a width defined by circumference of the via contact; and

filling the cavities with the mold material to form the base substrate of the package substrate;

forming further interconnect level of the package substrate which comprises forming a plurality of conductive studs directly coupled to and contact the via contacts by patterning the second and third conductive layers of the same conductive carrier, wherein a width of the conductive stud which is defined by circumference of the conductive stud is smaller than the width of the via contacts and the conductive stud is formed and contained within and does not extend beyond the width of the via contact;

providing a die having conductive contacts on its first or second surface, wherein the conductive contacts of the die are electrically coupled to the interconnect structures; and

forming a cap over the package substrate to encapsulate the die.

2. The method of claim 1 comprising forming conductive traces which are coupled to and contacts the conductive studs having materials of the second and third conductive layers, wherein the via contacts, conductive studs and conductive traces form the interconnect structures.

3. The method of claim 2 wherein the conductive traces are formed by plating.

4. The method of claim 3 wherein the conductive traces extends from under the die to periphery region of the die.

5. The method of claim 1 comprising providing a dielectric layer in direct contact with and partially covers the via contacts.

6. The method of claim 1 wherein the conductive studs are formed at peripheries of the package substrate such that side surfaces of the conductive studs are exposed.

7. The method of claim 1 wherein the first conductive layer is patterned by a mask and an etch to remove portions of the first conductive layer unprotected by the mask.

8. The method of claim 1 wherein:

excessive mold material is formed above a top surface of the via contact; and comprising

removing excessive mold material from one surface of the conductive carrier such that top surfaces of the via contacts are exposed.

9. The method of claim 1 wherein the cavities are filled by the mold material by transfer molding, printing, film assisted molding or compression molding technique.

10. The method of claim 1 wherein the conductive stud is formed at the center of the via contact.

11. The method of claim 1 wherein:

the second and third conductive layers are formed by plating; and

the second conductive layer comprises a material which is different than materials of the first and third conductive layers.

12. The method of claim 11 wherein the second conductive layer comprises nickel and the first and third conductive layers comprise copper.

13. The method of claim 1 wherein patterning the second and third conductive layers comprises first and second etch processes.

14. The method of claim 13 wherein the first etch process removes portions of the third conductive layer and stops on the second conductive layer and the second etch process removes portions of the second conductive layer and stops at a surface defined by top surfaces of the via contacts and the mold material.

15. The method of claim 1 comprising providing an insulating layer which covers and fills spaces between the conductive studs, wherein the insulating layer also partially covers and contacts top surface of the via contacts.

16. The method of claim 15 comprising forming conductive traces which are directly coupled to and extend from side surfaces of the conductive studs.

17. The method of claim 16 wherein the conductive traces are formed directly over top surface of the insulating layer.

18. The method of claim 17 wherein the conductive traces extend from the side surfaces of the conductive studs and beyond the width of the conductive studs.

19. The method of claim 18 wherein the cap directly contacts top surface of the conductive traces.

20. The method of claim 15 wherein top surface of the conductive studs is flushed with top surface of the insulating layer.

21. The method of claim 20 wherein the insulating layer and the mold material comprise different dielectric materials.

22. The method of claim 21 wherein the insulating layer comprises solder mask or inorganic insulating film and the mold material comprises epoxy resin material.