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ABSTRACT



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This invention describes a method and apparatus for vertically locking input and output video frame rates. The output vertical sync pulse is locked in
5 phase with the input vertical sync pulse, regardless of the input format and frequency. The output resolution, horizontal refresh rate, and delay are all user selectable. Two Phase Locked Loops are connected in series to achieve vertical lock between the input and output frames. Locking the vertical sync pulses between the input and output frames will eliminate mixing of pixels from
10 different input frames in one output frame. The first Phase Locked Loop generates the output pixel clock required to satisfy the user's display preferences but may not precisely represent the desired output pixel clock required for frame locking because current Phase Locked Loops use integer dividers. A second Phase Locked Loop adjusts its output, which is the reference frequency to
15 the first Phase Locked Loop, until a lock is achieved. A free running oscillator measures the frequency of the incoming video and sends its output to a micro-controller that computes the divider required in the first Phase Locked Loop based on user selected output resolution. The user may also adjust the delay between the vertical input and output video frames.

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(Figure 8)