

TRI-GATE DEVICES AND METHODS OF FABRICATION

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to the field of semiconductor integrated circuit manufacturing, and more particularly to a tri-gate fully depleted substrate transistor and its methods of fabrication.

2. DISCUSSION OF RELATED ART

In order to increase device performance, silicon on insulator (SOI) transistors have been proposed for the fabrication of modern integrated circuits. Figure 1 illustrates a standard fully depleted silicon on insulator (SOI) transistor 100. SOI transistor 100 includes a single crystalline silicon substrate 102 having an insulating layer 104, such as a buried oxide formed thereon. A single crystalline silicon body 106 is formed on the insulating layer 104. A gate dielectric layer 108 is formed on the single crystalline silicon body 106 and a gate electrode 110 formed on the gate dielectric 108. Source 112 and drain 114 regions are formed in the silicon body 106 along laterally opposite sides of gate electrode 110.

Fully depleted SOI have been proposed as a transistor structure to take advantage of ideal sub-threshold gradients for optimized on current/off current ratios. In order to achieve ideal subthreshold gradients with transistor 100, the thickness of the silicon body 106 must be about 1/3 the size of the gate length (Lg) of the transistor or Tsi = Lg/3. However, as gate lengths scale especially as they approach 30nm, the need for ever decreasing silicon film thickness (Tsi) makes this approach increasingly impractical. At 30 nanometer gate length, the thickness required of the silicon body is thought to need to



be less than 10 nanometers, and around 6 nanometer for a 20 nanometer gate length. The fabrication of thin silicon films with thicknesses of less than 10 nanometers, is considered to be extremely difficult. On one hand, obtaining wafer uniformity on the order of one nanometer is a difficult challenge. On the other hand, to be able to contact these thin films to form raised source/drain regions to decrease junction resistance, becomes almost impossible since the thin silicon layer in the source/drain regions becomes consumed during the gate etch and various cleans following the gate etch and spacer etch leaving insufficient silicon 106 for silicon to grow on.

A double gate (DG) device, such as shown in Figures 2A and 2B, have been proposed to alleviate the silicon thickness issue. The double gate (DG) device 200 includes a silicon body 202 formed on an insulating substrate 204. A gate dielectric 206 is formed on two sides of the silicon body 202 and a gate electrode 208 is formed adjacent to the gate dielectric 206 formed on the two sides of the silicon body 202. A sufficiently thick insulating layer 209, such as silicon nitride, electrically isolates the gate electrode 208 from the top of silicon body 202.

Double gate (DG) device 200 essentially has two gates, one on either side of the channel of the device. Because the double gate device 200 has a gate on each side of the channel, thickness (Tsi) of the silicon body can be double that of a single gate device and still obtain a fully depleted transistor operation. That is, with a double gate device 200 a fully depleted transistor can be formed where Tsi = (2xLg)/3. The most manufacturable form of the double gate (DG) device 200, however, requires that the body 202 patterning be done with photolithography that is 0.7 x smaller than that used to pattern the gate length (Lg) of the device. In order to obtain high density integrated circuits, it is generally desirable to have the most aggressive lithography occur with respect to the gate length (Lg) of the gate electrode 208. Although, double gate structures double the thickness of the silicon film (since there now is a gate on either side of the channel) these structures, however, are hideously difficult to fabricate. For example, silicon body 202 requires a

silicon body etch which can produce a silicon body 202 with an aspect ratio (height to width) of about 5:1.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is an illustration of a cross-sectional view of a depleted substrate transistor.

Figures 2A and Figure 2B illustrate a double gate depleted substrate transistor.

Figure 3 is an illustration of a tri-gate transistor in accordance with an embodiment of the present invention.

Figure 4A is an illustration of a tri-gate transistor in accordance with an embodiment of the present invention.

Figure 4B is an illustration of a tri-gate transistor in accordance with an embodiment of the present invention.

Figures 5A-5J illustrate methods of fabricating a tri-gate transistor in accordance with embodiments of the present invention.

Figure 6 is a plot which illustrates body heights and body widths which can be used to obtain partially depleted and fully depleted tri-gate transistors having gate lengths (lg) of 30 nm and 20 nm.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

The present invention is a novel tri-gate transistor structure and its method of fabrication. In the following description numerous specific details are set forth in order to provide a thorough understanding in the present invention. In other instances, well-known semiconductor process and manufacturing techniques have not been described in particular detail in order to not unnecessarily obscure the present invention.

The present invention is novel tri-gate transistor structure and its method of fabrication. In an embodiment of the present invention, the tri-gate transistor is a semiconductor on insulator (SOI) transistor. The tri-gate transistor is ideal for use in fully depleted substrate transistor applications. The tri-gate transistor includes a thin semiconductor body formed on an substrate, the substate can be an insulating substrate or a semiconductor substrate. A gate dielectric is formed on the top surface and the sidewalls of the semiconductor body. A gate electrode is formed on the gate dielectric on the top surface of the semiconductor body and is formed adjacent to the gate dielectric formed on the sidewalls of the semiconductor body. Source and drain regions are formed in the semiconductor body on opposite sides of the gate electrode. Because the gate electrode and the gate dielectric surround the semiconductor body on three sides, the transistor essentially has three separate channels and gates. The gate "width" of a transistor is equal to the sum of each of the three sides of the semiconductor body. Larger "width" transistors can be formed by connecting several tri-gate transistors together.

Because there are three separate channels formed in the semiconductor body, the semiconductor body can be fully depleted when the transistor is turned "ON", thereby enabling the formation of a fully depleted transistor with gate lengths of less than 30 nanometers without requiring the use of ultra-thin semiconductor bodies or requiring photolithographic patterning of the semiconductor bodies to dimensions less than the gate length (Lg) of the device. That is, the structure of the tri-gate transistor of the present invention enables a fully depleted transistor to be fabricated where the thickness of the

semiconductor body and width of the semiconductor body are equal to the gate length of the device. Because the novel tri-gate transistor of the present invention can be operated in a fully depleted manner, the device is characterized by ideal (i.e., very sharp) subthreshold slope and a reduced drain induced barrier lowering (DIBL) short channel effect of less than 100mV/V and ideally about 60 mV/V which results in a lower leakage current when the device is turned "OFF" resulting in lower power consumption.

An example of a tri-gate transistor 300 in accordance with an embodiment of present invention as illustrated in Figure 3. Tri-gate transistor 300 is formed on an substrate 302. In an embodiment of the present invention, substrate 302 is an insulating substrate which includes a lower monocrystalline silicon substrate 304 upon which is formed in insulating layer 306, such as a silicon dioxide film. Tri-gate transistor 300, however, can be formed on any well-known insulating substrate such as substrates formed from silicon dioxide, nitrides, oxides, and shappires. In an embodiment of the present invention, the substrate 302 can be a semiconductor substrate, such as but not limited to monocrystalline silicon substrate and gallium arsenide substrate.

Tri-gate transistor 300 includes a semiconductor body 308 formed on insulator 306 of insulating substrate 302. Semiconductor body 308 can be formed of any well-known semiconductor material, such as but not limited to silicon (Si), germanium (Ge), silicon germanium (Si_xGe_y), gallium arsenide (GaAs), InSb, GaP, GaSb and carbon nanotubes. Semiconductor body 308 can be formed of any well-known material which can be reversibly altered from an insulating state to a conductive state by applying external electrical controls. Semiconductor body 308 is ideally a single crystalline film when the best electrical performance of transistor 300, is desired. For example, semiconductor body 308 is a single crystalline film when transistor 300 is used in high performance applications, such as in a high density circuit, such as a microprocessor. Semiconductor body 308, however, can be a polycrystalline film when transistor 300 is used in applications requiring less stringent performance, such as in liquid crystal displays. Insulator 306 insulates semiconductor body 308 from monocrystalline silicon substrate

302. In an embodiment of the present invention, semiconductor body 308 is a single crystalline silicon film. Semiconductor body 308 has a pair of laterally opposite sidewalls 310 and 312 separated by a distance which defines a semiconductor body width 314. Additionally, semiconductor body 308 has a top surface 316 opposite a bottom surface 318 formed on substrate 302. The distance between the top surface 316 and the bottom surface 318 defines a body height 320. In an embodiment of the present invention the body height 320 is substantially equal to the body width 314. In an embodiment of the present invention, the body 308 has a width 314 and height 320 less than 30 nanometers and ideally less than 20 nanometers. In an embodiment of the present invention, the body height 320 is between ½ the body width 314 to 2 times the body width 314.

Tri-gate transistor 300 has a gate dielectric layer 322. Gate dielectric layer 322 is formed on and around three sides of semiconductor body 308 as shown in Figure 3. Gate dielectric layer 322 is formed on or adjacent to sidewall 312, on top surface 316 and on or adjacent to sidewall 310 of body 308 as shown in Figure 3. Gate dielectric layer 322 can be any well-known gate dielectric layer. In an embodiment of the present invention, the gate dielectric layer is a silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y) or a silicon nitride (Si_3N_4) dielectric layer. In an embodiment of the present invention, the gate dielectric layer 322 is a silicon oxynitride film formed to a thickness of between 5-20Å. In an embodiment of the present invention, gate dielectric layer 322 is a high K gate dielectric layer, such as a metal oxide dielectric, such as but not limited to tantalum pentaoxide (Ta_2O_5), and titantium oxide (TiO_2). Gate dielectric layer 322 can be other types of high K dielectric, such as but not limited to PZT.

Tri-gate device 300 has a gate electrode 324. Gate electrode 324 is formed on and around gate dielectric layer 322 as shown in Figure 3. Gate electrode 324 is formed on or adjacent to gate dielectric 322 formed on sidewall 312 of semiconductor body 308, is formed on gate dielectric 322 formed on the top surface 316 of semiconductor body 308, and is formed adjacent to or on gate dielectric layer 322 formed on sidewall 310 of semiconductor body 308. Gate electrode 324 has a pair of laterally opposite sidewalls 326

and 328 separated by a distance which defines the gate length (Lg) 330 of transistor 300. In an embodiment of the present invention the laterally opposite sidewalls 326 and 328 of the gate electrode 324 run in a direction perpendicular to the laterally opposite sidewalls 310 and 312 of semiconductor body 308.

Gate electrode 324 can be formed of any suitable gate electrode material. In an embodiment of the present invention to gate electrode 324 comprises of polycrystalline silicon doped to a concentration density between $1x10^{19}$ atoms/cm^3 – $1x10^{20}$ atoms/cm^3. In an embodiment of the present invention the gate electrode can be a metal gate electrode, such as but not limited to, tungsten, tantalum, titanium, and their nitrides. In an embodiment of the present invention the gate electrode is formed from a material having a mid-gap work function between 4.6-4.8 eV. It is to be appreciated, the gate electrode 324 need not necessarily be a single material and can be a composite stack of thin films, such as but not limited to a polycrystalline silicon/metal electrode or a metal/polycrystalline silicon electrode.

Tri-gate transistor 300 has a source region 330 and a drain region 332. Source region 330 and drain region 332 are formed in semiconductor body 308 on opposite sides of gate electrode 324 as shown in Figure 3. The source region 330 and the drain region 332 are formed of the same conductivity type such as N-type or P-type conductivity. In an embodiment of the present invention source region 330 and drain region 332 have a doping concentration of between $1x10^{19}$, and $1x10^{21}$ atoms/cm^3. Source region 330 and drain region 332 can be formed of uniform concentration or can include subregions of different concentrations or doping profiles such as tip regions (e.g., source/drain extensions). In an embodiment of the present invention when transistor 300 is a symmetrical transistor, source region 330 and drain region 332 will have the same doping concentration and profile. In an embodiment of the present invention when tri-gate transistor 300 is formed as an asymmetric transistor then the doping concentration and profile of the source region 330 and the drain region 332 may vary in order to obtain a particular electrical characteristic.

The portion of semiconductor body 308 located between source region 330 and drain region 332, defines the channel region 350 of transistor 300. The channel region 350can also be defined as the area of the semiconductor body 308 surrounded by the gate electrode 324. At times however, the source/drain region may extend slightly beneath the gate electrode through, for example, diffusion to define a channel region slightly smaller than the gate electrode length (Lg). In an embodiment of the present invention channel region 350 is intrinsic or undoped monocrystalline silicon. In an embodiment of the present invention, channel region 350 is doped monocrystalline silicon. When channel region 350 is doped it is typically doped to a conductivity level of between $1x10^{16}$ to $1x10^{19}$ atoms/cm^3. In an embodiment of the present invention, when the channel region is doped it is typically doped to the opposite conductivity type of the source region 330 and the drain region 332. For example, when the source and drain regions are N-type conductivity the channel region would be doped to p type conductivity. Similarly, when the source and drain regions are P type conductivity the channel region would be N-type conductivity. In this manner a tri-gate transistor 300 can be formed into either a NMOS transistor or a PMOS transistor respectively. Channel region 350 can be uniformly doped or can be doped non-uniformly or with differing concentrations to provide particular electrical and performance characteristics. For example, channel regions 350 can include well-known "halo" regions, if desired.

By providing a gate dielectric and a gate electrode which surrounds the semiconductor body on three sides, the tri-gate transistor is characterized in having three channels and three gates, one (g1) which extends between the source and drain regions on side 312 of silicon body 308, a second (g2) which extends between the source and drain regions on the top surface 316 of silicon body 308, and the third (g3) which extends between the source and drain regions on the sidewall 310 of silicon body 308. The gate "width" (Gw) of transistor 300 is the sum of the widths of the three channel regions. That is, the gate width of transistor 300 is equal to the height 320 of silicon body 308 at sidewall 310, plus the width of silicon body of 308 at the top surface 316, plus the height

320 of silicon body 308 at sidewall 312. Larger "width" transistors can be obtained by using multiple devices coupled together (e.g., multiple silicon bodies 308 surrounded by a single gate electrode 324).

Because the channel region 350 is surrounded on three sides by gate electrode 324 and gate dielectric 322, transistor 300 can be operated in a fully depleted manner wherein when transistor 300 is turned "on" the channel region 350 fully depletes thereby providing the advantageous electrical characteristics and performance of a fully depleted transistor. That is, when transistor 300 is turned "ON" a depletion region is formed and a channel region 350 along with an inversion layer at the surfaces of region 350 (i.e., an inversion layer is formed on the side surfaces and top surface of the semiconductor body). The inversion layer has the same conductivity type as the source and drain regions and forms a conductive channels between the source and drain regions to allow current to flowthere between. The tri-gate transistor of the present invention, can be said to be a nonplanar transistor because the channel regions are formed in both the horizontal and verticle directions in semiconductor body 308. The depletion region depletes free carriers from beneath the inversion layers. The depletion region extends to the bottom of channel region 350, thus the transistor can be said to be a "fully depleted" transistor. Fully depleted transistors have improved electrical performance characteristics over non-fully depleted or partially depleted transistors. For example, by operating transistor 300 in the fully depleted manner, gives transistor 300 an ideal or very steep subthreshold slope. The tri-gate transistor can be fabricated with very steep sub-threshold slope of less than 80 mV/decade, and ideally about 60 mV/decade even when fabricated with semiconductor body thicknesses of less than 30 nm. Additionally, operating transistor 300 in the fully depleted manner, transistor 300 has an improved drain induced barrier (DIBL) low in effect which provides for better "OFF" state leakage which results in lower leakage and thereby lower power consumption. In an embodiment of the present invention the tri-gate transistor 300 has a DIBL effect of less than 100mV/V and ideally less than 40 mV/V.

Figure 6 is an illustration of two plots 602 and 604 which set forth the body height and body width which will produce either fully depleted (F.D) or partially depleted (P.D) tri-gate transistors having gate length (Lg) of 30 nm (602) and 20 nm (604) respectively. In an embodiment of the present invention, the body height, body width and gate length are chosen to have dimensions in which a fully depleted transistor will be formed. In other embodiments, the tri-gate transistor has a body height, body width and gate length such that a partially depleted transistor is formed.

In an embodiment of the present invention tri-gate transistor 300 the source and drain regions can include a silicon or other semiconductor film 410 formed on and around semiconductor body 308 as shown in Figure 4A. For example, semiconductor film 410 can be a silicon film or a silicon alloy such as silicon germanium (Si_xGe_y). In an embodiment of the present invention the semiconductor film 410 is a single crystalline silicon film formed of the same conductivity type as the source region 330 and drain region 332. In an embodiment of the present invention the semiconductor film can be a silicon alloy such as silicon germanium wherein silicon comprises approximately 1 to 99 atomic percent of the alloy. The semiconductor film 410 need not necessarily be a single crystalline semiconductor film and in an embodiment can be a polycrystalline film. In an embodiment of the present invention the semiconductor film 410 is formed on the source region 330 and on the drain region 332 of semiconductor body 308 to form "raised" source and drain regions. Semiconductor film 410 can be electrically isolated from a gate electrode 324 by a pair of dielectric sidewall spacers 420 such as silicon nitride or silicon oxide or composites thereof. Sidewall spacers 420 run along the laterally opposite sidewalls 326 and 328 of gate electrode 324 as shown in Figure 4A thereby isolating the semiconductor film 410 from gate electrode 324 as shown in Figure 4A. An embodiment of the present invention sidewalls spacers 420 have a thickness of between 20-200Å. By adding a silicon or semiconductor film to the source and drain regions 330 and 332 of the semiconductor body and forming "raised" source and drain regions, the thickness of the

source and drain regions is increased thereby reducing the source/drain contact resistance to transistor 300 and improving its electrical characteristics and performance.

In an embodiment of the present invention a silicide film 430, such as, but not limited to, titanium silicide, nickel silicide, and cobalt silicide is formed on the source region 330 and drain region 332. In an embodiment of the present invention silicide film 430 is formed on a silicon film 410 of silicon body 308 as shown in Figure 4A. Silicide film 430 however can also be formed directly onto the top surface 316 of silicon body 308. For example, silicide film 430 can be formed on silicon body 308 by first forming a silicon film such as an undoped silicon film and a silicon body and then completely consuming the silicon film during the silicide process. Dielectric spacers 420 enables silicide film 430 to be formed on semiconductor body 308 or silicon film 410 in a self-aligned process (i.e., a salicide process).

Additionally, in the embodiment of the present invention a semiconductor or silicon film 440 can also be formed on the top of gate electrode 324 as can a silicide film 450 on the top surface gate electrode 325 as can be a silicide film 450. Silicide film 450 and silicon film 440 are typically formed at the same time as silicide film 430 and silicon film 420 on silicon body 308. The formation of a silicon film 440 on silicide film 450 on the gate electrode reduces the contact resistance to the gate thereby improving the electrical performance of transistor 300.

As stated above the gate "width" of transistor 300 is equal to the sum of the three gate width created from semiconductor body 308 of transistor 300. In order to fabricate the transistors with larger gate widths, transistor 300 can include an additional or multiple semiconductor bodies or fingers 308 as shown in Figure 4B. Each semiconductor body 308 has a gate dielectric layer 322 formed on its top surface and sidewalls as shown in Figure 4B. Gate electrode 324 is formed on and adjacent to each gate dielectric 322 on each of the semiconductor bodies 308. Each semiconductor body 308 also includes a source region 330 and a drain region 332 formed in the semiconductor body 308 on opposite sides of gate electrode 324 as shown in Figure 4B. In an embodiment of the

present invention each semiconductor body 308 is formed with the same width and height (thickness) as the other semiconductor bodies 308. In an embodiment of the present invention each source regions 330 and drain regions 332 of the semiconductor bodies 308 are electrically coupled together by the semiconductor material used to form semiconductor body 308 to form a source landing pad 460 and a drain landing pad 480 as shown in Figure 4B. Alternatively, the source regions 330 and drain regions 332 can be coupled together by higher levels of metalization (e.g., metal 1, metal 2, metal 3...) used to electrically interconnect various transistors 300 together into functional circuits. The gate width of transistor 300 as shown in Figure 4B would be equal to the sum of the gate width created by each of the semiconductor bodies 308. In this way, the tri-gate transistor 300 can be formed with any gate width desired.

A method of fabricating a tri-gate transistor in accordance with embodiments of the present invention is illustrated in Figures 5A-5J. The fabrication of a tri-gate transistor begins with substrate 502. A silicon or semiconductor film 508 is formed on substrate 502 as shown in Figure 5A. In an embodiment of the present invention, the substrate 502 is an insulating substrate, such as shown in Figure 5A. In an embodiment of the present invention, insulating substrate 502 includes a lower monocrystalline silicon substrate 504 and a top insulating layer 506, such as a silicon dioxide film or silicon nitride film. Insulating layer 506 isolates semiconductor film 508 from substrate 504, and in embodiment is formed to a thickness between 200-2000Å. Insulating layer 506 is sometimes referred to as a "buried oxide" layer. When a silicon or semiconductor film 508 is formed on an insulating substrate 502, a silicon or semiconductor on insulating (SOI) substrate 500 is created. In other embodiments of the pesent invention, the substrate 502 can be a semiconductor substrate, such as but not limited to a silicon monocrystalline substrate and a gallium arsenide substrate.

Although semiconductor film 508 is ideally a silicon film, in other embodiments it can be other types of semiconductor films, such as but not limited to germanium (Ge), a silicon germanium alloy (Si_xGe_y), gallium arsenide (GaAs), InSb, GaP, GaSb, as well as

carbon nanotubes. In an embodiment of the present invention, semiconductor film 508 is an intrinsic (i.e., undoped) silicon film. In other embodiments, semiconductor film 508 is doped to a p type or n type conductivity with a concentration level between $1x10^{16}$-$1x10^{19}$ atoms/cm^3. Semiconductor film 508 can be insitu doped (i.e., doped while it is deposited) or doped after it is formed on substrate 502 by for example ion-implantation. Doping after formation enables both PMOS and NMOS tri-gate devices to be fabricated easily on the same insulating substrate. The doping level of the semiconductor body at this point determines the doping level of the channel region of the device.

Semiconductor film 508 is formed to a thickness which is approximately equal to the height desired for the subsequently formed semiconductor body or bodies of the fabricated tri-gate transistor. In an embodiment of the present invention, semiconductor film 508 has a thickness or height 509 of less than 30 nanometers and ideally less than 20 nanometers. In an embodiment of the present invention, semiconductor film 508 is formed to the thickness approximately equal to the gate "length" desired of the fabricated tri-gate transistor. In an embodiment of the present invention, semiconductor film 508 is formed thicker than desired gate length of the device. In an embodiment of the present invention, semiconductor film 580 is formed to a thickness which will enable the fabricated tri-gate transistor to be operated in a fully depleted manner for its designed gate length (Lg).

Semiconductor film 508 can be formed on insulating substrate 502 in any well-known method. In one method of forming a silicon on insulator substrate, known as the SIMOX technique, oxygen atoms are implanted at a high dose into a single crystalline silicon substrate and then anneal to form the buried oxide 506 within the substrate. The portion of the single crystalline silicon substrate above the buried oxide becomes the silicon film 508. Another technique currently used to form SOI substrates is an epitaxial silicon film transfer technique which is generally referred to as bonded SOI. In this technique a first silicon wafer has a thin oxide grown on its surface that will later serve as the buried oxide 506 in the SOI structure. Next, a high dose hydrogen implant is made into the first silicon wafer to form a high stress region below the silicon surface of the first

wafer. This first wafer is then flipped over and bonded to the surface of a second silicon wafer. The first wafer is then cleaved along the high stress plain created by the hydrogen implant. This results in a SOI structure with a thin silicon layer on top, the buried oxide underneath all on top of the single crystalline silicon substrate. Well-known smoothing techniques, such as HC smoothing or chemical mechanical polishing (CMP) can be used to smooth the top surface of semiconductor film 508 to its desired thickness.

At this time, if desired, isolation regions (not shown) can be formed into SOI substrate 500 in order to isolate the various transistors to be formed therein from one another. Isolation regions can be formed by etching away portions of the substrate film 508 surrounding a tri-gate transistor, by for example well-known photolithographic and etching techniques, and then back filling the etched regions with an insulating film, such as SiO_2.

In order to form a tri-gate transistor on substrate 500, a photoresist mask 510 is formed on semiconductor film 508 as shown in Figure 5B. The photoresist mask 510 contains a pattern or plurality of patterns 512 defining locations where semiconductor bodies or fins will be subsequently formed in the semiconductor film 508. The photoresist pattern 512 defines the width 518 desired of the subsequently formed semiconductor bodies or fins of the tri-gate transistor. In an embodiment of the present invention, the pattern 512 define fins or bodies having a width 518 which is equal to or greater than the width desired of the gate length (Lg) of the fabricated transistor. In this way, the most stringent photolithography constraints used to fabricate the transistor are associated with the gate electrode patterning and not the semiconductor body or fin definition. In an embodiment of the present invention, the semiconductor bodies or fins will have a width 518 less than or equal to 30 nanometers and ideally less than or equal to 20 nanometers. In an embodiment of the present invention, the patterns 512 for the semiconductor bodies or fins have a width 518 approximately equal to the silicon body height 509. In an embodiment of the present invention, the photoresist patterns 512 have a width 518 which

is between ½ the semiconductor body height 509 and two times the semiconductor body height 509.

Additionally, as shown in Figure 5B, the photoresist mask 510 can also include patterns 514 and 516 for defining locations where source landing pads and drain landing pads, respectively, are to be formed. The landing pads can be used to connect together the various source regions and to connect together the various drain regions of the fabricated transistor. The photoresist mask 510 can be formed by well-known photolithographic techniques including masking, exposing, and developing a blanket deposited photoresist film.

After forming photoresist mask 510, semiconductor film 508 is etched in alignment with photoresist mask 510 to form one or more silicon bodies or fins and source and drain landing pads (if desired) as shown in Figure 5C. Semiconductor film 508 is etched until the underlying buried oxide layer 506 is exposed. Well-known semiconductor etching techniques, such as anisotropic plasma etching or reactive ion etching can be used to etch semiconductor film 508 in alignment with mask 510 as shown in Figure 5C.

After semiconductor film 508 is etched to form semiconductor bodies or fins 520 (and source/drain landing pads 522 and 524, if desired) the photoresist mask is removed by well-known techniques, such as by chemical stripping and O_2 ashing, to produce the substrate shown in Figure 5D.

Next, a gate dielectric layer 526 is formed on and around each semiconductor body 520. That is, a gate dielectric layer 526 is formed on the top surface 527 of each of the semiconductor bodies 520 as well as on the laterally opposite sidewalls 528 and 529 of each of the semiconductor bodies 520. The gate dielectric can be a deposited dielectric or a grown dielectric. In an embodiment of the present invention, the gate dielectric layer 526 is a silicon dioxide dielectric film grown with a dry/wet oxidation process. In an embodiment of the present invention, the silicon oxide film is grown to a thickness of between 5-15Å. In an embodiment of the present invention, the gate dielectric film 526 is a deposited dielectric, such as but not limited to a high dielectric constant film, such as

metal oxide dielectric, such as tantalum pentaoxide (Ta_2O_5) and titanium oxide (TiO2) or other high-K dielectrics, such as PZT and BST. A high dielectric constant film can be formed by any well-known technique, such as by chemical vapor deposition (CVD).

Next, as shown in Figure 5E, a gate electrode 530 is formed. The gate electrode 530 is formed on the gate dielectric layer 526 formed on the top surface 527 of each of the semiconductor bodies 520 and is formed on or adjacent to the gate dielectric 526 formed on or adjacent to the sidewalls 528 and 529 of each of the semiconductor bodies as shown in Figure 5E. The gate electrode 530 has a top surface 532 opposite of bottom surface formed on the insulating substrate 502 and has a pair of laterally opposite sidewalls 534 and 536. The distance between the laterally opposite sidewalls 534 and 536 define the gate length (Lg) 538 of the tri-gate transistor. Gate electrode 530 can be formed by blanket depositing a suitable gate electrode material over the substrate shown in Figure 5D. The gate electrode can be formed to a thickness 533 between 200-3000Å. In an embodiment the gate electrode has a thickness or height 533 of at least three times the height 509 of semiconductor bodies 520. The gate electrode material is then patterned with well-known photolithography and etching techniques to form gate electrode 530 from the gate electrode material. In embodiment of the present invention, the gate electrode material comprises polycrystalline silicon. In another embodiment of the present invention, the gate electrode material comprises a polycrystalline silicon germanium alloy. In yet other embodiment of the present invention, the gate electrode material can comprise a metal film, such as tungsten, tantalum, and their nitrides. Gate electrode 530 can be formed by well-known techniques, such as by blanket depositing a gate electrode material over the substrate of Figure 5D and then patterning the gate electrode material with well-known photolithography and etching techniques. In an embodiment of the present invention, the photolithography process used to define gate electrode 530 utilizes the minimum or smallest dimension lithography process used to fabricate the tri-gate transistor. (That is, in an embodiment of the present invention, the gate length (Lg) 538 of gate electrode 530 has a minimum feature dimension of the transistor defined by photolithography.) In an

embodiment of the present invention, the gate length 538 is less than or equal to 30 nanometers and ideally less than or equal to 20 nanometers.

Next, source and drain regions for the transistor are formed in semiconductor body 520 on opposite sides of gate electrode 530. In an embodiment of the present invention, the source and drain regions include tip or source/drain extension regions. Source and drain extension regions 540 and 542, respectively, can be formed by placing dopants 544 into semiconductor bodies 520 on both sides 532, 534 of gate electrode 530 in order to form tip regions 540 and 542 as shown in Figure 5F. Source and drain landing pads 522 and 524 are not shown in Figures 5F-5J to better illustrate aspects of the present invention. If source and drain landing pads 522 and 524 are utilized, they may be doped at this time also. For a PMOS tri-gate transistor, the semiconductor fins or bodies 520 are doped to a p type conductivity and to a concentration between $1x10^{20}$-$1x10^{21}$ atoms/cm^3. For a NMOS tri-gate transistor, the semiconductor fins or bodies 520 is doped with n type conductivity ions to a concentration between $1x10^{20}$-$1x10^{21}$ atoms/cm^3. In an embodiment of the present invention, the silicon films are doped by ion-implantation. In an embodiment of the present invention, the ion-implantation occurs in a vertical direction (i.e., a direction perpendicular to substrate 500) as shown in Figure 5F. When gate electrode 530 is a polysilicon gate electrode, it can be doped during the ion-implantation process. Gate electrode 530 acts as a mask to prevent the ion-implantation step from doping the channel region(s) 548 of the tri-gate transistor. The channel region 548 is the portion of the silicon body 520 located beneath or surrounded by the gate electrode 530. If gate electrode 530 is a metal electrode, a dielectric hard mask maybe used to block the doping during the ion-implantation process. In other embodiments, other methods, such as solid source diffusion, may be used to dope the semiconductor body to form source and drain extensions.

In embodiments of the present invention, "halo" regions can be formed in silicon body prior to the formation of a source/drain regions or source/drain extension regions. Halo regions are doped regions formed in the channel region 548 of the device and are of

the same conductivity but of a slightly higher concentration than the doping of the channel region of the device. Halo regions can be formed by ion-implantating dopants beneath the gate electrode by utilizing large angled ion-implantation techniques.

Next, if desired, the substrate shown in Figure 5F can be further processed to form additional features, such as heavily doped source/drain contact regions, deposited silicon on the source and drain regions as well as the gate electrode, and the formation of silicide on the source/drain contact regions as well as on the gate electrode.

In embodiments of the present invention, dielectric sidewall spacers 550 can be formed on the sidewalls of the gate electrode. Sidewall spacers can be utilized to offset heavy source/drain contact implants, can be used to isolate source/drain regions from the gate electrode during a selective silicon deposition processes and can be used in a salicide process to form silicide on the source and drain regions as well as on the gate electrode. Spacers can be formed by blanket depositing a conformal dielectric film 550, such as but not limited to silicon nitride, silicon oxide, silicon oxynitride or combination thereof over the substrate 500 of Figure 5F. Dielectric film is deposited in a conformal manner so that it forms to substantially equal heights on vertical surfaces, such as sidewalls 534 and 536 of gate electrode 530 as well as on horizontal surfaces, such as on the top 526 of silicon film 520 and the top of gate electrode 530. In an embodiment of the present invention, the dielectric film is a silicon nitride film formed by a hot wall low-pressure chemical vapor deposition (LPCVD) process. The deposited thickness of the dielectric film determines the width or thickness of the formed spacers. In an embodiment of the present invention, the dielectric film is formed to a thickness between 20-200Å.

Next, as shown in Figure 5G, the dielectric film is anisotropically etched by for example plasma etching or reactive ion etching to form sidewall spacers 550. The anisotropic etch of dielectric film removes the dielectric film from horizontal surfaces, such as the top of gate electrode 530 (as well as the top of landing pads 522 and 524 if used) and leaves dielectric sidewall spacers adjacent to vertical surfaces, such as sidewalls 534 and 536 of gate electrode 530. The etch is continued for a sufficient period of time to

remove the dielectric film from all horizontal surfaces. In an embodiment of the present invention, an over etch is utilized so that the spacer material on the sidewalls of the semiconductor bodies 520 is removed as shown in Figure 5G. The result is the formation of sidewall spacers 550 which run along and adjacent to sidewall 532 and 534 of gate electrode 530 as shown in Figure 5H.

Next, if desired, a semiconductor film 560 can be formed on the exposed surfaces of semiconductor body 520 (as well as on landing pads 522 and 524) as shown in Figure 5H. Additionally, if desired, a semiconductor film 562 can be formed on the top of gate electrode 530. The semiconductor film can be a single crystalline film or a polycrystalline film. In an embodiment of present invention, semiconductor film 560 is an epitaxial (single crystalline) silicon film. In an embodiment of the present invention, the silicon film 560 is formed by a selective deposition process whereby silicon is formed only on exposed regions which contain silicon, such as the exposed top surface 527 and sidewalls 528 and 529 of silicon body 520. In a selective deposition process the silicon film does not form on dielectric areas, such as sidewall spacers 555. When gate electrode 530 comprises a polycrystalline silicon film, silicon film would also selectively form on the top surface of gate electrode 530 to form silicon film 562. In an embodiment of present invention, a silicon film 560 is formed to a thickness between 50-500Å. In an embodiment of the present invention, the silicon film is formed to a thickness sufficient to provide enough silicon to be used or consumed during the formation of a silicide film on the source and drain regions. The silicon film can be insitu doped (i.e., doped during deposition) or subsequently doped by for example ion-implantation or solid source diffusion. The silicon film is doped to the conductivity type desired for the source and drain regions of the device. In an embodiment of the present invention, the deposited silicon film 560 and 562 are intrinsic silicon films (i.e., undoped silicon films). The deposition of semiconductor film 560 forms raised source and drain regions which improves the parasitics of the device.

In an embodiment of the present invention, as shown in Figure 5I, the deposited silicon film 560 and 562 are doped by ion-implantation utilizing a vertical ion-implantation angle. The ion-implantation process dopes the deposited silicon film 560 and the silicon body 520 located underneath to a concentration between $1x10^{20}$-$1x10^{21}$ atoms/cm^3 to form a source contact region 570 and a drain contact region 572. Sidewall spacers 550 offset the source/drain contact implantation step and define the tips regions as a region of the doped silicon body beneath sidewall spacer 550. The above referenced process forms source regions 570 and drain regions 572 which each comprise a tip region and a contact region. The tip region is the region of the silicon body 520 located beneath sidewall spacers 555. The contact regions are the regions of the silicon body and deposited silicon film which are adjacent to the outside edges of the sidewall spacers 550. Additionally, the source/drain contact regions include the source and drain landing pads 522 and 524 when utilized.

Next, if desired, a refractory metal silicide 580 can be formed on the source and drain contact regions as well as on the top of gate electrode 530 (or silicon film 562) as shown in Figure 5J. A refractory metal silicide film 580 can be formed with a self-aligned process, such as a salicide process. In a salicide process a refractory metal film, such as titanium, tungsten, nickel, cobalt or alike to blanket deposited over the substrate of Figure 5J. The substrate is then heated to a suitable temperature to cause the refractory metal film to react with silicon portion of substrate 500, such as silicon film 560 formed on the silicon bodies and silicon film 562 formed on the gate electrodes in order to form a refractory metal silicide. Locations where silicon is unavailable to react, such as dielectric spacers 555 and exposed portions of buried oxide 506, do not react and remain as refractory metal. A selective etch, such as a wet etch can then be utilized to remove the unreacted refractory metal and leave the refractory metal silicide on the contact areas. In this way, a metal silicide film can be self-aligned to the contact regions of a tri-gate transistor. This completes the fabrication of a tri-gate transistor in accordance with the present invention.

Thus, tri-gate transistors and methods of fabrication have been described.

IN THE CLAIMS

We claim:

1. A semiconductor device comprising:

a semiconductor body having a top surface and laterally opposite sidewalls formed on a substrate film;

a gate dielectric formed on said top surface of said silicon body and on said laterally opposite sidewalls of said silicon body; and

a gate electrode formed on said gate dielectric on said top of surface of said semiconductor body and adjacent to said gate dielectric on said laterally opposite sidewalls of said silicon body.

2. The device of claim 1 wherein said semiconductor body is silicon.

3. The device of claim 1 wherein said semiconductor body is a single crystalline film.

4. The device of claim 2 wherein said semiconductor body is intrinsic single crystalline silicon.

5. The device of claim 1 wherein said semiconductor body is a semiconductor selected from the group consisting of silicon (Si) germanium (Ge), silicon germanium (Si_XGe_y), gallium arsenide (GaAs), InSb, GaP, GaSb as well as carbon nanotubes.

6. The semiconductor device of claim 1 wherein said substrate is an insulating substrate.

7. The semiconductor of claim 1 wherein said substrate is a semiconductor substrate.

8. A tri-gate transistor comprising:

a single crystalline silicon body formed on an insulating substrate, said silicon body having a top surface and first and second laterally opposite sidewalls;

a gate dielectric formed on said top surface of said silicon body and on said first and second laterally opposite sidewalls of said silicon body;

a gate electrode formed on said gate dielectric on said top surface of said silicon body and adjacent to said gate dielectric on said first and said second laterally opposite sidewalls of said silicon body; and

a pair of source/drain regions formed in said silicon body on opposite sides of said gate electrode.

9. The tri-gate transistor of claim 8 wherein said transistor has a gate length (Lg) approximately equal to the distance between said first and second laterally opposite sidewalls of said silicon body.

10. The tri-gate transistor of claim 8 wherein said transistor has a gate length (Lg) approximately equal to the distance from said insulating film to the top surface of said silicon body.

11. The tri-gate transistor of claim 8 wherein the distance between said laterally opposite sidewalls of said silicon body is approximately equal to the distance from said insulating substrate to the top surface of said silicon body.

12. The trigate transistor of claim 8 wherein the distance between said laterally opposite sidewalls of said semiconductor is between ½ to two times the thickness of said silicon body on said insulating surface.

13. The tri-gate transistor of claim 8 wherein said single crystalline silicon body is intrinsic silicon.

14. The tri-gate transistor of claim 8 wherein said single crystalline silicon body is doped to a first conductivity type with a concentration of between $1x10^{16}$- $1x10^{20}$ atoms/cm^3.

15. The tri-gate transistor of 14 wherein said single crystalline silicon body is doped to a first conductivity type with a concentration of $1x10^{16}$- $1x10^{18}$ atoms/cm^3.

16. The tri-gate transistor of claim 8 further comprising a pair of sidewall spacer formed along laterally opposite sidewalls of said gate electrode.

17. The tri-gate transistor of claim 8 wherein said pair of source/drain regions further comprise silicon formed on and around said silicon body.

18. The tri-gate transistor of claim 15 wherein said silicon on said source/drain regions is epitaxial silicon.

19. A transistor comprising:

a plurality of semiconductor bodies each having a top surface and a pair of laterally opposite sidewalls formed on a substrate film;

a gate dielectric formed on the top surface and sidewalls of each of said semiconductor bodies;

a gate electrode formed on the gate dielectric on the top surface of each of said plurality of semiconductor bodies and adjacent to said gate dielectrics formed on each of said first and second laterally opposite sidewalls of each of said silicon bodies; and

a pair of source/drain regions formed in each of said semiconductor bodies on opposite sides of said gate electrode.

20. The transistor of claim 19 wherein said gate width of said transistor is approximately the sum of the gate widths of each of said semiconductor bodies wherein the gate width of a semiconductor body is two times the height of the semiconductor body plus the distances between the laterally opposite sidewalls..

21. The tri-gate transistor of claim 19 wherein the distance between the laterally opposite sidewalls of each of said silicon bodies is approximately the same.

22. The transistor of claim 19 wherein each of said source regions are coupled together and each of said drain regions are coupled together.

23. The transistor of claim 19 wherein said substrate is an insulating substrate.

24. The transistor of claim 19 wherein said substrate is a semiconductor substrate.

25. A fully depleted semiconductor on insulator transistor comprising:

a silicon body formed on an insulating film;

a gate dielectric formed on and around said silicon body;

a gate electrode formed on said gate dielectric on and around said silicon body;

a pair of source/drain regions formed in said silicon body on opposite sides of said gate electrodes;

wherein said gate length of said transistor is less than or equal to the width of said silicon body; and

when said transistor is turned "ON" said silicon body between said source/drain regions is fully depleted

26. The transistor of claim 25 wherein said gate length is less than 60 nanometers

27. The transistor of claim 25 wherein said gate length is less than 30 nanometers.

28. The transistor of claim 25 wherein said gate length is less than 20 nanometers.

29. The transistor of claim 25 wherein said gate length is less than or equal to the height of said semiconductor body on said insulating film.

30. The transistor of claim 25 wherein said semiconductor body is a single crystalline silicon film.

31. The transistor of claim 30 wherein said single crystralline silicon film is intrinsic silicon.

32. A fully depleted silicon on insulator transistor comprising:

a silicon body formed on an insulating substrate;

a gate dielectric formed on and around said silicon body;

a gate electrode formed on and adjacent to said gate dielectric formed on and around said silicon body;

a pair of source/drain regions formed on opposite sides of said gate electrode in said silicon body; and

wherein said transistor has a very sharp sub-threshold slope of less than 80 mV/decade and a drain induced barrier lowering of less than 100 mV/V.

33. The transistor of claim 32 wherein said drain induced barrier lowering is less than 80 mV/V.

34. The transistor of claim 32 wherein said sub-threshold slope is about 60 mV/decade.

35. A method of forming a semiconductor device comprising:

forming a semiconductor body having a top surface and laterally opposite sidewalls on a substrate film;

forming a gate dielectric on said top surface of said semiconductor body and on said laterally opposite sidewalls of said semiconductor body; and

forming a gate electrode on said gate dielectric and adjacent to said gate dielectric on said laterally opposite sidewalls of said semiconductor body.

36. The device of claim 35 wherein said semiconductor body comprises single crystalline silicon.

37. The device of claim 36 wherein said single crystalline silicon body is intrinsic silicon.

38. The device of claim 35 wherein said semiconductor body is selected from the group consisting of silicon (Si) germanium (Ge), silicon germanium (Si_xGe_y), gallium arsenide (GaAs), InSb, GaP, GaSb as well as carbon nanotubes.

39. The method of forming the device of claim 35 wherein the thickness of said semiconductor body from said insulating film to said semiconductor body top surface is approximately equal to the distance between said laterally opposite sidewalls of said silicon body.

40. The method of claim 35 wherein the thickness of said silicon body from said insulating layer to said top surface is between two times to ½ the distance between the laterally opposite sidewalls.

41. The method of claim 35 wherein said substrate is an insulating substrate.

42. The method of claims 35 wherein said substrate is a semiconductor substrate.

43. A method of forming a silicon on insulator transistor comprising:

patterning a silicon film formed on an insulating substrate into a silicon body having a top surface opposite a bottom surface formed on said insulating film, and a first and second laterally opposite sidewalls;

forming a gate dielectric layer on said top surface of said silicon body and on said sidewalls of said silicon body;

depositing a gate material over said silicon body and over said insulating substrate;

patterning said gate material to form a gate electrode on said gate dielectric layer on said top surface of said silicon body and adjacent to said gate dielectric on said sidewalls of said silicon body, said gate electrode having laterally opposite sidewalls which run perpendicular to the laterally opposite sidewalls of said silicon body; and

forming a pair of source/drain regions in said silicon body on opposite sides of said laterally opposite sidewalls of said gate electrode.

44. The method of claim 43 wherein said distance between said laterally opposite sidewalls of said silicon body is approximately equal to the thickness of said silicon body on said insulating substrate.

45. The method of claim 43 wherein the distance between said laterally opposite sidewalls of said gate electrode (gate length) is less than or equal to the distance between laterally opposite sidewalls of said silicon body.

46. The method of claim 43 wherein the distance between said laterally opposite sidewalls of said gate electrode (gate length) is less than or equal to the thickness of said silicon body on said insulating film.

47. The method of claim 43 wherein said silicon film is single crystalline silicon.

48. The method of claim 47 wherein said single crystalline silicon film is intrinsic silicon.

49. The method of claim 43 further comprising forming a pair of sidewall spacers on opposite sides of laterally opposite sidewalls of said gate electrode; and

forming a silicon film on and around said silicon body and adjacent to said sidewall spacers.

50. The method of claim 43 further comprising forming a silicide on said silicon film formed on said silicon body.

51. The method of claim 43 wherein said silicon film is formed by a selective deposition process.