

Description

The invention relates to a digital-to-analog converter for converting a digital input signal having n-bits into an analog output current, comprising:

a reference-current source for supplying a reference current,

a reference transistor coupled to the reference current source,

a plurality of m first current source transistors for generating m output currents each in a given ratio to the current in the reference transistor,

a plurality of m first switching devices for switching the output currents of associated first current-source transistors to a summing point at which the analog output current is obtained or to a point of constant potential, depending on the value of a bit of the digital input signal applied to a respective switching input of the switching device.

Such a digital-to-analog converter is suitable for various purposes and may be used in particular for controlling the "radial" motor in a compact-disc player.

A digital-to-analog converter of this type is known from for example, United States Patent Specifications 3,940,760 and 3,961,326. In the converters described therein the output currents of the current-source transistors constitute a binary-weighted series of current which currents are each in a given ratio to the current from the reference transistor. This transistor receives a reference current from a reference-current source. By means of negative feedback between the collector and the base the base voltage is controlled in such a way that the collector current of the reference transistor is substantially equal to the reference current. The number of current-source transistors required depends on the ratio between the smallest and the largest current to be supplied to the digital-to-analog converter. The output currents of the current-source transistors are applied to the output of the digital-to-analog converter or drained to a point of fixed potential by means of switches which are controlled by the digital input code. The known converters can be used as a multiplying converter, by varying the reference voltage which determines the reference current. A disadvantage of this known digital-to-analog converter is that if it has to supply mainly comparatively small output currents, the output currents of the current-source transistors, which supply the comparatively large currents, are drained in the point of fixed potential, which results in a substantial power dissipation.

This situation occurs in, for example, a compact-disc player. In this player the laser unit by means of which a compact disc is read is mounted on an arm which is moved over the compact disc along a radial arc by means of a motor. The control current for this motor is supplied by a digital-to-analog converter. When the spiral track on a compact disc is read a relatively small control current is needed for this motor. However, for rapidly jumping from one

track to another track on the compact disc, the motor demands a comparatively large control current. Since normal tracking is the situation which occurs most frequently, the digital-to-analog converter has to supply only a small current for most of the time.

Therefore, it is the object of the invention to provide a digital-to-analog converter which has a smaller power dissipation than the known digital-to-analog converter for the same range of output currents.

According to the invention this object is solved by the fixtures indicated in claim 1.

The invention is based on the recognition of the following fact. Since the output currents of the current-source transistors are in a fixed ratio to the current in the reference transistor, these output currents are a similar fraction smaller when the current in the reference transistor is a fraction of the reference current than in the case when the reference transistor carries the full reference current. By increasing the current in the reference transistor stepwise over the entire range of the digital input code, the range of the output current of the digital-to-analog converter is also increased stepwise. As the current-source transistors only supply currents corresponding to a specific sub-range, the currents in the next higher sub-ranges need no long be generated and therefore need not be drained. Thus, the power dissipation is substantially reduced and the efficiency of the digital-to-analog converter is increased accordingly.

An embodiment of the invention is characterized in that for each step the control device comprises a second current-source transistor, whose base is coupled to the base of the reference transistor and whose current is in a given ratio to the current in the reference transistor, which control device further comprises a second switching device for each second current-source transistor, which switching device connects the associated second current-source transistor to the reference current source or to a point of fixed potential. If a second current-source transistor is coupled to the reference-current source it drains a part of the reference current, so that the current in the reference transistor is only a fraction of the reference current. By stepwise reducing the number of second current-source transistors coupled to the reference transistor, the current in the reference transistor increases stepwise to the full reference current.

If a second current-source transistor is not coupled to the reference-current source, its output current can be drained to the power supply. A further improvement of the efficiency of the digital-to-analog converter may be obtained if, in accordance with a further embodiment of the invention, it is characterized in that the second switching device of at least one second current-source transistor connects the relevant second current-source transistor to the reference-current source or to a first current-source transistor.

Embodiments of the invention will now be

described in more detail, by way of example, with reference to the accompanying drawings, in which:

Fig. 1 shows a digital-to-analog converter in accordance with a first embodiment of the invention;

Fig. 2 shows a digital-to-analog converter in accordance with a second embodiment of the invention, and

Fig. 3 shows a digital-to-analog converter in accordance with a third embodiment of the invention.

Fig. 1 shows an analog-to-digital converter in accordance with a first embodiment of the invention, by means of which the inventive principle will be explained. The digital-to-analog converter comprises a reference-current source 2, which supplies a reference current I_{ref} . A reference transistor T_1 has its emitter connected to the negative power-supply terminal 10. Between the collector and the base of the transistor T_1 negative feedback is provided by means of the base-emitter junction of a transistor T_2 , whose collector is connected to the positive power-supply terminal 20. By means of this negative feedback the base-emitter voltage of the transistor T_1 is controlled so as to make the collector current equal to the current I_1 applied to this transistor. The digital-to-analog converter further comprises a plurality of first current-source transistors T_3 , T_4 and T_5 , whose base-emitter paths are connected in parallel with the base-emitter path of the transistor T_1 . The emitter areas of these transistors are scaled in accordance with a binary series and the emitter area of the transistor T_3 is equal to that of the transistor T_1 . The currents I_3 , I_4 and I_5 from the transistors T_3 , T_4 and T_5 are then equal to I_1 , $2I_1$ and $4I_1$, respectively. The output current I_3 of the current-source transistor T_3 is applied to a switching device 3.1, which comprises two transistors $T_{6,1}$ and $T_{7,1}$, arranged as a differential pair. The collector of the transistor $T_{7,1}$ is connected to the output 15 of the digital-to-analog converter and the collector of the transistor $T_{6,1}$ is connected to the positive power-supply terminal 20. The current source transistors T_4 and T_5 are connected to the switches 3.2 and 3.3 respectively, comprising transistors $T_{6,2}$, $T_{7,2}$ and transistors $T_{6,3}$, $T_{7,3}$ in the same way as the switch 3.1. The bases of the transistors $T_{7,1}$, $T_{7,2}$ and $T_{7,3}$ are connected to a terminal 14, which is at a reference voltage. The bases of the transistors $T_{6,1}$, $T_{6,2}$ and $T_{6,3}$ are connected to the inputs 11, 12 and 13. The bits of the digital input signal are applied to these inputs. If the voltage on an input corresponding to the one bit value is higher than the reference voltage, on the terminal 14, the output current of the relevant current-source transistor is drained to the positive power-supply terminal 20, and, if the voltage corresponding to the other bit-value is smaller than the reference voltage on the terminal 14, the output current of the relevant current-source transistor is switched to the output of the digital-to-analog converter.

The digital-to-analog converter further com-

prises a control device 30, which comprises a second current-source transistor T_8 , whose base-emitter junction is connected in parallel with that of the transistor T_1 . The emitter area of the transistor T_8 is in a ratio of 7:1 to that of the transistor T_1 , so that the output current I_8 is equal to $7I_1$. The transistor T_8 is connected to a switch 4, which comprises a differential pair with transistors T_9 and T_{10} . The base of the transistor T_{10} is connected to the reference input 14 and the base of the transistor T_9 is connected to a control input 16 and the collector of transistor T_9 is connected to the positive power-supply terminal 20, and the collector of the transistor T_{10} is connected to the reference current source 2.

The circuit operates as follows. The control signal for the input 16 of the control device 30 is derived from the digital input word by means of a logic circuit, not shown. If the three most-significant bits of a digital input word are zero this logic circuit generates a control signal for the input 16, which control signal is low relative to the reference voltage on the base of the transistor T_{10} . In this case the three least significant bits of the digital input word are applied to the inputs 11 to 13. If one of the three most significant bits becomes one, the logic circuit generates a control signal for the input 16, which control signal is high relative to the reference voltage on the base of the transistor T_{10} . The three most significant bits of the digital input word are then applied to the inputs 11 to 13. If the control signal on the input 16 of the control device 30 is low relative to the reference voltage on the base of the transistor T_{10} , the collector of the transistor T_8 is connected to the reference-current source 2. The current $I_8=7I_1$ is then taken from the reference-current source 2, so that the reference transistor T_1 carries a current $I_1=1/8 I_{ref}$. The output currents of the current-source transistor T_3 , T_4 and T_5 are then $I_3=1/8 I_{ref}$, $I_4=2/8 I_{ref}$ and $I_5=4/8 I_{ref}$, respectively. The output current of the digital-to-analog converter can thus increase from 0 to $7/8 I_{ref}$ in steps of $1/8 I_{ref}$. If the control signal on the input 16 is high relative to the reference voltage on the base of the transistor T_{10} , the current I_8 is drained to the positive power-supply terminal 20 via the transistor T_9 . The reference transistor T_1 then carries a current $I_1=I_{ref}$. The output currents of the current-source transistors T_3 , T_4 and T_5 are then equal to $I_3=I_{ref}$, $I_4=2 I_{ref}$ and $I_5=4 I_{ref}$, respectively. The output current of the digital-to-analog converter can then increase from 0 to $7I_{ref}$ in steps of I_{ref} . As in the range from 0 to $7/8 I_{ref}$ the currents of the range from I_{ref} to $7 I_{ref}$ are not generated and are not dissipated without being used the efficiency is improved substantially.

A digital-to-analog converter in accordance with a second embodiment will be described with reference to Fig. 2, in which parts performing the same functions bear the same reference numerals as in Fig. 1. The converter differs from that in Fig. 1 in that the control device 30 comprises a second current-source transistor T_{11} , whose base-emitter junction is connected in parallel with that of the

transistor T_1 in addition to the current-source transistor T_8 . The emitter area of the transistor T_{11} is in a ratio of 56:1 to that of the transistor T_1 , so that the output current of this transistor is equal to $I_{11}=56 I_1$. By means of a switch 4 comprising the transistors T_{12} and T_{13} the transistor T_{11} can be connected to the positive power-supply terminal 20 if the voltage on the control input 17 is higher than the reference voltage on the base 14 of the transistor T_{13} and it can be connected to the reference current source 2 if the voltage on the control input 17 is lower than the reference voltage on the base 14. By means of this digital-to-analog converter the output current range is increased in three steps. If the current-source transistors T_8 and T_{11} are connected to the reference-current source 2 the current in the reference transistor T_1 will be $I_1=1/64 I_{ref}$. The output currents of the transistors T_3 , T_4 and T_5 are then $I_3=1/64 I_{ref}$, $I_4=2/64 I_{ref}$ and $I_5=4/64 I_{ref}$, respectively. The output current range of the converter then varies from 0 to $7/64 I_{ref}$ in steps of $1/64 I_{ref}$. If only the current-source transistor T_8 is connected to the reference-current source 2, the transistor T_1 will carry a current $I_1=1/8 I_{ref}$ and if the currents I_3 and I_{11} are both drained to the positive power-supply terminal 20, the current in the transistor T_1 will be $I_1=I_{ref}$. The output current range is then as described for the converter shown in Fig. 1.

A digital-to-analog converter in accordance with a third embodiment will now be described with reference to Fig. 3, in which parts performing the same functions bear the same reference numerals as in Fig. 1. The converter differs from that shown in Fig. 1 in that the current I_8 from the transistor T_8 is not transferred to the positive power-supply terminal 20 but to the output of the current source transistor T_3 via the transistor T_9 . If the current-source transistor T_8 is connected to the reference-current source 2 via the transistor T_{10} , the current in the reference transistor T_1 will be $I_1=1/8 I_{ref}$, so that the output current range of the converter again varies from 0 to $7/8 I_{ref}$ in steps of $1/8 I_{ref}$. If the current source transistor T_8 is connected to the transistor T_3 via the transistor T_9 the transistor T_1 will carry the full reference current I_{ref} . A total current of $8 I_{ref}$ will then be applied to the switch 3.1. The output current of the converter can then increase from $2 I_{ref}$ to $14 I_{ref}$ in steps of $2 I_{ref}$. As the current I_8 from the current source transistor T_8 is no longer drained to the positive power-supply terminal 20 if this transistor T_8 is not connected to the reference current transistor 2, the efficiency of the converter is increased even further.

The invention is not limited to the embodiments described above. For example, the ratio between the currents in the current-source transistor and the reference transistor can also be adjusted by means of resistors arranged in the emitter lines of these transistors. Alternatively, the emitters of the first current-source transistors may be connected to an R-2R network. Further, the switches by means of which the currents from the current-source transistors are switched may

be constructed in any other way. Moreover, the feedback between the collector and the base of the transistor T_1 by means of the transistor T_2 can also be obtained in another manner, for example by means of an operational amplifier.

Claims

1. A digital-to-analog converter for converting a digital input signal having n-bits into an analog output current, comprising:

a reference-current source (2) for supplying a reference current (I_{ref}),

a reference transistor (T_1) coupled to the reference current source,

a plurality of m first current source transistors (T_3 , T_4 , T_5) for generating m output current (I_3 , I_4 , I_5) each in a given ratio to the current in the reference transistor,

a plurality of a first switching (3.1, 3.2, 3.3) devices for switching the output currents (I_3 , I_4 , I_5) of associated first current-source transistors (T_3 , T_4 , T_5) to a summing point (15) at which the analog output current is obtained or to a point of constant potential (20), depending on the value of a bit of the digital input signal applied to a respective switching input (11, 12, 13) of the switching device,

characterized in that the digital-to-analog converter comprises a control device (30) for increasing the current through the reference transistor in a number of k steps from a fraction of to substantially the full reference current from the reference current source, between a first value of the digital input signal corresponding to the minimum analog output current, and a second value of the digital input signal corresponding to the maximum output current, that the number of said m first current source transistors being equal to $m=n/(k+1)$, and that for subsequent values of the current through the reference transistor each time m more-significant bits of the n-bits digital input signal are applied to the switching inputs of the switching devices.

2. A digital-to-analog converter as claimed in Claim 1, characterized in that for each step the control device comprises a second current-source transistor, whose base is coupled to the base of the reference transistor and whose current is in a given ratio to the current in the reference transistor, which control device further comprises a second switching device for each second current-source transistor, which switching device connects the associated second current-source transistor to the reference current source or to a point of fixed potential.

3. A digital-to-analog converter as claimed in Claim 2, characterized in that the second switching device of at least one second current-source transistor connects the relevant second current-source transistor to the reference current source or to one of the first current-source transistors.

transistor T_1 in addition to the current-source transistor T_8 . The emitter area of the transistor T_{11} is in a ratio of 56:1 to that of the transistor T_1 , so that the output current of this transistor is equal to $I_{11}=56 I_1$. By means of a switch 4 comprising the transistors T_{12} and T_{13} the transistor T_{11} can be connected to the positive power-supply terminal 20 if the voltage on the control input 17 is higher than the reference voltage on the base 14 of the transistor T_{13} and it can be connected to the reference current source 2 if the voltage on the control input 17 is lower than the reference voltage on the base 14. By means of this digital-to-analog converter the output current range is increased in three steps. If the current-source transistors T_8 and T_{11} are connected to the reference-current source 2 the current in the reference transistor T_1 will be $I_1=1/64 I_{ref}$. The output currents of the transistors T_3 , T_4 and T_5 are then $I_3=1/64 I_{ref}$, $I_4=2/64 I_{ref}$ and $I_5=4/64 I_{ref}$, respectively. The output current range of the converter then varies from 0 to $7/64 I_{ref}$ in steps of $1/64 I_{ref}$. If only the current-source transistor T_8 is connected to the reference-current source 2, the transistor T_1 will carry a current $I_1=1/8 I_{ref}$ and if the currents I_3 and I_{11} are both drained to the positive power-supply terminal 20, the current in the transistor T_1 will be $I_1=I_{ref}$. The output current range is then as described for the converter shown in Fig. 1.

A digital-to-analog converter in accordance with a third embodiment will now be described with reference to Fig. 3, in which parts performing the same functions bear the same reference numerals as in Fig. 1. The converter differs from that shown in Fig. 1 in that the current I_3 from the transistor T_8 is not transferred to the positive power-supply terminal 20 but to the output of the current source transistor T_3 via the transistor T_9 . If the current-source transistor T_8 is connected to the reference-current source 2 via the transistor T_{10} , the current in the reference transistor T_1 will be $I_1=1/8 I_{ref}$, so that the output current range of the converter again varies from 0 to $7/8 I_{ref}$ in steps of $1/8 I_{ref}$. If the current source transistor T_8 is connected to the transistor T_3 via the transistor T_9 the transistor T_1 will carry the full reference current I_{ref} . A total current of $8 I_{ref}$ will then be applied to the switch 3.1. The output current of the converter can then increase from $2 I_{ref}$ to $14 I_{ref}$ in steps of $2 I_{ref}$. As the current I_3 from the current source transistor T_8 is no longer drained to the positive power-supply terminal 20 if this transistor T_8 is not connected to the reference current transistor 2, the efficiency of the converter is increased even further.

The invention is not limited to the embodiments described above. For example, the ratio between the currents in the current-source transistor and the reference transistor can also be adjusted by means of resistors arranged in the emitter lines of these transistors. Alternatively, the emitters of the first current-source transistors may be connected to an R-2R network. Further, the switches by means of which the currents from the current-source transistors are switched may

be constructed in any other way. Moreover, the feedback between the collector and the base of the transistor T_1 by means of the transistor T_2 can also be obtained in another manner, for example by means of an operational amplifier.

Claims

1. A digital-to-analog converter for converting a digital input signal having n-bits into an analog output current, comprising:

a reference-current source (2) for supplying a reference current (I_{ref}),

a reference transistor (T_1) coupled to the reference current source,

a plurality of m first current source transistors (T_3 , T_4 , T_5) for generating m output current (I_3 , I_4 , I_5) each in a given ratio to the current in the reference transistor,

a plurality of a first switching (3.1, 3.2, 3.3) devices for switching the output currents (I_3 , I_4 , I_5) of associated first current-source transistors (T_3 , T_4 , T_5) to a summing point (15) at which the analog output current is obtained or to a point of constant potential (20), depending on the value of a bit of the digital input signal applied to a respective switching input (11, 12, 13) of the switching device,

characterized in that the digital-to-analog converter comprises a control device (30) for increasing the current through the reference transistor in a number of k steps from a fraction of to substantially the full reference current from the reference current source, between a first value of the digital input signal corresponding to the minimum analog output current, and a second value of the digital input signal corresponding to the maximum output current, that the number of said m first current source transistors being equal to $m=n/(k+1)$, and that for subsequent values of the current through the reference transistor each time m more-significant bits of the n-bits digital input signal are applied to the switching inputs of the switching devices.

2. A digital-to-analog converter as claimed in Claim 1, characterized in that for each step the control device comprises a second current-source transistor, whose base is coupled to the base of the reference transistor and whose current is in a given ratio to the current in the reference transistor, which control device further comprises a second switching device for each second current-source transistor, which switching device connects the associated second current-source transistor to the reference current source or to a point of fixed potential.

3. A digital-to-analog converter as claimed in Claim 2, characterized in that the second switching device of at least one second current-source transistor connects the relevant second current-source transistor to the reference current source or to one of the first current-source transistors.



Patentansprüche

1. Digital/Analog-Wandler zum Umsetzen eines digitalen Eingangssignals mit n Bits in einen analogen Ausgangsstrom, mit einer Referenzstromquelle (2) zum Liefern eines Referenzstroms (I_{ref}),

einem mit der Referenzstromquelle verbundenen Referenztransistor (T_1),

einer Anzahl von m ersten Stromquellentransistoren (T_3, T_4, T_5) zum Erzeugen von m Ausgangsströmen (I_3, I_4, I_5) in je einem bestimmten Verhältnis zum Strom im Referenztransistor,

einer Anzahl von m ersten Schaltkreisen (3.1, 3.2, 3.3) zum Durchschalten der Ausgangsströme (I_3, I_4, I_5) zugeordneter erster Stromquellentransistoren (T_3, T_4, T_5) nach einem Summierungspunkt (15), an dem der analoge Ausgangsstrom ankommt, oder nach einem Punkt mit konstantem Potential (20) in Abhängigkeit vom Wert eines Bits des an einen betreffenden Schalteingang (11, 12, 13) des Schaltkreises gelegten digitalen Eingangssignals,

dadurch gekennzeichnet, daß der Digital/Analog-Wandler einen Steuerkreis (30) zum Erhöhen des Stroms durch den Referenztransistor in einer Anzahl von k Schritten von einem Bruchteil des Referenzstroms bis zum im wesentlichen vollen Referenzstrom aus der Referenzstromquelle zwischen einem ersten Wert des digitalen Eingangssignals entsprechend dem minimalen analogen Ausgangsstrom und einem zweiten Wert des digitalen Eingangssignals entsprechend dem maximalen Ausgangsstrom enthält, daß die Anzahl der m ersten Stromquellentransistoren gleich $m = n/(k+1)$ ist, und daß für aufeinanderfolgende Werte des Stroms durch den Referenztransistor jedesmal m bedeutsamere Bits des n Bits digitalen Eingangssignals den Schalteingängen der Schaltkreise zugeführt werden.

2. Digital/Analog-Wandler nach Anspruch 1, dadurch gekennzeichnet, daß für jeden Schritt der Steuerkreis einen zweiten Stromquellentransistor enthält, dessen Basis mit der Basis des Referenztransistors verbunden ist und dessen Strom in einem bestimmten Verhältnis zum Strom des Referenztransistors steht, dieser Steuerkreis außerdem einen zweiten Schaltkreis für jeden zweiten Stromquellentransistor enthält, und dieser Schaltkreis den zugeordneten zweiten Stromquellentransistor mit der Referenzstromquelle oder mit einem Punkt mit festem Potential verbindet.

3. Digital/Analog-Wandler nach Anspruch 2, dadurch gekennzeichnet, daß der zweite Schaltkreis aus wenigstens einem zweiten Stromquellentransistor den betreffenden zweiten Stromquellentransistor mit der Referenzstromquelle oder mit einem der ersten Stromquellentransistoren verbindet.

Revendications

1. Convertisseur numérique-analogique pour

convertir un signal d'entrée numérique présentant n bits en un courant de sortie analogique, comportant:

une source de courant de référence (12) pour délivrer un courant de référence (I_{ref}),

un transistor de référence (T_1) couplé à la source de courant de référence,

une pluralité de m premiers transistors (T_3, T_4, T_5) montés en source de courant pour engendrer m courants de sortie (I_3, I_4, I_5) chacun dans un rapport déterminé avec le courant dans le transistor de référence,

une pluralité de m premiers dispositifs de commutation (3.1, 3.2, 3.3) pour la commutation des courants de sortie (I_3, I_4, I_5) des premiers transistors montés en source de courant associés (T_3, T_4, T_5) à un point de sommation (15) auquel s'obtient le courant de sortie analogique ou à un point de potentiel constant (20), suivant la valeur d'un bit du signal d'entrée numérique appliqué à une entrée de commutation respective (11, 12, 13) du dispositif de commutation,

caractérisé en ce que le convertisseur numérique-analogique comporte un dispositif de commande (30) pour augmenter le courant traversant le transistor de référence en un nombre de k pas d'une fraction à pratiquement tout le courant de référence provenant de la source de courant de référence, entre une première valeur du signal d'entrée numérique correspondant au courant de sortie analogique minimal et une deuxième valeur du signal d'entrée numérique correspondant au courant de sortie maximal, en ce que le nombre desdits m premiers transistors montés en source de courant est égal à $m = n/(k+1)$ et en ce que pour les valeurs suivantes du courant traversant le transistor de référence chaque fois m bits de poids plus fort du signal d'entrée numérique à n bits sont appliqués aux entrées de commutation des dispositifs de commutation.

2. Convertisseur numérique-analogique selon la revendication 1, caractérisé en ce que pour chaque étape, le dispositif de commande comporte un deuxième transistor monté en source de courant, dont la base est couplée à la base du transistor de référence et dont le courant est dans un rapport donné avec le courant dans le transistor de référence, lequel dispositif de commande comporte en outre un deuxième dispositif de commutation pour chaque deuxième transistor monté en source de courant, lequel dispositif de commutation assure la connexion du deuxième transistor monté en source de courant associé à la source de courant de référence ou à un point de potentiel fixe.

3. Convertisseur numérique-analogique selon la revendication 2, caractérisé en ce que le deuxième dispositif de commutation d'au moins un deuxième transistor monté en source de courant source la connexion du deuxième transistor monté en source de courant en question à la source de courant de référence ou à un premier transistor monté en source de courant.

