A VARIABLE POWER ADAPTIVE TRANSMITTER

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 60/773,033 filed on February 14, 2006, and U.S. Provisional Application No. 60/763,041, filed on January 27, 2006. The disclosures of the above applications are hereby incorporated by reference in their entirety.

FIELD OF THE INVENTION

[0002] The present invention relates to communication systems, and more particularly to transmitters in network interfaces and other devices.

BACKGROUND OF THE INVENTION

[0003] Referring now to Figure 1, an exemplary network 10 is shown to include one or more wireless network devices 20-1, 20-2, ..., and 20-X (collectively wireless network devices 20) and/or one or more wired network devices 24-1, 24-2, ..., and 24-Y (collectively wired network devices 24). The wireless network devices 20 wirelessly communicate data packets with an access point 30. The wired network devices 24 communicate data packets over cable, fiber or other media with a router 40. The access point 30 also communicates with the router 40. The router 40, in turn, communicates with a broadband modem 44, which communicates with a service provider 48. The

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service provider 48, in turn, provides access to a distributed communications network 50 such as the Internet.

[0004] Referring now to FIG. 2, an exemplary wireless network device 20 is shown. The wireless network device 20 typically includes a host 58 and a wireless network interface 60. The wireless network interface 60 typically includes a wireless physical layer device (PHY) 62, which includes a transceiver 64 including a transmitter 66 and a receiver 68. The wireless network interface 60 also includes a media access controller (MAC) 70 and/or other components (not shown).

[0005] Referring now to FIG. 3, an exemplary wired network device 24 is shown. The wired network device 24 typically includes a host 78 and a wired network interface 80. The wired network interface 80 typically includes a wired physical layer device (PHY) 82, which includes a transceiver 84 including a transmitter 86 and a receiver 88. The wireless network interface 60 also includes a media access controller (MAC) 90 and/or other components (not shown).

[0006] As described above, during use the transmitters 66 and 86 receive data that is to be transmitted on a respective medium. A supply voltage of the network interface may pose some limitations on the dynamic range of the transmitters 66 and 86 relative to voltage references that are used to supply the transmitter.

[0007] Referring now to FIGs. 4 and 5, the transmitters 66 and 86 in FIGs. 2 and 3 typically receive a supply voltage that can swing between $+V_s$ and $-V_s$. In this case, V_s is less than or equal to a supply voltage such as V_{dd}.

However, when a transmitter signal that is to be output by the transmitter 100 has an amplitude that is higher than the voltage swing of the supply voltage, clipping may occur, for example at 110 and 112 in FIG. 5. Increasing the supply voltage tends to reduce clipping. However, increasing the supply voltage also tends to increase the power dissipation of the device.

SUMMARY OF THE INVENTION

[0008] A circuit comprises a delay module that receives a digital transmit signal and that generates a delayed transmit signal. A first digital to analog converter converts the delayed transmit signal to an analog transmit signal. An analog output circuit amplifies the analog transmit signal. An envelope generating module generates an envelope signal based on amplitude information related to the digital transmit signal. A supply adjustment module supplies a voltage supply reference when the envelope signal is less than a threshold and boosts the bias voltage of the amplifier above the voltage supply reference when the envelope signal is greater than the threshold.

[0009] In other features, a second digital to analog converter converts the envelope signal to an analog envelope signal. The first digital to analog converter has a higher resolution than the second digital to analog converter. A third digital to analog converter receives the envelope signal and selectively boosts a bias current for the amplifier. The bias current increases when the envelope signal exceeds the threshold. The wireless network interface is compliant with at least one of IEEE section 802.11, 802.11a, 802.11b, 802.11g, 802.11h, 802.11n, 802.16, and 802.20.

[0010] A circuit comprises an analog output module that receives a bias signal and a control signal. A delay module receives a first signal and that generates a delayed first signal. A control module receives the delayed first signal and generates the control signal based thereon. An envelope generating module receives a second signal including amplitude information related to the first signal and generates an envelope signal that selectively increases the bias signal to the analog output module when the envelope signal exceeds a predetermined threshold and before a corresponding portion of the first signal is received by the analog output module.

[0011] In other features, the first signal includes a digital modulated carrier signal. A rectifier module that rectifies the digital modulated carrier signal and outputs the rectified modulated carrier signal to the envelope generating module. A digital to analog converter converts the envelope signal to an analog envelope signal. The envelope signal has a slower rise time than a fastest rise time of the first signal. The analog output module comprises a power amplifier. The control module includes a transmitter module.

[0012] In other features, a switch communicates with a first reference voltage and is controlled by the envelope generating module. A capacitance communicates with an output of the envelope generating module and the switch. An inductance communicates with the analog output module and the capacitance. A matching network communicates with the analog output module. An antenna communicates with the matching network. The envelope generating module receives the first signal and generates the envelope signal based on the

first signal. The delay circuit delays the modulated carrier signal. An upconverter upconverts the delayed modulated carrier signal.

[0013] A circuit comprises analog output means for receiving a bias signal and a control signal. Delay means receives a first signal and generates a delayed first signal. Control means receives the delayed first signal and generates the control signal based thereon. Envelope generating means receives a second signal including amplitude information related to the first signal and generates an envelope signal that selectively increases the bias signal to the analog output means when the envelope signal exceeds a predetermined threshold and before a corresponding portion of the first signal is received by the analog output means.

[0014] In other features, the first signal includes a digital modulated carrier signal. Rectifier means rectifies the digital modulated carrier signal and outputs the rectified digital modulated carrier signal to the envelope generating means. Digital to analog converting means converts the envelope signal to an analog envelope signal. The envelope signal has a slower rise time than a fastest rise time of the first signal. The analog output means comprises power amplifying means for amplifying. The control means includes transmitting means for transmitting. Switching means for switching communicates with a first reference voltage and is controlled by the envelope generating means. Capacitance means provides capacitance and communicates with an output of the envelope generating means and the switching means. Inductance means

provides inductance and communicates with the capacitance means and the analog output means.

[0015] In yet other features, matching network means for matching communicates with the analog output means. An antenna communicates with the matching network means. The envelope generating means receives the first signal and generates the envelope signal based on the first signal. The delay means delays the modulated carrier signal. An upconverting means upconverts the delayed modulated carrier signal.

[0016] A method comprises receiving a bias signal and a control signal at an analog output module; receiving and delaying a first signal; generating the control signal based on the delayed first signal; receiving a second signal including amplitude information related to the first signal; and generating an envelope signal based on the second signal that selectively increases the bias signal to the analog output module when the envelope signal exceeds a predetermined threshold and before a corresponding portion of the first signal is received by the analog output module.

[0017] In other features, the first signal includes a digital modulated carrier signal. The method includes rectifying the digital modulated carrier signal and outputting the rectified digital modulated carrier signal to the envelope generating module. The method includes converting the envelope signal to an analog envelope signal. The envelope signal has a slower rise time than a fastest rise time of the first signal. The method further includes generating the envelope signal based on the first signal. The method further includes delaying

the modulated carrier signal and upconverting the delayed modulated carrier signal.

[0018] Further areas of applicability of the present disclosure will become apparent from the detailed description provided hereinafter. It should be understood that the detailed description and specific examples, while indicating the preferred embodiment of the disclosure, are intended for purposes of illustration only and are not intended to limit the scope of the disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The present invention will become more fully understood from the detailed description and the accompanying drawings, wherein:

[0020] Figure 1 is functional block diagram of an exemplary wireless network according to the prior art;

[0021] Figure 2 is a functional block diagram of an exemplary wireless network device of FIG 1;

[0022] Figure 3 is a functional block diagram of an exemplary wired network device of FIG 1;

[0023] Figure 4 is a functional block diagram of a transmitter that is powered by a voltage source according to the prior art;

[0024] Figure 5 is an exemplary waveform of a wireless signal transmitted by the transmitter of FIG. 4;

[0025] Figure 6A and 6B are functional block diagrams of exemplary adaptive transmitters according to the present invention;

[0026] Figure 7A is an exemplary functional block diagram and electrical schematic of a supply adjustment module;

[0027] Figure 7B is an exemplary functional block diagram and electrical schematic of an assymetrical supply adjustment module;

[0028] Figure 7C is an exemplary functional block diagram and electrical schematic of a symmetrical supply adjustment module;

[0029] Figure 8A illustrates a symmetrical boosted waveform;

[0030] FIG. 8B illustrates the slower signal rise time of the envelope signal;

[0031] Figure 8C illustrates an asymmetrical boosted waveform;

[0032] Figure 9 is an exemplary functional block diagram of an exemplary RF amplifier with boosting;

[0033] FIG. 10A is a functional block diagram and electrical schematic of another exemplary adaptive transmitter;

[0034] FIG. 10B illustrates a rectified and boosted waveform;

[0035] Figure 11A is an exemplary implementation of the present invention in a network accessed storage module;

[0036] Figure 11B is an exemplary implementation of the present invention in a digital versatile disc drive;

[0037] Figure 11C is an exemplary implementation of the present invention in a high definition television;

[0038] Figure 11D is an exemplary implementation of the present invention in a wireless local area network device associated with a vehicle;

[0039] Figure 11E is an exemplary implementation of the present invention in a cellular phone;

[0040] Figure 11F is an exemplary implementation of the present invention in a set top box; and

[0041] Figure 11G is an exemplary implementation of the present invention in a media player.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0042] The following description is merely exemplary in nature and is in no way intended to limit the disclosure, its application, or uses. For purposes of clarity, the same reference numbers will be used in the drawings to identify similar elements. As used herein, the term module, circuit and/or device refers to an Application Specific Integrated Circuit (ASIC), an electronic circuit, a processor (shared, dedicated, or group) and memory that execute one or more software or firmware programs, a combinational logic circuit, and/or other suitable components that provide the described functionality. As used herein, the phrase at least one of A, B, and C should be construed to mean a logical (A or B or C), using a non-exclusive logical or. It should be understood that steps within a method may be executed in different order without altering the principles of the present disclosure.

[0043] Referring now to FIGs. 6A and 6B, adaptive transmitters 150-1 and 150-2 (collectively adaptive transmitters 150) according to the present invention are shown. Components of the adaptive transmitter 150 receive a

voltage reference V_s. Unlike conventional systems, the voltage reference V_s can temporarily be greater than the supply voltage V_{dd}. Therefore, some components within the transmitter can be temporarily driven higher than the voltage reference V_{dd} to avoid clipping and increase dynamic range while maintaining relatively low power dissipation.

[0044] In FIG. 6A, the adaptive transmitter 150-1 includes a digital signal processor (DSP) 152 that outputs a transmit signal that is to be transmitted. A delay module 154 delays the transmit signal by a predetermined delay and/or a variable delay that can be adjusted. A digital to analog converter 158 converts the delayed transmit signal to an analog transmit signal. The analog transmit signal is output to an analog output circuit such as an amplifier 162, which amplifies the analog transmit signal. While an amplifier is shown, any analog output circuit that requires a bias voltage can be used.

[0045] A boost module 164 receives the transmit signal (or amplitude information related to the transmit signal) and selectively increases voltage V_s supplied to the amplifier and/or any other analog output circuit above a threshold such as the voltage supply level V_{dd} when the analog transmit signal exceeds the voltage supply level or any other threshold. In contrast to causal systems, the voltage boost to the amplifier 162 occurs before the amplifier 162 receives the corresponding transmit signal that exceeded the threshold. Therefore, clipping can be avoided unlike in causal systems where clipping may be reduced but not avoided. The envelope signal has also may have a rise time that is slower than the fastest rise time of the transmit signal.

[0046] The boost module 164 comprises an envelope module 170, a digital to analog converter 172 and a supply adjustment module 174. The transmit signal may be output to an envelope module 170. The envelope module 170 generates an envelope signal that is based on the transmit signal. The envelope signal tracks positive and/or negative peaks of the transmit signal at a lower bandwidth. The envelope signal is output to a digital to analog converter 172, which converts the envelope signal to an analog signal. The analog signal from the digital to analog converter 172 is output to a supply adjustment module 174. The supply adjustment module 174 generates a variable voltage supply or bias for the amplifier 162.

[0047] When the envelope signal is less than the threshold signal, the supply adjustment module 174 supplies $V_s = V_{dd}$. When the envelope signal is greater than the threshold signal, the supply adjustment module 174 temporarily boosts V_s above V_{dd}. The boost voltage V_{Boost} allows the amplifier in the transmitter to track the transmit signal without clipping the transmit signal. The delay provided by the delay module 154 allows the supply adjustment module 174 to generate the additional voltage required to boost V_s above V_{dd}. The digital to analog converter 158 may have a higher resolution and/or bandwidth than the digital to analog converter 172.

[0048] As can be appreciated, the envelope signal generator does not need to receive the same signal as the delay module 154 and D/A converter 158 as shown in FIG. 6A. For example, the digital signal processor 152 can output amplitude information related to the digital signal to the envelope signal

generator and the transmit signal (including additional information) to the delay module 154 and D/A converter 158. Other types of signals may be used as well.

[0049] Referring now to FIGs. 7A-7C and 8A-8C, an exemplary supply adjustment module 174 is shown to include a switch S_{Boost} and a boost capacitor C_{Boost} that receives a boost voltage from the digital to analog converter 172. When the envelope signal is less than the threshold signal, the switch S_{Boost} is closed and the supply adjustment module 174 supplies $V_s = V_{dd}$. When the envelope signal is greater than the threshold signal, the switch S_{Boost} is opened and the supply adjustment module 174 supplies $V_s = V_{dd} + V_{Boost}$. Energy stored in the capacitor C_{Boost} will supply bias voltages and/or current to the amplifier and/or other analog output circuits. In FIG. 8A, the boost voltage temporarily increases the voltage supplied (V_s) above V_{dd} and reduces or prevents clipping of the transmitter signal.

[0050] In FIG. 7B, the digital signal is output to positive and negative envelope generating modules 176 and 177, which generate positive and negative envelope signals, respectively. Outputs of the positive and negative envelope generating modules 176 and 177 are input to digital to analog converters (DACs) 178 and 179, respectively. Outputs of the DACs 178 and 179 communicate with positive and negative boost capacitors C_{boost+} and C_{boost-}, respectively. Switches 181-1 and 181-2 are operated as described above to selectively bias an amplifier 180 with V_{dd} or a boost voltage.

[0051] In FIG. 7C, the digital signal is fed to a rectifier 182 (or absolute value circuit) that rectifies the signal. If used, the absolute value circuit may

selectively change sign bits to provide an absolute value. An envelope module outputs positive and negative envelope signals to DACs 184 and 185, respectively. Outputs of the DACs 184 and 185 communicate with positive and negative boost capacitors C_{boost+} and C_{boost-}, respectively. Switches 186-1 and 186-2 are operated as described above to selectively bias an amplifier 187 with V_{dd} or a boost voltage.

[0052] The circuit in FIG. 7B generates a symmetrical boosted waveform that is shown in FIG. 8A. In FIGs. 8A and 8B, the transmitter signal 190 has a higher bandwidth than the envelope signal 192. The envelope signal 192 anticipates the transmitter signal 190. In other words, the envelope signal 192 does not merely follow the increase of the transmitter signal 190 as would be the case for traditional peak envelope detector signals generally illustrated at 188. Rather, the envelope signal 192 begins to increase in anticipation of the increase in the transmitter signal 190 and may have a higher amplitude than the traditional peak envelope detector signal. Furthermore, the bandwidth of the envelope signal 192 is lower than the bandwidth of the transmitter signal 190. In other words, a rise time of the envelope signal 192 is greater than a fastest rise time of the transmitter signal 190. Stated another way, a slope 197 of the envelope signal in FIG. 8A will be less than a slope 196 of a corresponding (and delayed) portion of the transmitter signal 190. Using an envelope signal having a faster response or a step response (such as the one shown at 199 in FIG. 8B) may tend to cause high frequency noise.

[0053] In FIG. 8C, an asymmetrical waveform that can be generated by the circuit in FIG. 7C is shown. The boost that is generated is different for positive and negative portions of the signal. Therefore, the positive and negative bias voltages for the differential amplifier may also be different.

[0054] Referring now to FIG. 9, an adaptive transmitter 200 can be implemented in an RF amplifier for a wireless transmitter. Components of the adaptive transmitter 200 receive a voltage supply V_{dd}. Some components within the transmitter, however, can be temporarily driven higher than the voltage supply V_{dd}. A digital transmit modulator 202 outputs the transmit signal to the delay module 154 and to a rectifier 201 (or absolute value module), which outputs the rectified digital signal to the envelope module 170. The digital to analog converter 158 converts the delayed transmit signal to an analog transmit signal. The analog transmit signal is output to an upconverter 204 that upconverts the signal. The upconverted signal is output the amplifier 162, which amplifies the signal.

[0055] The envelope module 170 generates an envelope signal that is based on the transmit signal and/or a threshold signal. The envelope signal is output to a digital to analog converter 172, which converts the envelope signal to an analog signal. The analog signal from the digital to analog converter 172 is output to a supply adjustment module 174. The supply adjustment module 174 generates a variable voltage supply for the amplifier 162.

[0056] When the envelope signal is less than the threshold signal, the supply adjustment module 174 supplies $V_s = V_{dd}$. When the envelope signal is

greater than the threshold signal, the supply adjustment module 174 temporarily boosts V_s above V_{dd}. The delay provided by the delay module 154 allows the supply adjustment module 174 to generate the additional voltage required to boost V_s above V_{dd}. A digital to analog converter 208 also receives the envelope signal and generates an RF bias current. The bias current selectively biases the amplifier 162. The bias current may be provided at the same time that the boost voltage is provided and/or may continually provide an adaptive bias current to the amplifier 162. A bias adjustment module 210 adjusts an RF bias current to the amplifier based on the envelope signal.

[0057] Suitable applications include wireless network devices and wired network devices. The network devices can be VDSL or VDSL2 compliant. The wireless network devices can be compliant with IEEE standards 802.11, 802.11a, 802.11b, 802.11g, 802.11h, 802.11n, 802.16, and 802.20 and/or with Bluetooth and cellular phones, for example those that are compliant with GSM 4G.

[0058] Referring now to FIGs. 10A-10B, a transmitter circuit 240 includes a digital signal processor (DSP) 242 that generates a first signal containing amplitude information and a modulated carrier signal. A rectifier 244 (or absolute value circuit) rectifies the signal and outputs the signal to an envelope generator module 246, which generates an envelope signal as described above. A DAC 250 converts the envelope signal to an analog envelope signal and generates a boost voltage V_{Boost} across a capacitor C_{Boost}. The envelope generator module 246 also generates a control signal that

selectively opens and closes a switch 258, which is connected to V_{dd}. The switch is operated as described above.

[0059] A delay module 255 receives the modulated carrier signal and generates a delayed modulated carrier signal. An upconverter module 256 upconverts the delayed signal. A transmitter 257 generates a control signal for a control terminal of a power amplifier 264 based on the delayed modulated carrier signal. An inductance 260 may be connected between the boost capacitor C_{boost} and a first terminal of the power amplifier 264. A matching network 266 is coupled to the first terminal and to an antenna 268. In FIG. 10B, the digital transmit signal is rectified (for example at 300) and an analog envelope signal is generated as shown. The voltage bias to the amplifier selectively increases above V_{dd} as needed to prevent clipping.

[0060] Referring now to Figures. 11A-11G, various exemplary implementations of the present invention are shown. Referring now to Figure 11A, the present invention can be implemented in a network accessed storage module (NAS) 901 that includes a hard disk drive 900. The present invention may implement and/or be implemented in a wireless network interface module, which is generally identified in Figure 11A at 904. In some implementations, signal processing and/or control circuit 902 and/or other circuits (not shown) in the HDD 900 may process data, communicate with the module 904, perform coding and/or encryption, perform calculations, and/or format data that is output to and/or received from a magnetic storage medium 906.

[0061] The HDD 900 may communicate with another networked device (not shown) such as a computer, a mobile computing device such as a personal digital assistant, cellular phone, media or MP3 player and the like, and/or other device via one or more wired links 908 and/or the module 904. The HDD 900 may be connected to memory 909 such as random access memory (RAM), low latency nonvolatile memory such as flash memory, read only memory (ROM) and/or other suitable electronic data storage. The HDD 900 may also include a power supply module 903.

[0062] Referring now to Figure 11B, the present invention can be implemented in a digital versatile disc (DVD) drive 910. The present invention may implement and/or be implemented in wireless network interface module, which is generally identified in Figure 11B at 911. Signal processing and/or control circuit 912 and/or other circuits (not shown) in the DVD drive 910 may process data, perform coding and/or encryption, perform calculations, and/or format data that is read from and/or data written to an optical storage medium 916. In some implementations, the signal processing and/or control circuit 912 and/or other circuits (not shown) in the DVD drive 910 can also perform other functions such as encoding and/or decoding and/or any other signal processing functions associated with a DVD drive.

[0063] The DVD drive 910 may communicate with an output device (not shown) such as a computer, television or other device via one or more wired links 917 and/or wireless links via the module 911. The DVD drive 910 may communicate with mass data storage 918 that stores data in a nonvolatile

manner. The mass data storage 918 may include a hard disk drive (HDD). The HDD may have the configuration shown in Figure 11A. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The DVD drive 910 may be connected to memory 919 such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. The DVD drive 910 may also include a power supply 913.

[0064] Referring now to Figure 11C, the present invention can be implemented in a high definition television (HDTV) 920. The present invention may implement and/or be implemented in either or both signal processing and/or control circuits, which are generally identified in Figure 11E at 922, and a wireless network interface module 929.

[0065] The HDTV 920 receives HDTV input signals in either a wired or wireless format and generates HDTV output signals for a display 926. In some implementations, signal processing circuit and/or control circuit 922 and/or other circuits (not shown) of the HDTV 920 may process data, perform coding and/or encryption, perform calculations, format data and/or perform any other type of HDTV processing that may be required.

[0066] The HDTV 920 may communicate with mass data storage 927 that stores data in a nonvolatile manner such as optical and/or magnetic storage devices. At least one HDD may have the configuration shown in Figure 11A and/or at least one DVD may have the configuration shown in Figure 11B. The HDD may be a mini HDD that includes one or more platters having a diameter

that is smaller than approximately 1.8". The HDTV 920 may be connected to memory 928 such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. The HDTV 920 also may include a power supply 923.

[0067] Referring now to Figure 11D, the present invention may implement and/or be implemented in a wireless network interface module 948 of a vehicle 930. A powertrain control system 932 receives inputs from one or more sensors such as temperature sensors, pressure sensors, rotational sensors, airflow sensors and/or any other suitable sensors and/or that generates one or more output control signals such as engine operating parameters, transmission operating parameters, and/or other control signals.

[0068] The control system 940 may likewise receive signals from input sensors 942 and/or output control signals to one or more output devices 944. In some implementations, the control system 940 may be part of an anti-lock braking system (ABS), a navigation system, a telematics system, a vehicle telematics system, a lane departure system, an adaptive cruise control system, a vehicle entertainment system such as a stereo, DVD, compact disc and the like. Still other implementations are contemplated.

[0069] The powertrain control system 932 may communicate with mass data storage 946 that stores data in a nonvolatile manner. The mass data storage 946 may include optical and/or magnetic storage devices for example hard disk drives HDD and/or DVDs. At least one HDD may have the configuration shown in Figure 11A and/or at least one DVD may have the

configuration shown in Figure 11B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The powertrain control system 932 may be connected to memory 947 such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. Vehicle 930 may also include a power supply 933.

[0070] Referring now to Figure 11E, the present invention can be implemented in a cellular phone 950 that may include a cellular antenna 951. The present invention may implement and/or be implemented in a wireless network interface module 968. In some implementations, the cellular phone 950 includes a microphone 956, an audio output 958 such as a speaker and/or audio output jack, a display 960 and/or an input device 962 such as a keypad, pointing device, voice actuation and/or other input device. The signal processing and/or control circuits 952 and/or other circuits (not shown) in the cellular phone 950 may process data, perform coding and/or encryption, perform calculations, format data and/or perform other cellular phone functions.

[0071] The cellular phone 950 may communicate with mass data storage 964 that stores data in a nonvolatile manner such as optical and/or magnetic storage devices for example hard disk drives HDD and/or DVDs. At least one HDD may have the configuration shown in Figure 11A and/or at least one DVD may have the configuration shown in Figure 11B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The cellular phone 950 may be connected to memory

966 such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. Cellular phone 950 may also include a power supply 953.

[0072] Referring now to Figure 11F, the present invention can be implemented in a set top box 980. The present invention may implement and/or be implemented in a network interface module 996. The set top box 980 receives signals from a source such as a broadband source and outputs standard and/or high definition audio/video signals suitable for a display 988 such as a television and/or monitor and/or other video and/or audio output devices. The source may be connected to the set top box 980 via the network interface module 996. The signal processing and/or control circuits 984 and/or other circuits (not shown) of the set top box 980 may process data, perform coding and/or encryption, perform calculations, format data and/or perform any other set top box function.

[0073] The set top box 980 may communicate with mass data storage 990 that stores data in a nonvolatile manner. The mass data storage 990 may include optical and/or magnetic storage devices for example hard disk drives HDD and/or DVDs. At least one HDD may have the configuration shown in Figure 11A and/or at least one DVD may have the configuration shown in Figure 11B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The set top box 980 may be connected to memory 994 such as RAM, ROM, low latency nonvolatile memory

such as flash memory and/or other suitable electronic data storage. Set top box 980 may also include a power supply 983.

[0074] Referring now to Figure 11G, the present invention can be implemented in a media player 1000. The present invention may implement and/or be implemented in a wireless network interface 1016. In some implementations, the media player 1000 includes a display 1007 and/or a user input 1008 such as a keypad, touchpad and the like. In some implementations, the media player 1000 may employ a graphical user interface (GUI) that typically employs menus, drop down menus, icons and/or a point-and-click interface via the display 1007 and/or user input 1008. The media player 1000 further includes an audio output 1009 such as a speaker and/or audio output jack. The signal processing and/or control circuits 1004 and/or other circuits (not shown) of the media player 1000 may process data, perform coding and/or encryption, perform calculations, format data and/or perform any other media player function.

[0075] The media player 1000 may communicate with mass data storage 1010 that stores data such as compressed audio and/or video content in a nonvolatile manner. In some implementations, the compressed audio files include files that are compliant with MP3 format or other suitable compressed audio and/or video formats. The mass data storage may include optical and/or magnetic storage devices for example hard disk drives HDD and/or DVDs. At least one HDD may have the configuration shown in Figure 11A and/or at least one DVD may have the configuration shown in Figure 11B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller

than approximately 1.8". The media player 1000 may be connected to memory 514 such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. Media player 1000 may also include a power supply 1013. Still other implementations in addition to those described above are contemplated.

[0076] While an amplifier 162 is shown, any analog output circuit that requires a bias voltage and/or current can be used. The present invention saves power by generally lowering the required supply voltage while selectively increasing the supply voltage as needed. As a result, the dynamic range of the circuit is improved without significantly increasing power dissipation.

[0077] Those skilled in the art can now appreciate from the foregoing description that the broad teachings of the present invention can be implemented in a variety of forms. Therefore, while this invention has been described in connection with particular examples thereof, the true scope of the invention should not be so limited since other modifications will become apparent to the skilled practitioner upon a study of the drawings, the specification and the following claims.

CLAIMS

1. A circuit comprising:

a delay module that receives a digital transmit signal and that generates a delayed transmit signal;

a first digital to analog converter that converts said delayed transmit signal to an analog transmit signal;

an analog output circuit that receives said analog transmit signal;

an envelope generating module that generates an envelope signal based on amplitude information related to said digital transmit signal; and

a supply adjustment module that supplies a voltage supply reference when said envelope signal is less than a threshold and that boosts said bias voltage of said analog output circuit above said voltage supply reference when said envelope signal is greater than said threshold.

2. The circuit of Claim 1 further comprising a second digital to analog converter that converts said envelope signal to an analog envelope signal, wherein said first digital to analog converter has a higher resolution than said second digital to analog converter.

3. The circuit of Claim 2 further comprising a third digital to analog converter that receives said envelope signal and generates a third signal and that selectively boosts a bias current for said analog output circuit based on said third signal.

4. The circuit of Claim 3 wherein said bias current increases when said envelope signal exceeds said threshold.

5. A wired network interface comprising the circuit of Claim 1.

6. A wireless network interface comprising the circuit of Claim 1.

7. The wireless network interface of Claim 6 wherein said wireless network interface is compliant with at least one of IEEE section 802.11, 802.11a, 802.11b, 802.11g, 802.11h, 802.11n, 802.16, and 802.20.

8. The circuit of Claim 1 wherein said envelope generating module receives said digital transmit signal and generates said envelope signal based on said digital transmit signal.

9. The circuit of Claim 1 wherein a rise time of said envelope signal is slower than a fastest rise time of said analog transmit signal.

10. The circuit of Claim 1 wherein said threshold is substantially equal to a reference voltage supply level of said circuit.

11. A circuit comprising:

a delay module that receives a digital transmit signal and that generates a delayed transmit signal;

a first digital to analog converter that converts said delayed transmit signal to an analog transmit signal;

an analog output circuit that receives said analog transmit signal;

a supply boost module that samples a signal including amplitude information of said digital transmit signal and that selectively boosts a voltage reference supplied to said analog output circuit before a corresponding portion of said analog transmit signal is received by said analog output circuit based on a difference between said sampled signal and a threshold.

12. The circuit of Claim 11 wherein said supply boost module includes:

an envelope generating module that generates an envelope signal;

a second digital to analog converter that converts said envelope signal to an analog envelope signal; and

a supply adjustment module that supplies a voltage supply reference when said envelope signal is less than said threshold and that boosts said bias voltage of said analog output circuit above said voltage supply reference when said envelope signal exceeds said threshold.

13. The circuit of Claim 12 wherein said first digital to analog converter has a higher resolution than said second digital to analog converter.

14. The circuit of Claim 12 further comprising a third digital to analog converter that receives said envelope signal and that generates a bias current for said analog output circuit.

15. The circuit of Claim 14 wherein said bias current increases when said envelope signal exceeds said threshold.

16. A wired network interface comprising the circuit of Claim 12.

17. A wireless network interface comprising the circuit of Claim 12.

18. The wireless network interface of Claim 17 wherein said wireless network interface is compliant with at least one of IEEE section 802.11, 802.11a, 802.11b, 802.11g, 802.11h, 802.11n, 802.16, and 802.20.

19. The circuit of Claim 12 wherein said envelope generating module receives said digital transmit signal and generates said envelope signal based on said digital transmit signal.

20. The circuit of Claim 12 wherein said envelope signal has a rise time that is slower than a fastest rise time of said analog transmit signal.