

STRUCTURE OF INTERFACE PORTION OF TEST FIXTURE

Technical field

5 The present invention is related to a structure of an interface portion of a test fixture provided on a test head of a semiconductor test system for forming an interface between a device to be tested and the test system and for transmitting signals between a performance board mounted on the test head and a socket board mounted on a test handler on
10 which the device to be tested is mounted.

Background Art

An example of the conventional technology is explained with reference to Figures 4-6 as follows.

15 First, the outline of the semi-conductor test system using the test handler is explained.

As shown in Figure 4, an example of the semi-conductor test system is comprised of a work station 90, a semiconductor test system main frame 70, a test head 71 and a
20 test handler 80.

The work station 90 connected to the semiconductor test system main frame 70 is an engineering work station functioning as an interface with an operator.

25 The semiconductor test system main frame 70 is comprised of a test processor for controlling an overall whole system including peripheral devices, various kinds of units for generating test signals and measuring the test results, an electric power source for supplying electric power with various voltages.

30 The transmission route from the semiconductor test system main frame 70 to the electronic circuits stored in the test head 71 is formed by a connecting cable and the test signals are transmitted therethrough.

35 The test signals from the electronic circuits stored in the test head 71 are transmitted to the performance board 62



mounted on the test head 71.

The test signals on the performance board 62 are transmitted to a plurality of IC sockets 11 which are mounted on a socket board 10 by electrically connecting the performance board 62 to the socket board 10 through a test fixture 100.

Conversely, output signals from the IC sockets 11 are transmitted to the semiconductor test system main frame through the transmission route in the direction opposite to the above route.

The test fixture 100 can be removed and replaced depending on the types of the performance board 62 and the socket board 10.

The test handler 80 is an automatic handling machine for automatically conveying the devices to be tested to the plurality of IC sockets 11 mounted on the socket board 10, inserting the device to be tested in the socket board, thereafter picking the device from the IC sockets, classifying the device in accordance with the result of the test and conveying the devices to the storage places.

Generally, in the test handler 80, the side of the socket board 10 having the IC sockets is placed in a constant temperature chamber so that the devices to be tested can be tested at a predetermined high or low temperature.

Under the system configuration of the semiconductor test system described in the foregoing, automatic testing of the devices under test is conducted.

Next, description will be made regarding the test fixture 100 for transmitting signals between the performance board 62 mounted on the test head 71 and the socket board 10.

The signals are transmitted between the performance board 62 and the socket board 10 mainly through a connect board 40.

Generally, the configuration of connection between the performance board 62 and the connect board 40 is the same as that between the socket board 10 and the connect board 40.



Hence, mainly the configuration of connection between the socket board 10 and the connect board 40 as shown in Figures 5 and 6 is explained in the following.

As shown in Figures 5 and 6, in the conventional technology, pin sockets 60 having contact pieces inside are pressed in the socket board 10.

In this event, since the pin socket 60 is longer than the thickness of the socket board 10, an end of the pin socket 60 is protruding beyond the surface of the socket board 10 by about 1mm.

The reason of having this configuration is that in order to improve the high frequency characteristics when transmitting the signals therebetween, the distance between the test fixture 100 and the IC sockets needs to be minimized, and therefore the thickness of the socket board 10 has to be small.

At each end of the connect board 40, a pin 61 and a pin header 50 molded by plastics and the like for supporting the pin 61 are provided.

The pin header 50 is fixed to a pad 44 on the connect board 40 by soldering.

Signal patterns 43 which function as the transmission route of the signals and an inner layer GND pattern 45 form a strip line therebetween, thereby establishing characteristic impedance of, for instance, 50 ohm.

A round pattern 41 is connected to an inner ground layer pattern 45 by a through hole 42.

On the other hand, the pad 44 provided at an end of the connect board 40 is connected to the pad at the other end of the connect board 40 through the signal pattern 43.

The pin headers 50 are provided at both ends of the connect board 40.

Similarly, although not shown in the drawings, another end of the connect board 40 is electrically connected to the performance board 62 through the pin header 50.

Under the above configuration, signals are transmitted



between the performance board 62 and the socket board 10 through the test fixture 100.

At the time the signals from the connect board 40 pass through the pin 61, due to the mismatching in characteristic impedance at the pin header 50, the wave form of the signals would be distorted.

For this reason, transmission of high frequency signals are conducted directly from the performance board 62 to the socket board 10 through a coaxial cable with two pin terminals by soldering the two terminals.

In the conventional technology, the transmission of signals between the performance board 62 and the socket board 10 has been conducted through the test fixture 100 as explained in the foregoing.

The above noted conventional technology causes the following problems in its practical use.

(A) when transmitting the high frequency signals between the performance board 62 on the test head 71 and the socket board 10 on the test handler 80, it is not possible to match the characteristic impedance at the pin header 50. As a result, if the test signal has to be transmitted at high speed, distortion of wave form of the test signal is occurred due to the reflection of transmitting signals.

(B) Since the pin socket 60 has an inner contact lead, it is difficult to decrease the outer diameter of the pin socket 60. Therefore, pitch of the array of the pin socket 60 is limited, and thus it is difficult to increase the mounting density.

(C) In order to conduct temperature testing, the side of the IC sockets 11 mounted on the socket board 10 must be kept at a constant temperature. However, due to the thermal conduction from the pin sockets 60, good heat insulation characteristic is not available.

(D) Since a socket guide which functions as a guide member is provided on the IC sockets 11 mounted on the socket board 10 for inserting the device to be tested in the sockets



or taking out the device therefrom, it is preferable that the socket board 10 have fewer protrusions thereon.

If the thickness of the socket board 10 is increased in order to eliminate the protrusions on the socket board 10, 5 the distance between the IC sockets 11 and the test fixture 100 will increase, resulting in problems for transmitting high frequency signals, such as an increase in capacitance.

The conventional technology have the problems in the practical use as stated in (A)-(D) above. Therefore, the 10 present invention is made to solve these problems. It is an object of the present invention to provide a structure of an interface portion of a test fixture wherein test signals of high frequency can be transmitted therethrough without distortion, a pin array of a high mounting density can be 15 achieved, heat at the side of the IC sockets of the socket board is not easily transferred by thermal conduction, and a surface of the socket board at the side of the IC sockets 11 is formed flat.

20 Disclosure of the Invention

A first aspect of the present invention, which is made to achieve the above objects, is a structure of an interface portion of a test fixture provided on a test head of a semiconductor test system for transmitting signals between a 25 performance board which interfaces a device to be tested and a socket board mounted on a test handler for inserting the device to be tested in a socket or taking out therefrom, characterized in that:

a plurality of surface mount connectors 20 mounted on a 30 socket board 10 only on a side opposite to an IC socket mounted side;

a connect board 40 for transmitting signals from an end of the connect board to another end thereof; and

connectors 30 attached to an end of the connect board 40 35 and fitted with each of the surface mount connectors 20 while maintaining impedance matching in characteristic impedance



therebetween.

A second aspect of the present invention, which is made to achieve the above objects, is a structure of an interface portion of a test fixture provided on a test head of a semiconductor test system for transmitting signals between a performance board which interfaces a device to be tested and a socket board mounted on a test handler for inserting the device to be tested in a socket or taking out therefrom, characterized in that:

10 a plurality of surface mount connectors 20 mounted on a socket board 10 only on a side opposite to an IC socket mounted side, and further mounted on a surface of the performance board 62;

a connect board 40 for transmitting signals from an end of the board to another end; and

15 a plurality of connectors 30 attached to an end of the connect board 40 and further attached to another end of the connect board 40 and fitted with each of the surface mount connectors 20 of the socket board 10 or the performance board 20 62 while maintaining impedance matching of characteristic impedance therebetween.

Brief Description of the Drawings

Figure 1 is a cross sectional view of the signal transmission portion of the test fixture at the socket board side thereof according to the present invention.

Figure 2 is a cross sectional view of the ground portion of the test fixture at the socket board side according to the present invention.

30 Figure 3 is a partial top view of the test fixture at the socket board side thereof according to the present invention.

Figure 4 is a block diagram showing a semiconductor test system.

35 Figure 5 is a cross sectional view of the test fixture at the socket board side thereof in the conventional



technology.

Figure 6 is a cross sectional view of the conventional test fixture of Figure 5 taken along the line A-A.

5 Best Mode for Carrying Out the Invention

With reference to Figures 1-3, an embodiment of the present invention is explained in the following.

As shown in Figures 1 and 2, in the structure of the interface portion of a test fixture 100, the socket board 10
10 is provided with a surface mount connector 20.

A connector 30 attached to the connect board 40 is provided at a fitting portion of the test fixture 100 with the surface mount connector 20.

Alternatively, a coaxial cable connected with the
15 connector 30 may be provided at the fitting portion of the test fixture 100 with the surface mount connector 20.

Although not shown in the drawings, the configuration of the test fixture 100 at the side of the performance board 62 may be similarly configured by providing a surface mount
20 connector 20 on the performance board 62 and providing a connector 30 attached to the connect board 40.

Alternatively, as a structure of the test fixture 100 at the side of the performance board 62, a coaxial cable may be directly attached to the performance board 62 by soldering.

25 Further, the test fixture 100 at the side of the performance board 62 may be electrically connected to the test head 71 through a board (a mother board, for instance) having a multi-layer structure.

As described above, the signals are transmitted between
30 the socket board 10 and the performance board 62 through the interface portion of the test fixture 100.

Next, each of the components is explained.

The surface mount connector 20 is a connector with which the connector 30 is fitted and electrically connected.

35 As to the kinds of the surface mount connector 20, different kinds of connector may be used between a signal pin



21 and a GND (ground) pin 24 which can be mounted on the surface of the socket board 10.

For example, the signal pin 21 is formed of 36 pins and the GND pin 24 is formed of 4 pins.

5 Both ends of the connect board 40, the connector 30 is fixed to the connect board by attaching a signal contact 31 to a signal pattern 43 and a GND contact 32 to the GND pattern 41 by soldering.

10 The connector 30 has the structure wherein an insulating body is sandwiched between the signal contact 31 and the GND contact 32. Namely, it has the structure like that of a strip line.

15 Namely, like the characteristic impedance of the signal pattern 43 of the connect board 40, the characteristic impedance between the signal contact 31 and the GND contact 32 is matched to 50 ohm.

20 Therefore, owing to the matching in the characteristic impedance, the transmission of high frequency signals between the connect board 40 and the socket board 10 and between the connect board 40 and the performance board 62 becomes possible.

25 Further, since the surface mount connector 20 is mounted only on the surface opposite to the side where the IC sockets 11 are mounted thereon, there are no protrusions at the IC sockets 11 side of the socket board 10.

Therefore, because there are no protrusions at the IC sockets 11 side of the socket board 10, socket guides for guiding a device to be tested being inserted or taken out can be done smoothly.

30 Further, since no pin sockets are used, the thermal conduction from the IC sockets side of the socket board 10 to the surface mount connector 20 side thereof is reduced.

35 In addition, since the surface mount connector 20 is of a small size, the pitch of the signal pins 21 can be easily reduced and thus the packaging density can be increased.

For instance, while the pitch of the conventional pin



socket 60 is 2.54mm, the pitch of the signal pins 21 of the surface mount connector 20 can be decreased to a range about 0.8mm to 0.5mm.

5 As explained above, conventionally, a transmission route for signals have been formed by directly connecting the performance board 62 to the socket board 10 through a coaxial cable with two pin terminals by soldering the two pin terminals. The present invention makes it possible to form the transmission route without using the coaxial cable by
10 transmitting high frequency signals through the interface portion of the test fixture of the embodiment of the present invention.

Further, by eliminating the soldered coaxial cable, separation or replacement of the test fixture 100 and the
15 socket board 10 can be easily conducted by merely removing the attachment of the surface mount connector.

Industrial Applicability

The present invention is embodied in the manner as
20 described above and has the following effects.

The present invention solves all of the problems of the conventional technology listed in (A)-(D).

Namely, since the characteristic impedance between the connect board and the socket board is matched by the surface
25 mount connector and the characteristic impedance between the connect board and the performance board is also matched, transmission of high frequency signals becomes possible.

Further, signals of high density can be transmitted by using the surface mount connector.

30 Further, the heat at the IC socket 11 side of the socket board is prevented from conducting to the connect board side thereof.

Further, since protrusions are eliminated from the IC socket 11 side of the socket board to form a flat face, the
35 socket guide for guiding the device to be tested when inserting and pulling out can be done smoothly without any



disruption.

As described above, the structure of the interface
portion of the test fixture according to the present
invention has a substantial advantage, when used in
5 combination with the semiconductor test system and the test
handler, for testing the device under test which operates at
high frequency signals with high accuracy.

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WHAT IS CLAIMED IS:

1. A structure of an interface portion of a test fixture provided on a test head of a semiconductor test system for transmitting signals between a performance board which interfaces a device to be tested and a socket board mounted on a test handler for inserting the device to be tested in a socket or taking out therefrom, comprising:

a plurality of surface mount connectors 20 mounted on a socket board 10 only on a side opposite to an IC socket mounted side;

a connect board 40 for transmitting signals from an end of the connect board to another end thereof; and

connectors 30 attached to an end of the connect board 40 and fitted with each of the surface mount connectors 20 while maintaining impedance matching in characteristic impedance therebetween.

2. A structure of an interface portion of a test fixture provided on a test head of a semi-conductor test system for transmitting signals between a performance board which interfaces a device to be tested and a socket board mounted on a test handler for inserting the device to be tested in a socket or taking out therefrom, comprising:

a plurality of surface mount connectors 20 mounted on a socket board 10 only on a side opposite to an IC socket mounted side, and further mounted on a surface of the performance board 62;

a connect board 40 for transmitting signals from an end of the board to another end; and

a plurality of connectors 30 attached to an end of the connect board 40 and further attached to another end of the connect board 40 and fitted with each of the surface mount connectors 20 of the socket board 10 or the performance board 62 while maintaining impedance matching of characteristic impedance therebetween.

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