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METHOD FOR FLIP-CHIP BONDING

The present invention relates to a method of producing an electrically conducting connection between a chip with multiple contact elements or contact surfaces and a substrate (flip-chip mounting), especially by means of application of ultrasonic energy to connect a chip with a substrate with the electrically conductive connection between the contact elements of the flip-chip and the corresponding contact elements/contact surfaces of the substrate directly as ultrasonic weld bonds. The invention relates further to the chip and the substrate with which the method has been used.

In flip-chip bonding, the contact elements on the contact surfaces or the bond paths have a typical height of 15 μm to 75μm and are produced in the form of stud bumps, solder bumps or by the "plating process." For the ultrasonic flip-chip bonding primarily stud bumps and contact elements in accordance with the "plate process" are used. The space or gap remaining after the bonding between the substrate and the silicon for the chip amounts usually to 50% to 70% of the starting gap dimension. So that forces between the substrate and the chip, which can arise because of the different thermal expansion coefficients of the substrate and the chip ("thermal mismatch") can be taken up (the shear stress would otherwise loosen the chip from the

substrate), it is known to introduce with a very fine needle between the chip and the substrate an additional adhesive subsequent to the bonding to increase the mechanical stability of the entire assembly. This process is characterized as underfilling or underfill.

Especially with very small distances between the chip and substrate and a small space (pitch) between the individual contact elements, this underfill process can no longer be used since the remaining gap does not allow a homogeneous underfilling with adhesive.

The object of the invention is to provide a chip construction or substrate construction and a method of making it, with which a secure fastening between the chip and carrier substrate can be achieved and whereby the "underfill" process step can be eliminated.

This object is achieved in that on the side of the chip turned toward the substrate, between the contact elements and especially on the free chip surface and/or on the side of the substrate turned toward the chip between the contact surface and especially the residual surfaces which are covered by the chip, at least regionally, a bonding material is provided.

The objects are further achieved in that by means of the bonding material between the contact elements of the flip-chip and/or between the contact areas of the substrate, a further bond between the substrate and the flip-chip is produced.

The bonding material thus serves to produce a reliable bond between the chip and the substrate withstanding the shear stresses so as to insure that with thermal loading of the assembly, a release of the chip or a breaking of the electrical contacts is avoided.

The bonding material can in one embodiment be preferably nonconducting and has independently from this requirement characteristics which allow the bonding material to function for example as an adhesive, especially a two component adhesive or also as an ultrasonic weld material, for example, an ultrasonically weldable plastic. In another embodiment the bonding material can be electrically conductive and an electrically conductive bond can be formed between the chip or the electrical circuitry provided thereon and the substrate (for example surfaces for ground and voltage supply).

The bonding material can be supplementarily applied to the above-mentioned surface of a chip or a substrate, preferably simultaneously with the fabrication process for the chip or the substrate. This can be done by conventional process steps during the fabrication of the chip or substrate, for example, by a lithographic process, by means of the thin layer technique, the etching technique or another fabrication method known to the artisan.

The special advantage of such a construction in which a bonding material is applied to one or the other element (chip/substrate) before the bonding itself lies in that the

bonding material is already located between the two elements to be bonded at the time bonding is required and thus does not have to be underfilled between the bond partners. In addition, the spacing between the contact elements or between the chip and the substrate can be as small as desired. The method step of underfilling is then eliminated along with the cost so that the cycling time can be reduced.

Aside from the alternative whereby the bonding material is applied to the substrate prior to the bonding, preferably the bonding, material prior to bonding is also applied to the side of the flip-chip which is turned toward the substrate on bonding. Ideally, the bonding material is provided on the chip at the time of manufacture.

The bonding material can be so applied that its height over the chip base surface is slightly less than the heights of the contact elements of the chip. The height can amount to, for example, 5 to 9 micrometers when the contact elements have heights of at least 15 micrometers. This has the advantage that during the bonding process steps, initially, the end surfaces of the contact elements of the chip will come into contact with the corresponding contact surfaces of the substrate so that initially there is a concentration of the ultrasonic energy on these parts.

The reduced height of the bonding material by comparison to the contact elements of the chip can also be realized when the bonding material is applied to the substrate rather than the flip-chip according to the first alternative. In

this case, the bonding material on the substrate can project beyond the contact pads and especially can have a height which is less than the height of the contact elements of the chip applied to the substrate to achieve the above mentioned advantage.

By applying a pressing force and an ultrasonic excitation, an electric connection can then be produced between the flip-chip and substrate, whereby the contact elements deform and are pressed together. This reduces the spacing between the flip-chip and the substrate so that then the bonding material will first contact the substrate or a further bonding material layer on the substrate.

It can be provided that already during the contact a solid bond can be effected between the flip-chip and the substrate, for example, by an adhesive effect between the bonding material and the substrate or by an adhesive effect between the respective bonding material on the chip and the substrate which can form a two component adhesive.

Alternatively, it can be provided that a reliable connection between the chip and substrate is obtained first after an ultrasonic welding of the bonding material with the juxtaposed partner element (substrate, chip or further bonding material). In this case the complete bonding process is, for example, two staged, whereby in the first stage, the electrically conductive ultrasonic bonding between contact elements and surfaces [pads] is produced and then the additional bonding is brought about. It is possible to carry out the two stages simultaneously.

With the sequence of the welding in stages which follow one another in time, it can be provided that the welding of the bonding material is effected with other welding parameters, especially at other ultrasonic frequencies and/or with other pressures than the welding of the contact elements. Thus for each process step the optimum welding parameters can be chosen.

In a further feature of the invention, it can be provided that the bonding material, whether applied on the chip or the substrate, has recesses in the material, especially in the form of channels or grooves. These recesses or channels/grooves serve to take up material, for example, whether of the contact elements or for example of the bonding material which is pressed out during the bonding. This pressed out material finds place in the recesses/channels without creating false electrical connections.

The bonding material can be applied area-wide or also only at point locations between the contact elements (chip) or contact pads (substrate). With an area-wide arrangement it is preferably that the contact material surround the contact elements or contact surfaces especially with a clearance.

Because of the presence of the preferred spacing, again a region or channel is formed which surrounds the contact surface or contact element and thus serves to receive material of the contact element or the bonding material in a stress free and force free manner upon the pressing or deformation during bonding. These regions/channels can also form an insulation

between the contact elements/contact surfaces and the bonding material, especially when the bonding material is formed as an electrically conductive material so as to avoid undesirable short circuiting between the contact elements/surfaces and the bonding material.

Especially in an alternative configuration of the bonding material as an electrically conductive material, it is possible using the bonding material in a very simple manner to provide at least in regions a surface electric connection between the substrate and chip or the electronic circuitry thereon. Such a surface connection with multiple independent contacts can, for example, be used to supply one or more supply voltages or also a ground potential. In this manner the known requirements, precisely for high power chips which require a number of contact elements to be supplied with voltage or ground, can be satisfied.

Such conductive bonding materials to create electric connections between the chip and substrate can be applied in optional patterns to the chip or substrate, for example, it can extend as a meandering connection between the contact elements and surfaces.

Furthermore, the contact elements or surfaces of the chip or substrate can be replaced by the bonding material especially where the electric contacts are prepared for voltage supply and the application of a ground potential.

An embodiment of the invention is illustrated in the accompanying drawing. It shows:

FIG. 1: a plan view of the underside of a flip-chip.

FIG. 2: a sectional side elevation of a flip-chip.

FIGS. 1 and 2 show that, as a replacement for the underfill between the chip one and a substrate which has not been illustrated, a bonding material 2, for example an ultrasonically weldable synthetic resin is used especially in the bond region between the contact elements 3 (bond pads).

Alternatively thereto an adhesive, especially a two component adhesive, can be used which is applied to both bonding partners in a bone-dry manner [so that dust will not adhere thereto] and whose adhesive effect is first initiated when both sides are brought into contact, i.e. when the metallic contact elements 3 are correspondingly deformed. The bonding material can also be an ultrasonic weldable plastic coating which can be used as the last mask in the wafer process.

In the present embodiment, the bonding material 2 is applied over a wide area between the contact elements 3. Between the contact elements 3 and the bonding material 2, intervening spaces 4 or channels 4 are left so that, upon welding with ultrasound, place for deformed material both of the contact elements 3 and also of the bonding material 2 remains and which upon welding is plastically deformed and laterally spread.

It is advantageous when, in the fabrication of the wafer additional material as the bonding material 2 is applied by the "plating" so that the "underfill" process step is superfluous and the mechanical stability of the bond between the chip and

substrate is achieved either by the effect of the ultrasound or through a chemical process and which, after producing the electrically conductive connection, that is after deformation of the contact element, results in a full surface contact.

With ultrasonic welding, initially the electrical contacts are formed and then the adhesive bonding with welding as a consequence of the fact that the adhesive material 2 has a lesser height than the contact elements 3. In the invention it is further provided that upon producing the electrical contacts and than the additional bonding, different ultrasound energies and/or ultrasound frequencies can be used. By contrast with the use of anisotropic conductive adhesives, the process of the invention has the advantage that the bond is lower ohmic since no randomly oriented silver particles are required as current tracks but the bonding material can provide a direct contact between the chip and substrate.

In addition, the method of the invention can be used for small contact spacings or pitches whereas with anisotropic conductive adhesive, smallest mean path lengths must be maintained in order to insure insulation.

PATENT CLAIMS:

1. A chip/substrate (1) with multiple contact elements/surfaces (3) for producing an electrically conductive connection between a chip (1) and a substrate, especially by means of ultrasonic welding, characterized in that on the side of the chip/substrate (1) turn toward the substrate/chip, between the contact elements/surfaces (3) at least over regions a bonding material (2), especially one which is arranged ultrasonically.

2. A chip or substrate according to claim 1 characterized in that the height of the bonding material is less than the height of the contact elements (3) of the chip (1).

3. A chip or substrate according to one of the preceding claims characterized in that the bonding material (2) has recesses (4), especially in the form of channels and/or grooves (4).

4. A chip or substrate according one of the preceding claims characterized in that the bonding material (2) surrounds a contact element (3)/a contact surface, especially at a distance.

5. A chip or substrate according to claim 4 characterized in that a spacing between the bonding material (2)

and the contact element (3)/surface a channel (4)/ a groove is formed which surrounds the contact element (3)/the contact surface and especially insulates it against the bonding material.

6. A chip or substrate according to one of the preceding claims characterized in that the bonding material (2) is weldable by means of ultrasound and especially at least regionally forms an area-wide electrically nonconducting or conducting between chip and substrate.

7. A chip or substrate according to one of the preceding claims characterized in that the bonding material (2) is an adhesive, especially whereby the chip (1) and the substrate each have a part of a two-component adhesive (2) on the surface facing the other.

8. A method of connecting a chip (1), especially according to one of the preceding claims, with a substrate, in which between the contact elements (3) of the chip (1) and the corresponding contact elements (3)/contact surfaces of the substrate an ultrasonic weld connection is produced, characterized in that by means of a bonding material (2) provided between the contact elements (3) of the chip (1) and/or between the contact surfaces of a substrate a further bond is formed between the substrate and the chip (1).

9. The method according to claim 8 characterized in that the additional bond is effected by an ultrasonic welding of the bonding material (2) with the chip (1)/substrate.

10. The method according to one of the preceding claims, characterized in that the welding of the bonding material (2) is carried out with other welding parameters, especially with another welding frequency and/or pressure, than the welding of the contact elements (3).

11. The method according to one of the preceding claims, characterized in that during the welding and/or adhesion, material of the bonding material (2) and/or the contact element material (3) is pressed into gaps (4) in the material or into channels/grooves (4).

12. The method according to one of the preceding claims, characterized in that by means of the bonding material (2) an at least area-wide surface conducting bond is produced between the chip and substrate.