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STRUCTURE AND METHOD OF APPLYING STRESSES TO PFET AND NFET TRANSISTOR CHANNELS FOR IMPROVED PERFORMANCE

BACKGROUND OF THE INVENTION

The present invention relates to the fabrication of semiconductor integrated circuits, and more specifically to an apparatus and method of making strained channel complementary metal oxide semiconductor (CMOS) transistors.

Both theoretical and empirical studies have demonstrated that carrier mobility in a transistor can be greatly increased when a stress of sufficient magnitude is applied to the conduction channel of a transistor to create a strain therein. Stress is defined as force per unit area. Strain is a dimensionless quantity defined as the unit change, for example a percentage change, in a particular dimension of an item, in relation to the initial dimension of that item. An example of strain is the change in length versus the original length, when a force is applied in the direction of that dimension of the item: for example in the direction of its length. Strain can be either tensile or compressive. In p-type field effect transistors, the application of a compressive longitudinal stress, i.e. in the direction of the length of the conduction channel, creates a strain in the conduction channel which is known to increase the drive current of a PFET. However, if the same compressive stress is applied to the conduction channel of an NFET, its drive current



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decreases. However, when a tensile stress is applied to the conduction channel of an n-type field effect transistor (NFET), the drive current of the NFET increases.

Accordingly, it has been proposed to increase the performance of an NFET by applying a tensile longitudinal stress to the conduction channel of the NFET, while increasing the performance of a PFET by applying a compressive longitudinal stress to its conduction channel. Several ways have been proposed to impart different kinds of stresses to different regions of a wafer that house NFET and PFET transistors. In one example, mechanical stress is manipulated by altering the materials in shallow trench isolation regions (STIs) disposed adjacent to the conduction channels of FETs to apply a desired stress thereto. Other proposals have centered on modulating intrinsic stresses present in spacer features. Yet other proposals have focused on introducing etch-stop layers such as those that include silicon nitride.

SUMMARY OF THE INVENTION

According to an aspect of the invention, a semiconductor device structure is provided which includes a first semiconductor device; a second semiconductor device; and a unitary stressed film disposed over both the first and second semiconductor devices. The stressed film has a first portion overlying the first semiconductor device, the first portion imparting a first

magnitude compressive stress to a conduction channel of the first semiconductor device, the stressed film further having a second portion overlying the second semiconductor device, the second portion not imparting the first magnitude compressive stress to a conduction channel of the second semiconductor device, the second portion including an ion concentration not present in the second portion such that the second portion imparts one of a compressive stress having a magnitude much lower than the first magnitude, zero stress, and a tensile stress to the conduction channel of the second semiconductor device.

In one embodiment, the first and second semiconductor devices include a p-type field effect transistor (PFET) and an n-type field effect transistor (NFET), respectively. In a preferred embodiment, a second stressed film is disposed over the first stressed film and overlying both the PFET and the NFET. An intermediate layer is provided overlying the PFET between the first and the second stressed films but not overlying the NFET. The second stressed film imparts a tensile stress to the conduction channel of the NFET, but not to that of the PFET, because of the intervening intermediate layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a structure including a PFET and an NFET according to an embodiment of the invention.

Figure 2A through 10 illustrate stages in fabrication of a PFET and an NFET according to an embodiment of the invention.

DETAILED DESCRIPTION

Figure 1 is a cross-sectional view illustrating one embodiment of the present invention. As shown in Figure 1, a single-crystal semiconductor region 14 is illustrated in which two semiconductor devices are provided, such as NFET 10 and PFET 20 of complementary metal oxide semiconductor (CMOS) circuitry. The NFET and PFET are separated by shallow trench isolation (STI) region 50. As discussed earlier, an appropriate stress applied to a transistor channel region can significantly increase carrier mobility, resulting in improved performance. As shown in Figure 1, a unitary stressed film 900 is disposed over both the PFET 20 and the NFET 10 to impart stresses to each transistor.

In the exemplary structure shown in FIG. 1, the unitary stressed film 900 includes two portions, a first portion 901 that imparts a compressive stress having a first magnitude to the conduction channel 91 of the PFET 20 and a second portion 902 that overlies the NFET 10. Although the second portion 902 is part of the same unitary stressed film 900 as the first portion 901, the second portion does not impart a compressive stress at the first magnitude to the conduction channel 92 of the NFET 10. This is because the

second portion 902 includes an ion concentration which is not present in the first portion. The ion concentration causes the second portion 902 to have a different magnitude of stress, or even a different type of stress, i.e., a tensile stress. The second portion 902 has either a compressive stress having a magnitude much lower than the first magnitude, zero stress, or a tensile stress. By way of example, in one embodiment of the invention, the unitary stressed film 900 consists essentially of a nitride such as silicon nitride and the ion concentration in the second portion includes germanium (Ge) ions.

In a preferred embodiment, illustrated in Figure 1, a second stressed film 990 is disposed over the first portion 901 and the second portion 902 of the unitary stressed film. The second stressed film 990 is a tensile stressed film, imparting a tensile stress to the conduction channel of the NFET 10. Thus, the second stressed film is disposed over both the compressive stressed first portion 901 and over the second portion 902 of stressed film 900. In order that the tensile stressed second film 990 does not affect the compressive stress applied to the PFET by the underlying compressive stressed first portion 901, an intermediate layer 550 is disposed over the PFET 20 to space the second film at a sufficient distance from the compressive stressed portion 901 of the underlying unitary stressed film. The intermediate layer 550 is disposed on the first stressed film 900 but only overlying the PFET 20 and not the overlying NFET 10.

The second stressed film 990 can be formed of a variety of

materials. In a preferred embodiment, the second stressed film 990 consists essentially of a nitride, such as silicon nitride. In one embodiment, the intermediate layer 550 has a thickness measuring between 100 Å and 300 Å and includes a conformal dielectric material, the layer 550 preferably including an oxide such as silicon dioxide.

The structure further includes a dielectric fill 1000 and conductive vias 1100 contacting silicide regions 32 overlying the source and drain regions 24 of the NFET 10 and the PFET 20 and conductive vias 1102 contacting silicide regions 28 of the gate conductors of the NFET and the PFET.

Thus, in the structure illustrated, permanent tensile and compressive stresses are applied to the NFET and the PFET, respectively, to improve the performance of each. A high level of stress can be applied because both tensile and compressive stresses are applied to localized regions of the wafer in which the NFET and the PFET are disposed.

The magnitudes of the stresses applied to each region can be controlled by the film thickness and characteristics of an ion implantation, as will be discussed later. An advantage of the structure 12 is that the topography of the wafer is more even between the regions of the wafer in which the PFET and NFETs are formed. This results because limited processes, such as reactive ion etch (RIE) processes, are applied to the

structure to form the stressed films, and a relatively thin layer of oxide is used as an intermediate layer between the stressed films.

The NFET 10 and PFET 20 shown in Figure 1 are formed from a substrate 16. The substrate 16 may either be a bulk substrate or, more preferably, a semiconductor-on-insulator substrate, such as a silicon-on-insulator (SOI) substrate, in which a relatively thin single-crystal semiconductor region 14 of a semiconductor is formed over an insulating layer 18, as shown. When field effect transistors (FETs) are formed in such SOI substrates, faster switching operation is often achieved than otherwise, because junction capacitance between the channel region of the transistor and the bulk substrate is eliminated. Preferably, a single-crystal semiconductor region 14 of silicon is provided as the semiconductor-on-insulator layer.

Reference is made herein to NFET and PFET transistors having channel regions disposed within a single-crystal silicon region of a substrate. However, the present invention is not limited to the fabrication of transistors in a pure silicon crystal. In place of silicon, the single crystal semiconductor region 14 may consist essentially of a semiconductor alloy such as that of silicon germanium. The teachings of the present invention are also understood to apply to the fabrication of transistors in other types of semiconductor materials such as III-V compound semiconductors having a composition $Al_AIn_BGa_CAs_DP_EN_F$, wherein A, B, C, D, E and F represent the

respective percentages of each element Al, In, Ga, As, P and N in the semiconductor crystal, the percentages totaling 100. Gallium arsenide (GaAs), indium phosphide (InP), gallium nitride (GaN), and InGaAsP are common examples of such semiconductors.

With continued reference to Figure 1, the gate conductors of the NFET and the PFET have dopant types and concentrations provided according to the workfunctions needed for each type of transistor. The gate conductor of the PFET is p+ doped, e.g., using boron, while the gate conductor of the NFET is n+ doped e.g., using phosphorus or arsenic. This is achieved by heavily doped polysilicon lower layers 26 of the gate conductors being preferably doped to concentrations between about 10^{18} cm^{-3} to 10^{20} cm^{-3} .

Each gate conductor preferably includes a low-resistance portion 28 disposed above the polysilicon portion 26. The low-resistance portion 28 has much less resistance than the polysilicon portion 26, the low-resistance portion preferably including a metal, a silicide of a metal, or both. In a preferred embodiment, the low-resistance portion 28 includes a silicide formed by a self-aligned process (a "salicide"), being a conductive silicide of a silicide precursor metal such as nickel but not limited to tungsten, titanium and cobalt. More preferably, the silicide is a compound of cobalt (CoSi_2). Alternatively, each gate conductor can include a metal layer in place of the polysilicon layer 26 such as a metal layer formed as a replacement gate after high temperature processing of the source and drain regions of the transistor

have been completed.

The NFET 10 includes a channel region 92 and the PFET 20 includes a channel region 91, both channel regions being disposed below the respective gate conductor 26, as separated therefrom by a gate dielectric 27. The gate dielectric 27 preferably includes a layer of silicon dioxide which is thermally grown from the surface of the single-crystal semiconductor region 14.

The NFET and the PFET further include first spacers 40 disposed on sidewalls of the gate conductors. The spacers 40 are preferably formed of a conformably deposited dielectric material such as an oxide, e.g., silicon dioxide, or a nitride such as silicon nitride.

Halo and extension regions 22 are disposed adjacent to the gate conductors 26, their locations determined by the thickness of spacers 40. Second spacers 30 are disposed on sidewalls of the first spacers 40. Each transistor further includes source and drain regions 24 disposed on alternate sides of the gate conductors, the locations of the source and drain regions being determined by the combined thicknesses of the first and second spacers 30 and 40.

Figures 2A through 10 illustrate stages in the fabrication of the structure 12, according to an embodiment of the invention. Figures 2A

illustrates a stage in which the polysilicon gate conductor (GC) layers 26 are formed to overlie an NFET device region 15 and a PFET device region 17 of the single-crystal semiconductor region 14 of the substrate 16. For ease of illustration, the insulating layer 18 and the portion of the substrate 16 underlying the insulating layer are omitted from the views shown in FIGS. 2A through 10. The polysilicon GC layers 26 are spaced from the respective device regions 15, 17 by a gate dielectric 27, which is preferably an oxide thermally grown on the surface of the single-crystal semiconductor region 14. Workfunction doping of the gate conductors, as discussed above, is preferably already provided by this stage of fabrication. Spacers 40 are also provided, and the shallow trench isolation region 50 has already been provided at this stage.

As shown in Figure 2B, extension and halo regions 22 are formed in both the NFET and PFET device regions 15, 17, by implantation, using the polysilicon GC layers 26 and spacers 40 as masks determining the edges of the implanted regions. When the implants are performed to the NFET device region 15, the PFET device region 17 is prevented from being implanted by a mask formed over the PFET device region. When the implants are performed to the PFET device region 17, the NFET device region 15 is prevented from being implanted by a mask formed over the NFET device region.

Thereafter, as shown in Figure 3, second spacers 30 are

formed on sidewalls of the first spacers 40. Thereafter, implantations are performed to define the source and drain regions 24 for the NFET and the PFET, in a similar manner to that in which the halo and extension implants are performed.

Thereafter, as shown in Figure 4, silicide regions 28 and 32 are formed overlying the gate conductors 26 and the source and drain regions of the transistors. These silicide regions are preferably formed in a self-aligned manner by depositing a silicide precursor metal, reacting it with the underlying silicon metal and then removing any unreacted metal that remains, through a wet cleaning process, for example. At the conclusion of this step, the NFET 10 and the PFET 20 are fully formed.

In Figure 5, a unitary compressive stressed film 500 is formed over the PFET 20 and the NFET 10. The film 500 preferably consists of a nitride, such as silicon nitride, as illustrated in Figure 5. Preferably, the thickness of the film 500 and the parameters of its deposition are selected so as to achieve a particular magnitude of stress.

Thereafter, an intermediate film 550, which is preferably not stressed, is deposited over the structure. Film 550 is preferably a dielectric layer rather than conductive or semiconductive in nature, and is preferably conformal to the contour of the underlying topography. Preferably, film 550 includes an oxide, preferably being silicon dioxide, and such layer can be

formed, for example, by a low temperature deposition such as from a tetraethylorthosilicate (TEOS) precursor. In one preferred embodiment, the thickness of this layer is between 50 Å and 150 Å.

Thereafter, as shown in Figure 6, the PFET 20 is masked while a step is performed to remove the intermediate film 550 which overlies the NFET 10.

Figure 7 illustrates the structure after the intermediate film 550 is removed from the NFET 10. An etching technique is used which is selective to the underlying nitride film 500 to remove the oxide film 550 from the region overlying the NFET 10, as illustrated.

Thereafter, as illustrated in Figure 8, the portion of the stressed film 500 that is exposed and overlying the NFET 10 is implanted with ions, preferably germanium (Ge) ions, as shown by arrows 805. During this step, the stressed film 500 that overlies the PFET 20 is protected from being substantially altered by a mask 810.

The dose and energy of the ion implantation can be adjusted so that the stress in the implanted film 500 is reduced to a value close to zero. The ion implantation reduces the film stress by breaking bonds between silicon and nitrogen atoms, and causing dislocations. Experiments have demonstrated that both tensile and compressive stress can be reduced

through ion implantation to values close to zero. As a result of the ion implantation, the stress present in the silicon nitride film 500 overlying the NFET 10 is relaxed while the same film 500 retains a compressive stress in the area overlying the PFET 20. Moreover, upon conducting a thermal cycle such as annealing, the implanted portion of the film 500 can be converted to a tensile-stressed film.

Subsequent thereto, a thermal annealing process is preferably conducted. Due to the presence of the implanted ion concentration (Ge) in the portion of the film 500 overlying the NFET 10, the annealing process transforms portion of the film 500 overlying the NFET 10 to a film having a much lower magnitude of stress than that originally deposited. As a result of this process, the implanted portion of the film may even be converted to a tensile-stressed film. The portion of the stressed film 500 overlying the NFET is referenced as 902 in FIG. 1. The remaining portion of the film which overlies the PFET 20 is referenced as 901 in FIG. 1.

As further illustrated in Figure 9, preferably, a second stressed film 990 is formed specifically to apply a tensile-stressed film to the NFET 10. The second stressed film 990 is formed to overlie both the NFET 10 and the PFET 20, as illustrated. The second layer of film 990 preferably includes a tensile stressed nitride film, such as silicon nitride, for applying a tensile stress to the NFET 10. The thickness and characteristics of this second film 990 are selected to impart a desired level of tensile stress to the channel region of the

NFET 10.

Once the second stressed film 990 is formed, the previously formed oxide layer 550 functions to maintain the stressed film 990 at a sufficient distance from the underlying compressive stressed PFET 20 so as not to interfere with the amount of compressive stress which is desired to be induced in the channel region of the PFET 20.

As further shown in Figure 10, a layer of dielectric material 1000 is deposited over the structure containing the NFET 10 and the PFET 20. The dielectric layer can be formed of any of a variety of insulating materials, such as an oxide, e.g. a TEOS deposited oxide, a doped glass such as borophosphosilicate (BPSG) glass, or a low-K dielectric such as an organic material.

Referring to Figure 1 again, to complete the structure conductive vias are formed in the dielectric region to provide conductive vias 1100 contacting the silicide regions 32 disposed on the source and drain regions, as well as conductive vias 1102 contacting the silicide regions 28 of the gate conductors. The conductive vias are filled with a conductive material such as a metal or metal silicide to provide electrical connections to the NFET and PFET.

Many variations are contemplated within the scope of the

invention. In one embodiment, stressed films are formed to impart stresses to the conduction channels of devices other than PFET and NFETs (e.g., gated diodes, silicon-controlled rectifiers, triacs, etc., to name but a few).

In one such variation, instead of depositing and patterning the intermediate film over the PFET prior to forming the second stressed film, the second stressed film can be formed over both the NFET and the PFET and then patterned to remove that film from overlying the PFET, provided that such steps are performed at relatively low temperatures and under such conditions which avoid altering the characteristics of the compressive stressed portion 901 (FIG. 1) of the unitary stressed film.

In one variation of the above-described embodiment, the unitary-stressed film, as deposited over the NFET and the PFET, has a tensile stress having a first magnitude. This film imparts a tensile stress having a desirably high magnitude to the conduction channel of the NFET. After forming the unitary stressed film, the NFET is masked, and ions (e.g., Ge ions) are implanted into a portion of the unitary stressed film which overlies the PFET. After annealing, the portion of the unitary stressed film which overlies the PFET has either a tensile stress having a magnitude much lower than the first magnitude, a zero stress, or a compressive stress. In such embodiment, the second stressed film overlying the PFET desirably has a high magnitude compressive stress, in order to provide a desirably high magnitude compressive stress to the conduction channel of the PFET.

While the invention has been described with reference to certain preferred embodiments thereof, those skilled in the art will understand the many modifications and enhancements which can be made without departing from the true scope and spirit of the invention, which is limited only by the appended claims.

CLAIMS:

What is claimed is:

1. A semiconductor device structure, comprising:

a first semiconductor device;

a second semiconductor device;

a unitary stressed film disposed over both said first and second semiconductor devices, said stressed film having a first portion overlying said first semiconductor device, said first portion imparting a first magnitude compressive stress to a conduction channel of said first semiconductor device, said stressed film further having a second portion overlying said second semiconductor device, said second portion not imparting said first magnitude compressive stress to a conduction channel of said second semiconductor device, said second portion including an ion concentration not present in said second portion such that said second portion imparts one of a compressive stress having a magnitude much lower than said first magnitude, zero stress, and a tensile stress to said conduction channel of said second semiconductor device.

2. The semiconductor device structure as claimed in claim 1, wherein said first semiconductor device includes a p-type field effect transistor (PFET) and said second semiconductor device includes an n-type field effect transistor (NFET).

3. The semiconductor device structure as claimed in claim 2, wherein said unitary stressed film includes silicon nitride and said ion concentration includes a concentration of implanted germanium (Ge) ions.

4. The semiconductor device structure as claimed in claim 3, further comprising a second stressed film overlying said PFET and said NFET, said second stressed film imparting a tensile stress to said conduction channel of said NFET, and further comprising an intermediate layer overlying said PFET between said first and said second stressed films, said intermediate layer not overlying said NFET.

5. The semiconductor device structure as claimed in claim 2, wherein said second stressed film consists essentially of a nitride.

6. The semiconductor device structure as claimed in claim 2, wherein said second stressed film consists of a silicon nitride.

7. The semiconductor device structure as claimed in claim 2, wherein said intermediate layer includes a conformal dielectric material.

8. The semiconductor device structure as claimed in claim 2, wherein said intermediate layer consists essentially of an oxide.

9. The semiconductor device structure as claimed in claim 8, wherein said intermediate layer consists of silicon dioxide.

10. The semiconductor device structure as claimed in claim 8, wherein a thickness of said intermediate layer is between 100 Å and 300 Å.

11. A semiconductor device structure, comprising:

a first semiconductor device;

a second semiconductor device;

a unitary stressed film disposed over both said first and second semiconductor devices, said stressed film having a first portion overlying said first semiconductor device, said stressed film imparting a tensile stress having a first magnitude to a conduction channel of said first semiconductor device, said stressed film further having a second portion overlying said second semiconductor device, said second portion not imparting said first magnitude tensile stress to a conduction channel of said second semiconductor device, said second portion including an ion concentration not present in said second portion such that said second portion imparts one of a tensile stress having a magnitude much lower than said first magnitude, zero stress, and a compressive stress to said conduction channel of said second semiconductor device.

12. A method of fabricating a semiconductor device structure, comprising:

forming a p-type field effect transistor (PFET) and an n-type field effect transistor (NFET), said NFET and said PFET each having a conduction channel disposed in a single-crystal semiconductor region of a substrate;

forming a stressed film having a compressive stress at a first magnitude over said PFET and said NFET;

applying a mask to cover said PFET while exposing said NFET;

ion implanting a portion of said stressed film overlying said NFET, said mask protecting another portion of said stressed film overlying said PFET from said ion implantation; and

annealing said substrate,

whereby said compressive stress of said implanted portion of said stressed film is much reduced from said first magnitude by said annealing, such that said implanted portion overlying said NFET imparts one of a much reduced magnitude compressive stress, a zero stress and a tensile stress to said conduction channel of said NFET, and said other portion continues to impart said first magnitude compressive stress to said conduction channel of said PFET.

13. The method of claim 12, further comprising the steps of:

forming an intermediate layer overlying said PFET between said first and said second stressed films, said intermediate layer not overlying said NFET; and

forming a second stressed film overlying said PFET and said NFET, said second stressed film imparting a tensile stress to said conduction

channel of said NFET.

14. The method of claim 13 wherein said second stressed film consists essentially of silicon nitride.

15. The method of claim 13, wherein said intermediate layer consists essentially of an oxide.

16. The method of claim 15, wherein said intermediate layer consists essentially of silicon dioxide.

17. The method of claim 16, wherein said layer of silicon dioxide is deposited at a low temperature.

18. The method of claim 17, wherein said silicon dioxide is deposited from a tetra-ethylorthosilicate (TEOS) precursor.

19. The method of claim 12, wherein a thickness of said stressed film is varied to adjust a magnitude of said stress.

20. The method of claim 12, wherein a characteristic of said ion implanting is varied to adjust a magnitude of said stress.