WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first semiconductor chip including bitlines, wordlines, first bonding pads, second bonding pads, and memory cells,

the memory cells being electrically connected to the bitlines and the wordlines,

the first bonding pads being electrically connected to the bitlines, and

the second bonding pads being electrically connected to the wordlines;

a second semiconductor chip including third bonding pads, fourth bonding pads, and an input/output circuit,

the third bonding pads being electrically connected to the first bonding pads,

the fourth bonding pads being electrically connected to the second bonding pads, and

the input/output circuit being configured to write data to the memory cells via the third bonding pads and the fourth bonding pads;

a sensing line extending along an edge portion of the first semiconductor chip, an edge portion of the second semiconductor chip, or both the edge portion of the first semiconductor chip and the edge portion of the second semiconductor chip; and

a detecting circuit in the second semiconductor chip, the detecting circuit being configured to detect defects from the first semiconductor chip, the second semiconductor chip, or both the first semiconductor chip and the second semiconductor chip using the sensing line.

2. The semiconductor device of claim 1, wherein

the sensing line extends along the edge portion of the first semiconductor chip to surround the first semiconductor chip,

the sensing line extends along the edge portion of the second semiconductor chip to surround the second semiconductor chip, or

the sensing line extends along the edge portion of the first semiconductor chip to surround the first semiconductor chip and the sensing line extends along the edge portion of the second semiconductor chip to surround the second semiconductor chip.

3. The semiconductor device of claim 2, wherein

the input/output circuit is not in the first semiconductor chip, and

the memory cells are not in the second semiconductor chip.

4. The semiconductor device of any one of claims 1 to 3, wherein

the first bonding pads and the second bonding pads are on a first surface of the first semiconductor chip, and

the third bonding pads and the fourth bonding pads are on a second surface of the second semiconductor chip that faces the first surface of the first semiconductor chip.

5. The semiconductor device of claim 4, wherein

the first bonding pads directly contact the third bonding pads, and

the second bonding pads directly contact the fourth bonding pads.

6. The semiconductor device of claim 1, wherein

the sensing line includes a first sensing line and a second sensing line that are in the first semiconductor chip and the second semiconductor chip, respectively,

the first sensing line and the second sensing line are electrically connected to each other,

the input/output circuit is not in the first semiconductor chip, and

the memory cells are not in the second semiconductor chip.

7. The semiconductor device of claim 6, wherein

the first semiconductor chip includes a first bonding metal on a first surface of the first semiconductor chip,

the first bonding metal is electrically connected to the first sensing line,

the second semiconductor chip includes a second bonding metal on a second surface of the second semiconductor chip,

the second bonding metal is electrically connected to the second sensing line, and

the first bonding metal and the second bonding metal directly contact each other.

8. The semiconductor device of claim 1, wherein

the sensing line includes a first sensing line and a second sensing line that are in the first semiconductor chip and the second semiconductor chip, respectively, the first sensing line and the second sensing line are electrically connected to the detecting circuit, and

the first sensing line and the second sensing line are not electrically connected to each other.

9. The semiconductor device of claim 8, wherein

the second semiconductor chip includes a connecting line that is electrically connected to the detecting circuit and is not electrically connected to the second sensing line, and

the first sensing line is electrically connected to the connecting line.

10. The semiconductor device of claim 8 or claim 9, wherein a first distance between the first sensing line and the edge portion of the first semiconductor chip differs from a second

distance between the second sensing line and the edge portion of the second semiconductor chip.

11. The semiconductor device of claim 10, wherein the first distance is greater than the second distance.

12. The semiconductor device of claim 1, wherein

the sensing line is in the first semiconductor chip, but the sensing line is not in the second semiconductor chip,

the second semiconductor chip includes a connecting line that is electrically connected to the detecting circuit, and

the sensing line is electrically connected to the connecting line.

13. The semiconductor device of claim 1, wherein

the sensing line is in the second semiconductor chip, but the sensing line is not in the first semiconductor chip, and

the sensing line is electrically connected to the detecting circuit.

14. A semiconductor device comprising:

a first semiconductor chip including a first sensing line along edge portions of the first semiconductor chip to surround the first semiconductor chip;

a second semiconductor chip including a second sensing line along edge portions of the second semiconductor chip to surround the second semiconductor chip; and

a detecting circuit configured to detect defects from the first semiconductor chip using the first sensing line and configured to detect defects from the second semiconductor chip using the second sensing line,

the detecting circuit being in the second semiconductor chip, but the detecting circuit not being in the first semiconductor chip.

15. The semiconductor device of claim 14, wherein

the first semiconductor chip includes a first bonding metal on a first surface of the first semiconductor chip, the first bonding metal being electrically connected to the first sensing line,

the second semiconductor chip includes a second bonding metal on a second surface of the second semiconductor chip that faces the first surface of the first semiconductor chip, the second bonding metal being electrically connected to the second sensing line, and

the first bonding metal and the second bonding metal directly contact each other.

16. The semiconductor device of claim 14 or claim 15, wherein

the first sensing line and the second sensing line are electrically connected to the detecting circuit, and

the first sensing line and the second sensing line are not electrically connected to each other.

17. The semiconductor device of claim 16, wherein the first sensing line and the second sensing line do not vertically overlap with each other.

18. A semiconductor device comprising:

a first semiconductor chip;

a second semiconductor chip that is below the first semiconductor chip;

a sensing line extending along an edge portion the first semiconductor chip, an edge portion of the second semiconductor chip, or both the edge portion of the first semiconductor chip and the edge portion of the second semiconductor chip; and

a detecting circuit electrically connected to the sensing line and in the second semiconductor chip,

the detecting circuit being configured to detect defects from the first semiconductor chip, the second semiconductor chip, or both the first semiconductor chip and the second semiconductor chip using the sensing line, and

a first height from a bottom surface of a first substrate of the first semiconductor chip to a top surface of the first semiconductor chip differs from a second height from a bottom surface of a second substrate of the second semiconductor chip to a top surface of the second semiconductor chip.

19. The semiconductor device of claim 18, wherein the first height is greater than the second height.

20. The semiconductor device of claim 19, wherein a ratio of the first height and the second height is 2:1 to 100:1.