

CLAIMS

I/we claim,

1. A structure, comprising:
an opening extending into an integrated configuration, the opening having a sidewall; and
a material within the opening; the material being configured to create an undulating topography relative to the sidewall; the undulating topography having a surface roughness characterized by a mean roughness parameter R_{mean} which is the mean peak-to-valley distance along the undulating topography; the R_{mean} being at least about 4 nm.
2. The structure of claim 1 wherein the material is a first material, and further comprising a second material within the opening and along at least a portion of the undulating topography; the second material being compositionally different than the first material.
3. The structure of claim 2 wherein the first material includes at least one discrete grain which is at least partially surrounded by the second material.
4. The structure of claim 2 wherein the first material is an insulative material.
5. The structure of claim 2 wherein the first material is a conductive material.
6. The structure of claim 2 wherein the first material is a semiconductive material.
7. The structure of claim 2 wherein the first material includes one or more metals.

8. The structure of claim 2 wherein the first material includes one or more metals in combination with one or more of boron, carbon, silicon, germanium, nitrogen and oxygen.

9. The structure of claim 2 wherein the first material includes one or more of Cu, Al, Ag, Au, W, Ti and Fe.

10. The structure of claim 9 wherein the second material includes one or more titanium nitride, silicon nitride, aluminum oxide, tungsten, silicon dioxide and semiconductor material.

11. The structure of claim 2 wherein the second material includes one or more Ti, W and Si.

12. The structure of claim 11 wherein the second material further includes one or both of O and N.

13. The structure of claim 2 wherein the first material comprises one or both of Si and Ge.

14. The structure of claim 13 wherein the first material further includes one or more additional constituents selected from the group consisting of B, P and As; with a total concentration of said additional constituents within the first material being within a range of from about 0.5 at% to about 5 at%.

15. The structure of claim 2 wherein the surface roughness is also characterized by a maximum roughness parameter $R_{\max}$ which is the maximum peak-to-valley distance along the undulating topography; and wherein the $R_{\max}$ is at least about 10 nm.

16. The structure of claim 2 wherein the R_{mean} is at least about 10 nm.

17. The structure of claim 2 wherein the R_{mean} is at least about 20 nm.

18. The structure of claim 2 wherein the R_{mean} is at least about 50 nm.

19. The structure of claim 2 wherein the integrated configuration comprises a vertical stack of alternating insulative levels and conductive levels, and wherein the opening extends through the stack.

20. The structure of claim 19 wherein the opening is lined with an insulative liner, and wherein the first and second materials are within the lined opening.

21. A memory device, comprising:
a vertical stack of alternating insulative levels and conductive levels;
a slit extending through the stack;
a granular first material within the slit and having a mean granule maximum dimension (D_{maxmean}) along a cross-section of at least about 4 nm; the granular first material partially filling the opening to leave unfilled regions between grains of the granular first material;
a second material within at least some of the unfilled regions; the second material being compositionally different than the first material;
channel material pillars extending through the stack; and
memory cells along the channel material pillars.

22. The memory device of claim 21 wherein the slit separates a first block region from a second block region.

23. The memory device of claim 21 wherein the granular first material is directly against one or more of the conductive levels.

24. The memory device of claim 21 comprising one or more voids at least partially surrounded by the first material.

25. The memory device of claim 21 wherein the slit is lined with an insulative liner, and wherein the first and second materials are within the lined slit.

26. The memory device of claim 21 wherein the $D_{\max_{\text{mean}}}$ is at least about 10 nm.

27. The memory device of claim 21 wherein the slit has a width along the cross-section, and wherein the $D_{\max_{\text{mean}}}$ is at least about 2% of said width.

28. The memory device of claim 21 wherein the slit has a width along the cross-section, and wherein the $D_{\max_{\text{mean}}}$ is at least about 5% of said width.

29. The memory device of claim 21 wherein the slit has a width along the cross-section, and wherein the $D_{\max_{\text{mean}}}$ is at least about 10% of said width.

30. The memory device of claim 21 wherein the first material includes one or more of Cu, Al, Ag, Au, W, Ti and Fe.

31. The memory device of claim 21 wherein the first material comprises one or both of Si and Ge, and further includes one or more additional constituents selected from the group consisting of B, P and As; with a total concentration of said additional constituents within the first material being within a range of from about 0.5 at% to about 5 at%.

32. A method of forming an integrated assembly, comprising:
forming a vertical stack of alternating insulative levels and conductive levels;
forming channel material pillars to extend through the stack;
forming a slit to extend through the stack; and
forming a panel within the slit; the forming of the panel comprising forming a first material within the slit to partially fill the slit, and forming a second material within the partially-filled slit; the first material having a surface comprised by an undulating outer topography; the undulating outer topography being characterized by a mean roughness parameter R_{mean} which is the mean peak-to-valley distance along the undulating outer topography; the R_{mean} being at least about 4 nm.
33. The method of claim 32 wherein the first material is a sputter-deposited metal.
34. The method of claim 33 wherein the sputter-deposited metal includes one or more of Cu, Al, Ag, Au and Fe.
35. The method of claim 32 wherein the first material includes at least one discrete grain which is at least partially surrounded by the second material.
36. The method of claim 32 wherein the first material comprises one or both of Si and Ge.
37. The method of claim 36 wherein the first material further includes one or more additional constituents selected from the group consisting of B, P and As; with a total concentration of said additional constituents within the first material being within a range of from about 0.5 at% to about 5 at%.

38. The method of claim 32 wherein one or more voids remain within the slit after the forming of the second material within the partially-filled slit.

39. The method of claim 32 further comprising:
lining the slit with an insulative liner; and
forming the first and second materials within the lined slit.

40. The method of claim 39 wherein the insulative liner comprises one or both of silicon dioxide and silicon nitride.

41. The method of claim 39 further comprising partially filling the lined slit with a third material prior to forming the first material within the lined slit.

42. The method of claim 41 wherein the third material comprises a same composition as the second material.

43. The method of claim 41 wherein the third material comprises a different composition than the second material.