

Description

Title: Manufacturing of a Donor Substrate for the Manufacture of a POI Structure

The present invention relates to the manufacturing process of donor substrates for the manufacture of Piezo on Insulator, POI, structures, in particular, POI structures usable for the manufacturing of microelectronic, micromechanical and photonic devices. Further, the invention relates to the manufacturing process of POI structures by means of thus manufactured donor substrates.

10 In the field of microelectronics, micromechanics and photonics POI structures are of increasing importance due to superior sensibility and information propagation properties, for example. For example, sensors as surface acoustic wave (SAW) sensors, or bulk acoustic wave (BAW) sensors utilizing the piezoelectric effect to transduce an electrical signal into a mechanical / acoustic wave offer particularly advantageous options due to
15 a wide variety of measurable ambient parameters including temperature, pressure, strain and torque, for example.

A typical POI structure comprises a layer of piezoelectric material, in particular, a single-crystal material, such as, for example, lithium niobate (LiNbO_3) or lithium tantalate
20 (LiTaO_3), on a support substrate, for example, made of silicon. Various processes of forming a thin layer of piezoelectric material on the support substrate are known in the art. Application of the Smart Cut™ technology has been proven particularly advantageous. According to this technology (see, for example, WO 2020/200986 A1), a piezoelectric substrate formed on a support substrate is implanted by light species to form a
25 weakened region in the piezoelectric substrate and afterwards the piezoelectric substrate is bonded to a target substrate. By fracture at the weakened region the thin layer of piezoelectric material can be obtained on the support substrate. The transferred layer of piezoelectric material is subject to an annealing process and, subsequently, a polishing process, particular, by chemical mechanical polishing, CMP, in an attempt to im-
30 prove the crystalline quality and achieve the desired thickness uniformity of a mono-domain layer of piezoelectric material with substantially all dipole moments being aligned parallel to each other in a given direction.

However, the quality of the piezoelectric layer to be transformed from a donor substrate comprising the piezoelectric substrate to a target substrate is not satisfying in the art. In order to obtain the piezoelectric substrate a massive block of a piezoelectric material is formed on the support substrate and grinded and/or etched. It has been observed that
5 the upper portion of the obtained piezoelectric substrate and, thus, the piezoelectric layer to be transformed exhibits some edge roll up which results in a higher thickness level at the edge of the layer as compared to the central region. Upon bonding and the expansion of the bonding wave across the bonding interface gas enclosures which could normally escape from the bonded structure by being pushed out during closure of
10 the bonding interface appear due to the edge roll up and result in edge bonding voids formed in the final POI structure.

Therefore, it is an object of the present invention to provide a technique of manufacturing a donor substrate comprising a piezoelectric layer for the manufacture of a POI
15 structure (based on the Smart Cut™ technology) with a highly uniform layer of piezoelectric material to be transferred from the donor substrate to a target substrate.

The present invention addresses this object by providing a method of manufacturing a donor substrate (pseudodonor, PSD) for the manufacture of a Piezoelectric on Insulator,
20 POI, structure, comprising

providing a support (manipulator) substrate;

forming a block of piezoelectric material on or over the support substrate, wherein the
25 piezoelectric material comprises or consists of one of lithium tantalate and lithium niobate;

chemical-mechanical polishing, CMP, the block of piezoelectric material to obtain a piezoelectric substrate; and
30

implanting a species (for example, hydrogen, maybe supplemented by helium) into the piezoelectric substrate to obtain a weakened layer in the piezoelectric substrate;

and wherein the CMP is performed by means of a CMP pad comprising a sub pad with a hardness of more than 45 shore A.

5 The shore A grade may be defined/measured according to the DIN ISO 48-4:2018 standard.

Forming the block of piezoelectric material on or over the support substrate may comprise bonding the block of piezoelectric material to the support substrate by means of a dielectric bonding layer, for example, a photo (UV) polymer layer or a layer made of or
10 comprising silicon oxide and/or silicon nitride. Grinding the block of piezoelectric material may be performed before the CMP.

Contrary to the art, the CMP of the piezoelectric and, thereby, the upper piezoelectric layer of the same to be transferred to a target substrate in the process of manufacturing
15 a POI structure is performed by an entirely hard CMP pad comprising a sub pad with a hardness of more than 45 shore A whereas a top pad (for contacting the piezoelectric layer) of the CMP pad is used as it is conventionally done (for example, a rigid top pad made of polyurethane). In the art, sub pads with a hardness of only about 35 shore A are commonly used. Depending on the actual application, according to an embodiment,
20 a CMP pad comprising a sub pad with a hardness of more than 45 shore A, in particular, more than 50 shore A, or with a hardness in the range on 45 shore A to 55 shore A, in particular, in a range of 50 shore A to 55 shore A, may be used. Usage of such hard sub pads is somewhat counterintuitive in view of a risk of generating scratches in the surface of the piezoelectric layer to be transferred. However, it turned out that a uniform
25 thickness of the piezoelectric layer to be transferred by significantly reducing edge roll up by CMP by means of entirely hard CMP pads can be achieved without causing scratches into the surface of the piezoelectric layer to be transferred. Consequently, a more reliable bonding of the transferred piezoelectric layer to the target substrate without bonding voids can be reliably achieved.

30

Other parameters of the entire manufacturing process of the donor substrate may be chosen as it is done conventionally and known to the skilled person.

According to an embodiment, the sub pad has a density of more than 0.35 g/cm^3 , in particular, more than 0.4 g/cm^3 , or in the range of 0.35 g/cm^3 to 0.45 g/cm^3 . These parameter ranges may prove advantageous in terms of the thickness uniformity of the resulting polished piezoelectric layer of the donor substrate, in particular, in combination with the above cited parameter ranges.

According to another embodiment, the sub pad has a compression force deflection in the range of 600 kPa to 670 kPa, in particular of about 641.212 kPa. The compression force deflection may be defined/measured according to the DIN ISO 48-4:2018 standard. These parameter ranges may prove advantageous in terms of the thickness uniformity of the resulting polished piezoelectric layer of the donor substrate, in particular, in combination with the above cited parameter ranges.

According to another embodiment, the CMP is performed by means of a CMP slurry consisting of an aqueous suspension of amorphous silicon with a weight percent of the amorphous silicon of less than 20, in particular, in the range of 10 to 18 or 12.5 to 17.5, contrary to the parameter range of a conventionally used CMP slurry given by 25 to 35 weight percent. The parameter ranges according to the embodiment may prove advantageous in terms of the thickness uniformity of the resulting polished piezoelectric layer of the donor substrate, in particular, in combination with the above cited parameter ranges. The amorphous silicon used for the CMP slurry may comprise or consist of precipitated amorphous silicon particles with diameters in the range of 40 to 60 nm.

Furthermore, it is provided a method of manufacturing a Piezoelectric on Insulator, POI, structure comprising performing the steps of the method of manufacturing a donor substrate according to one of the above-described examples and transferring a piezoelectric layer from the piezoelectric substrate to a target substrate comprising bonding the donor substrate to the target substrate at the side of the piezoelectric substrate and fracturing the piezoelectric substrate at the weakened layer in an anneal process.

Thereby, the piezoelectric layer can be reliably transferred to the target substrate without too heavy defects. Further post-processing (annealing and polishing) may, however,

still be needed to provide a piezoelectric layer suitable for particular applications. It is noted that naturally occurring silicon oxide may be present between the transferred piezoelectric layer and the target substrate. Further, a dielectric assembly layer may be formed on or over a surface of the target substrate before transfer of the piezoelectric layer to that surface. This dielectric assembly layer may be made of or comprise silicon oxide and/or silicon nitride or a stack of layers composed of these materials. Moreover, depending on the actual application a charge trapping layer may be formed on or over a surface of the target substrate before transfer of the piezoelectric layer to that surface. The charge trapping layer may be made of or comprise polycrystalline silicon.

As mentioned above post-processing of the piezoelectric layer transferred to the target substrate may be performed. The post-processing may comprise a thermal anneal step for increasing the crystalline quality of the transferred piezoelectric layer and consolidating the bonding of the transferred piezoelectric layer to the target substrate. The post-processing may further comprise CMP of the transferred piezoelectric layer after the thermal anneal in order to increase the thickness uniformity and surface quality and in order to remove multi-domain regions with different polarities caused by the anneal.

It is noted that other parameters of the entire manufacturing process of the manufacture of the POI structure as the ones described above with respect to the manufacture of the donor substrate may be chosen as it is done conventionally and known to the skilled person.

Further, it is provided a POI structure comprising a piezoelectric layer formed on or over a target substrate and obtainable by the method according to one of the above-described examples, wherein the piezoelectric layer may exhibit a thickness uniformity (thickness range across the diameter of the layer) of less than 50 nm, in particular, less than 20 nm. Furthermore, it is provided a microelectronic, micromechanical or photonic device or micro-electro-mechanical system (MEMS) comprising such a POI structure.

Additional features and advantages of the present invention will be described with reference to the drawings. In the description, reference is made to the accompanying Figures that are meant to illustrate preferred embodiments of the invention. It is understood that such embodiments do not represent the full scope of the invention.

5

[Fig. 1] illustrates steps of a method of manufacturing a POI structure according to an embodiment of the present invention.

[Fig. 2] illustrates the technical effect of a highly uniform piezoelectric layer to be transferred to a target substrate resulting from a method of manufacturing a donor structure
10 for the manufacture of a POI structure according to an embodiment of the present invention.

Herein, it is provided a method of manufacturing a donor substrate comprising a piezoelectric layer for the manufacture of a POI structure. The piezoelectric layer to be transferred to a target substrate exhibits a high thickness uniformity resulting from polishing performed with a relatively hard CMP polishing sub pad. The method may be comprised
15 by a method of manufacturing a POI structure according to the Smart Cut™ technology.

Fig. 1 illustrates steps of a method of manufacturing a POI structure according to an embodiment of the present invention. The method is similar to a method described in
20 WO 2020/200986 A1 but differs from the latter one by the inventive process of polishing the piezoelectric layer of the donor substrate to be transferred to a target substrate.

As shown in step i) of Fig. 1 a donor substrate 1 is provided that comprises a piezoelectric substrate 1a formed on a support (manipulator) substrate 1b. The piezoelectric substrate 1a is made of lithium tantalate (LiTaO_3) or lithium niobate (LiNbO_3). The support
25 substrate 1b may be made of a material (or a plurality of materials) with a coefficient of thermal expansion close to that exhibited by a target substrate 7, i.e., the thermal expansion coefficient of the support substrate 1b differs from the one of the target substrate 7 by less than the difference of the thermal expansion coefficient of the piezoelectric substrate 1a and that of the target substrate 7. The support substrate 1b and the target
30 substrate 7 may have identical thermal expansion coefficients and both substrates may, for example, consist of or comprise silicon. Moreover, both substrates may have similar thicknesses.

In order to obtain the donor substrate 1, a massive block of piezoelectric material may be attached to the support substrate 1b, for example, using a molecular adhesion bonding technique. The bonding may be mediated by a dielectric bonding (adhesion) layer (not shown in Fig. 1), for example, a photo (UV) polymer layer or a layer made of or
5 comprising silicon oxide and/or silicon nitride. The bonding process may include the application of a low temperature heat treatment (for example, at a temperature between 50 and 300°C, typically 100°C) making it possible to sufficiently reinforce the bonding energy to allow the following thinning step.

Subsequently, the piezoelectric substrate 1a is formed by thinning. The thinning step is
10 carried out in such a way that the piezoelectric substrate 1a has a sufficiently low thickness such that the stresses generated during heat treatment applied in a later processing stage are reduced. On the other hand, the thickness has to be sufficiently high in order to provide the piezoelectric layer 3 that is to be transferred to the target substrate 7 or to provide for a plurality of such layers that are to be transferred one after the
15 other in multiple transfer steps (after respective regeneration of the donor substrate 1) to respective target substrates. The thickness of the piezoelectric substrate 1a can be, for example, between 5 and 400 µm, for example, 20 µm or 100 µm or 200 µm.

The thinning comprises mechanical-chemical polishing (CMP). According to the invention, the CMP is performed using a relatively hard polishing sub pad. A polishing pad
20 comprises a top pad for contacting the material surface to be polished and a sub pad. While the top pad is conventionally chosen (for example, as a rigid top pad made of polyurethane), according to the invention, the sub pad of the CMP pad used for polishing the upper portion of the piezoelectric substrate and, thereby, the piezoelectric layer to be transferred to a target substrate in the process of manufacturing a POI structure has
25 a hardness of more than 45 shore A. Depending on the actual application, a material with a hardness of more than 45 shore A, in particular, more than 50 shore A, or a hardness in the range on 45 shore A to 55 shore A, in particular, in a range of 50 shore A to 55 shore A may be chosen for the sub pad of the CMP pad.

By using such a relatively hard sub pad edge roll up of the piezoelectric layer to be
30 transferred resulting conventionally in edge bonding voids formed in the final POI structure can be significantly suppressed. Consequently, a more reliable bonding of the transferred piezoelectric layer to the target substrate 7 can be achieved.

According to different embodiments the sub pad used for CMP of the piezoelectric layer 3 of the donor substrate 1 has a density of more than 0.35 g/cm^3 , in particular, more than 0.4 g/cm^3 , or in the range of 0.35 g/cm^3 to 0.45 g/cm^3 .and the sub pad may have a compression force deflection in the range of 600 kPa to 670 kPa, in particular of about
5 641.212 kPa.

For example, the sub pad of a CMP used for CMP of the piezoelectric layer 3 of the donor substrate 1 may be made of thermoplastic polyurethane and have a hardness of 53 shore A, density of 0.4 g/cm^3 , compression force deflection of 641.212 kPa (93 psi) and
10 thickness of 0.79 mm (35 mil) compared to a typical conventionally used sub pad used for CMP of a piezoelectric layer of a donor substrate used in a Smart Cut™ process for obtaining a POI structure being made of polyurethane and having a hardness of 35 shore A.

15 According to an embodiment, the CMP is performed by means of a CMP slurry consisting of an aqueous suspension of amorphous silicon with a weight percent of the amorphous silicon of less than 20, in particular, in the range of 10 to 18 or 12.5 to 17.5. The amorphous silicon used for the CMP slurry may comprise or consist of precipitated amorphous silicon particles with diameters in the range of 40 to 60 nm. For example,
20 Klebosol 30HB50 having amorphous silicon with 25 to 35 weight percent and an average diameter of the precipitated amorphous silicon particles of 50 nm may be suitably diluted with water, for example, with a 1:1 dilution, in order to obtain the CMP slurry used for CMP of the piezoelectric layer 3 of the donor substrate 1.

25 Other parameters of the overall CMP process as well as the overall process of manufacturing the POI structure illustrated in Fig. 1 may be conventionally chosen.

Fig. 2 illustrates edge roll up reduction by the usage of a CMP pad comprising a hard sub pad according to an embodiment. For the results shown a sub pad made of thermoplastic polyurethane and had a hardness of 53 shore A, density of 0.4 g/cm^3 , compression force deflection of 641.212 kPa (93 psi) and thickness of 0.79 mm (31 mil) was
30 used with a CMP slurry in the silicon concentration range mentioned above. The abscissa in Fig. 2 shows the distance from the edge of the piezoelectric layer 3 in mm and the ordinate shows the edge thickness deviation from the central thickness in Å. The

three edge profiles obtained for a conventional (POR) CMP pad for different wafers shows the disadvantageous edge roll up (see maxima of the curves). Contrary, by means of two different inventive sup pads used for the CMP such edge roll up can be clearly suppressed. For the results shown a sub pad made of thermoplastic polyurethane and had a hardness of 53 shore A, density of 0.4 g/cm^3 , compression force deflection of 641.212 kPA (93 psi) and thickness of 0.79 mm (31 mil) was used with a
5 CMP slurry in the silicon concentration range mentioned above.

In step ii) of the method illustrated in Fig. 1 hydrogen (maybe supplemented by helium) is implanted in the piezoelectric substrate 1a through the exposed surface 4 to generate
10 a weakened layer 2 which marks the separation of the piezoelectric layer 3 from the remainder part 5 of the donor substrate 1. The nature and dose of the implanted species and the implantation energy can be chosen according to the thickness of the piezoelectric layer 3 that is to be transferred to the target substrate 7 and the physicochemical properties of the piezoelectric substrate 1a. For example, for a lithium tantalate substrate a dose of hydrogen ions between 10^{16} and $5 \cdot 10^{17} \text{ at/cm}^2$ with an energy between
15 30 keV and 300 keV may be implanted to delimit the piezoelectric layer 3 with a thickness of 200 nm to 2000 nm, for example.

According to the method illustrated in Fig. 1 the implantation step ii) is followed by the step of attaching iii) the donor substrate 1 to the support substrate 7 at the side of the
20 piezoelectric substrate 1a by molecular adhesion and/or electrostatic bonding. A dielectric assembly layer 7b may be provided between the piezoelectric substrate 1a of the donor substrate 1 and the target substrate 7. The dielectric assembly layer 7b may comprise an oxide and may be made of or comprise silicon oxide and/or silicon nitride or a stack of layers composed of these materials. Further, a charge trapping layer, for example,
25 made of or comprising polycrystalline silicon, may be formed on or over the target substrate 7 in order to enhance the electrical resistivity of the same if it is desired by an actual application.

The piezoelectric layer 3 is then detached from the remainder part 5 of the donor substrate 1 to obtain iv) a POI structure 9 comprising the target substrate 7, the dielectric assembly layer 7b (if provided) and the piezoelectric layer 3. Detachment at the weakened layer 2 is facilitated by heat treatment in a temperature range of around 100°C to
30

600° to allow the transfer of the piezoelectric layer 3 to the target substrate 7. Alternatively or additionally detachment at the weakened layer 2 can be facilitated by the application of a blade or a jet of gaseous or liquid fluid or any other mechanical force applied to the weakened layer 2.

5

Post-processing of the transferred piezoelectric layer 3 is necessary to obtain a transferred piezoelectric layer 3 having satisfactory mono-domain crystalline and surface quality (reduced roughness) and thickness uniformity as demanded by actual applications. The post-processing comprises a heat treatment v) of the piezoelectric layer 3, for example, at about 500°C in a neutral atmosphere or an atmosphere comprising oxygen. This heat treatment makes it possible to cure crystalline defects present in the piezoelectric layer and consolidates the bonding between the piezoelectric layer 3 and the target substrate 7.

15 However, the heat treatment causes diffusion of hydrogen contained in the piezoelectric layer 3, particularly in its upper portion (of thickness of about 50 nm or less, for example) and, thereby, generation of a plurality of ferroelectric domains giving the upper portion a multi-domain character. In fact, the hydrogen implanted in the piezoelectric substrate 1a during the step of defining the piezoelectric layer 3 above the weakened layer 20 2 is distributed in this substrate according to a profile presenting a concentration peak at the level of the weakening plane 2. After fracture at the weakened layer 2 the piezoelectric layer 3 transferred to the target substrate 7, thus, has a significant concentration of hydrogen and heat treatment leads to the generation of multi-domains, i.e., a plurality of regions exhibiting different polarities. Performance of devices which are intended to be 25 formed on/in the piezoelectric layer 3 would be heavily affected by such multi-domains.

In order to remove the upper multi-domains and increase surface quality and thickness uniformity of the transferred piezoelectric layer 3 the post-processing comprises polishing of the exposed surface of the piezoelectric layer 3 (see step vi) in Fig. 1). For example, 30 100 to 300 nm of the upper part of the piezoelectric layer 3 may be removed by the polishing process to reach a pre-determined target thickness, for example, of about 600 nm.

Claims

1. A method of manufacturing a donor substrate (1) for the manufacture of a Piezo-electric on Insulator, POI, structure (9), comprising
- 5 providing a support substrate (1b);
- forming a block of piezoelectric material on or over the support substrate (1b), wherein the piezoelectric material comprises or consists of one of lithium tanta-
late and lithium niobate;
- 10 chemical-mechanical polishing, CMP, the block of piezoelectric material to obtain a piezoelectric substrate (1a); and
- implanting a species into the piezoelectric substrate (1a) to obtain a weakened
15 layer (2) in the piezoelectric substrate (1a);
- and wherein the CMP is performed by means of a CMP pad comprising a sub pad with a hardness of more than 45 shore A.
- 20 2. The method according to claim 1 wherein the CMP is performed by means of a CMP pad comprising a sub pad with a hardness of more than 50 shore A, or with a hardness in the range on 45 shore A to 55 shore A, in particular, in a range of 50 shore A to 55 shore A.
- 25 3. The method according to claim 1 or 2, wherein the sub pad has a density of more than 0.35 g/cm³, in particular, more than 0.4 g/cm³, or in the range of 0.35 g/cm³ to 0.45 g/cm³.
- 30 4. The method according to one of the preceding claims, wherein the sub pad has a compression force deflection in the range of 600 kPa to 670 kPa.

5. The method according to one of the preceding claims, wherein the CMP is performed by means of a CMP slurry consisting of an aqueous suspension of amorphous silicon with a weight percent of the amorphous silicon of less than 20, in particular, in the range of 10 to 18 or 12.5 to 17.5.
- 5 6. The method according to claim 5, wherein the amorphous silicon comprises or consists of precipitated amorphous silicon particles with diameters in the range of 40 to 60 nm.
- 10 7. The method according to one of the preceding claims, further comprising grinding the block of piezoelectric material before the CMP.
8. A method of manufacturing a Piezoelectric on Insulator, POI, structure (9), comprising
- 15 performing the steps of one of the preceding claims; and
- transferring a piezoelectric layer (3) from the piezoelectric substrate to a target substrate (7) comprising bonding the donor substrate (1) to the target substrate (7) at the side of the piezoelectric substrate (1a) and fracturing the piezoelectric substrate (1a) at the weakened layer (2).
- 20 9. The method according to one of the preceding claims, further comprising performing a heat treatment followed by CMP of the piezoelectric layer (3) transferred to the target substrate (7).
- 25 10. Piezoelectric on Insulator, POI, structure (9), comprising a piezoelectric layer (3) formed on or over a target substrate (7) and obtainable by the method according to one of the claims 8 and 9.
- 30 11. Microelectronic, micromechanical or photonic device or micro-electro-mechanical system comprising the POI structure (9) according to claim 10.