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ABSTRACT

Fabrication of a microelectronic device comprising:

- a) producing a structure with a support (100) provided with a semiconductor layer (12) of a first level (N_1) of components, said support (100) being provided with another semiconductor layer (120) of a second level (N_2), said other semiconductor layer (120) including a lower sublayer (121) in contact with said insulating layer and an upper sublayer (122) disposed on the lower sublayer, a first of said lower and upper sublayers being made from crystalline semiconductor material (C) while a second of said lower and upper sublayers is made from amorphous semiconductor material (A), then
- b) forming at least one transistor gate block (132) on said semiconductor layer (120), then
- c) forming, on either side of the gate block (132), by implantation(s) of dopants in said semiconductor layer (120), doped regions (125) on either side of a semiconductor region located facing the gate block (132) and provided for accommodating a channel of said transistor, then
- d) implementing at least one low-temperature heat treatment so as to implement a recrystallisation of the second semiconductor sublayer while using the first semiconductor sublayer as a start region of a crystalline front while implementing an activation of said dopants.

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Figure 6B