

ABSTRACT

COMPUTER SYSTEM THAT MAINTAINS SYSTEM WIDE CACHE COHERENCY DURING DEFERRED COMMUNICATION TRANSACTIONS

A computer system is disclosed having a requesting bus agent that issues a communication transaction over a bus and an addressed bus agent that defers the communication transaction to avoid high bus latency. The addressed bus agent later issues a deferred reply transaction over the bus to complete the communication transaction. Special snoop ownership and cache state transition rules maintain cache coherency and processor consistency during deferred communication transactions.

(Figure 7a)