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IPOS

DISLOCATION FREE LOCAL OXIDATION OF SILICON WITH SUPPRESSION OF NARROW SPACE FIELD OXIDE THINNING EFFECT

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to processes for the manufacture of semiconductor devices and more particularly to processes for forming field isolation.

(2) Description of prior art

The formation of integrated circuit devices on silicon substrates requires that a means be provided to electrically isolate the various circuit components from each other. In many cases p/n junctions themselves can be used to form at least part of the necessary isolation. Most isolation requirements, which cannot be resolved by circuit design, relate to the lateral isolation of devices. To some extent, junction isolation can be used here also. However, as device technology leads to smaller and smaller geometries as well

as shallower structures, junction isolation technology becomes very limited.

The successful use of silicon for integrated circuits for the last thirty years can, in part, be attributed to the marvelous insulating properties of it's oxide. No other commonly known semiconductor material has this unique feature. Thus silicon oxide has become well established as the isolation material for integrated circuit chips. Earliest usage of this material involved growing it on the substrate in selected regions which are defined by an oxidation masking material. To this end, silicon nitride came into widespread use. Referring to Fig. **1**, a pad silicon oxide film **22** several hundred Angstroms thick is grown on the surface of a silicon wafer **20**. Next a film of silicon nitride **24** is deposited to a thickness of several thousand Angstroms using a chemical-vapor-deposition process. The pad oxide **22** is used as a buffer layer, preventing the highly stressed silicon nitride from causing dislocations in the silicon.

Using standard photolithographic techniques followed by etching, a pattern is defined in the oxide/nitride mask, leaving bare those regions **26** on the silicon which are to become isolation regions. Referring next to Fig. **2**, the wafer **20** is subjected to an oxidizing ambient at elevated temperatures, during which the exposed areas are converted to silicon oxide **28**. The oxidation proceeds at the oxide-silicon interface. Thereby pockets of silicon oxide **27** several thousand

Angstroms deep can be formed in the patterned areas. These pockets **27** provide the necessary electrical isolation for the subsequently formed semiconductor devices. The process just described has become known by several names, one of which is LOCOS an acronym for LOCal Oxidation of Silicon. LOCOS has been practiced for over twenty-five years and has been adapted to many specific applications. One of the problems with conventional LOCOS, illustrated in Fig. **2** is that the pad oxide **22** permits oxidation to take place under the silicon nitride mask, pushing up the edge of the mask and thereby leaving a raised portion of the oxide around the mask perimeter, known as "Birds Head" **28** and a protrusion of oxide under the edge of the oxidation mask **29**, caused by diffusion of oxidant through the thin pad oxide **22**, known as "Birds Beak". The birds head **28**, being a protrusion above the surface, causes shadowing and thinning problems with subsequently deposited metallization stripes traversing across it. Thin areas in metal interconnection lines constitute "weak spots" and are subject to increased current density, heating, and subsequent electrical failure. The birds beak **29** can be reduced by using as thin as possible pad oxide **22** or by stiffening the mask by using a thicker silicon nitride layer **24**. In some instances, a sidewall oxidation barrier is formed along the mask edge to prevent penetration of the oxidant under the nitride mask. Unfortunately, these practices lead to an abrupt feature **25** wherein the high shearing stresses are produced in the silicon which lead to the

formation of dislocations. These dislocations propagate diagonally into the device active regions causing junction failure.

Typically, the field oxide is grown at temperatures above 1,000°C . At these temperatures, stresses which would be developed due to the volume expansion, are relieved by plastic flow of the oxide. However, upon completion of the oxidation, and when the wafer is cooled, sufficient plastic flow is no longer able to relieve stresses below about 960°C (**Wolf, S.**,"Silicon Processing for the VLSI Era", Vol.2, Lattice Press, Sunset Beach, CA, (1990),p693). Thermal stresses now develop due to the difference in thermal expansion coefficients of the silicon oxide and the silicon. The profile of the field oxide is now the determining factor for the distribution of stresses within the silicon. Abrupt features in the silicon/silicon oxide profile, such as **25** in Fig. **2**, are responsible for high values of x-y shearing stresses which produce dislocations. Such abrupt features **25** occur when a stiff mask edge is used to control the field oxidation.

The compressive stresses developed within the growing field oxide also have been observed to retard the oxidation rate of silicon. Known as the field oxide thinning effect, this phenomena is observed when field oxide is grown in mask openings below about 0.5 to 0.6 microns. See for example, **P. Belluti and M. Zen** in J. Electrochem. Soc. 143, (1996) p 2953.

Efforts to diffuse the abruptness of a stiff mask edge and to control the extent of birds beak encroachment into the silicon active area as well as the shape of the birds head, have been made using "L" shaped spacers which form a foot at the mask edge. **Jang US5,397,733** describes several ways in which these spacers can be formed. An example of such a spacer is shown in Fig. **3**. The thin nitride foot **30** surrounding the periphery of the thicker nitride mask provides a region of more flexible mask at the edge of the opening, thereby allowing easier expansion of the growing field oxide under it. The thicker, and therefore stiffer, section **32** continues to constrict the birds beak. By proper selection of the thickness and length of the mask foot **30** as well as the thickness of the more rigid portion **32** , it becomes possible to tailor the mask edge to provide a field oxide profile **36** with reduced stress at the expense of minimal birds beak encroachment. Jang cites prior art difficulties in forming the L-shaped spacer, specifically, difficulties in controlling thickness and length of the spacer. Indeed, the control of these parameters in a manufacturing environment is difficult.

The precise tailoring of the field oxidation mask edge becomes even more critical as device geometries shrink into the sub-half micron range. As field oxide widths approach these dimensions oxidation rates are significantly reduced and stress induced crystalline defects cause serious degradation of the

semiconductor devices. The balance between reducing birds beak encroachment and preventing stress induced dislocations requires an even greater control of the field oxide oxidation mask edge. The invention herein described provides an added dimension in mask engineering. In addition, the invention eliminates the process steps required by **Jang et.al.** for spacer formation.

Yook et.al. US5,445,990 teaches the use of a mask comprising two silicon nitride layers separated by a silicon oxide layer. Each silicon nitride layer is patterned with an opening after it is formed, thereby necessitating two photolithographic steps. The opening in the second nitride layer is smaller than that in the first nitride layer and is concentric with it. After the field oxide is grown a third photolithographic step protects the field isolation region while the oxidation mask and the birds beak region are removed. This method effectively uses the stiff mask approach to reduce birds beak and makes no effort to subdue abrupt oxide contours or reduce stress formation.

Rao US5,294,563 similarly uses an edge sealed poly buffered nitride mask wherein nitride sidewalls on the polybuffered mask edge provide an edge seal to all but the thinner than conventional pad oxide. The result is similar to other stiff-mask/thin-pad oxide methods of reducing birds beak.

Su et.al. US5,294,563 teaches the use of an undercut of the polysilicon of a conventional poly buffered silicon nitride oxidation mask to create an overlap by the subsequently formed oxide isolation of an implanted well. This permits the same mask to be used for both the implant and the isolation oxidation.

SUMMARY OF THE INVENTION

It is an object of this invention to provide a method for forming a field oxide isolation compatible with sub-half-micron device technology having reduced stress induced dislocations.

It is another object of this invention to provide a method for forming a field oxide isolation having a smooth surface topology at its periphery, thereby improving step coverage of subsequently deposited conductive layers.

It is yet another object of this invention to provide a method for forming a field oxide isolation with improved minimal birds beak encroachment into device active areas.

It is still another object of this invention to suppress the field oxide thinning effect which occurs when field oxide is grown between narrow mask spacings.

It is yet another object of this invention to describe a novel oxidation mask which will yield an improved field oxide isolation for use with sub half-micron integrated circuit technology.

These objects are accomplished by the use of a novel oxidation mask for growing the field oxide isolation. The mask is so designed that the stiffness of its edge changes during the oxidation cycle. During the initial stages of oxidation, when the oxidation rate is greatest, the mask edge is flexible and permits the rapidly growing silicon oxide to expand somewhat freely at the mask edge. thereby permitting relief of growth induced stresses. The dynamic relief of compressive stresses during the early stages of oxide growth, by use of a flexible mask edge, has the added benefit of suppressing the field oxide thinning effect.

As oxidation proceeds the mask edge becomes stiffer, thereby restricting subjacent growth and reducing birds beak encroachment. The edge of the mask is so designed that the edge stiffness begins to increase when the growth rate has slowed sufficiently to enable stress relief by viscous flow of the growing oxide. This feature thus provides a time dependent means for controlling birds beak and stress by mask design.

The mask comprises two layers of silicon nitride separated by an auxiliary layer and deposited over a pad oxide layer. The auxiliary layer between the two silicon nitride layers is recessed by a controlled amount. The first silicon nitride layer, being thinner than the second then becomes a flexible foot at the mask

edge which permits a smoother lateral transition. After the initial growth period the first silicon nitride mask contacts the thicker cantilevered second silicon nitride which causes the stiffness of the mask edge to increase.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. **1** is a cross sectional view of a wafer with a conventional LOCOS oxidation mask before field oxide formation.

Fig. **2** is a cross sectional view of a wafer with a conventional LOCOS oxidation mask after field oxide formation.

Fig. **3** is a cross sectional view of a wafer having a LOCOS oxidation mask with a modified edge according to prior art.

Figs. **4A** through Fig. **4D** are cross sectional views of a wafer showing the sequence of processing steps for forming the LOCOS oxidation mask according to this invention.

Figs. **5A** and Fig. **5B** are cross sectional views of a wafer showing a field oxide at two instants of time during its growth using an oxidation mask formed according to this invention.

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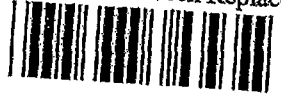


DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to Fig. **4A**, a p-doped <100> oriented monocrystalline silicon wafer **40** having a resistivity of between about 6 to 9 ohm cm. is used. A multi-layered oxidation mask is formed by first growing a layer of silicon oxide(pad oxide) **42** to a thickness of about 20 nm. by subjecting the wafer to a clean dry oxidizing ambient in a furnace at about 950°C. A first silicon nitride layer **44** about 30 nm. thick is then deposited, preferably by low pressure chemical vapor deposition (LPCVD). An auxiliary layer **46** of silicon oxide is deposited over the first silicon nitride **44** layer by LPCVD at a temperature of about 800°C. The thickness of this layer **46** is about 150 nm. Next a second silicon nitride layer **48** is deposited over the auxiliary layer using LPCVD at about 800°C to a thickness of about 150 nm. This completes the deposition of the isolation mask stack.

Photoresist **50** is applied over the mask stack, and patterned by well known photolithographic techniques to define the areas of the wafer **52** where field isolation regions are to be formed, Exposure at the mask formation is chosen to secure the dimensions of spaces during development 50 nm. less than they are on the reticle. The second silicon nitride layer **48** is then etched

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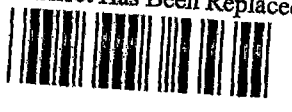


using RIE whereby the opening **52** in the photoresist is translated into an opening **52** in the second silicon nitride layer **48**. The residual photoresist is then stripped, either by plasma ashing or by chemical strippers. Fig. **4B** shows the cross section after the photoresist has been removed.

Referring now to Fig. **4C**, a wet chemical etch is applied to remove the auxiliary silicon oxide layer **46** in the opening as well as provide the undercut **54** between the two silicon nitride layers . For the silicon oxide auxiliary layer an etchant comprising 50 parts by volume of deionized water (DI-H_2O) and 1 part by volume of 49 wt%(28.3 molar) HF. The etch rate of this preparation is calibrated so that the etch time to achieve the desired undercut distance λ may be determined. An etch time of 15 minutes produces a cavity length λ of about 75 nm.

The field isolation mask is then completed as shown in Fig. **4D**, by etching the first silicon nitride layer **44** by RIE using the opening **52** in the second silicon nitride layer **48** as a mask. The pad oxide **42** acts as an etch stop for this etch. Endpoint is determined by optical spectroscopy by observing the appearance of oxygen in the etching ambient. Appropriate etchants and conditions to provide high etch-rate-ratios are well known to those practicing this art such that the taper of the walls of the resultant opening can be well controlled, and the etching

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can be cleanly terminated at or slightly within the pad oxide layer **42**.

The field oxide isolation is next grown in a clean oxidation furnace using an ambient gas containing oxygen, either alone or in combination with water vapor, and an optional chlorine containing additive such as trichloroethane to minimized mobile ion contamination. The oxidation temperature is typically between 950°C and 1,100°C. Fig. **5A** shows a cross section of the field oxide **58** at an early stage of growth. The edges of the first silicon nitride layer **44** of the oxidation mask have been pushed up by the growth of oxide under the pad oxide. The growth rate of the field oxide is governed by linear-parabolic kinetics wherein the growth rate is very rapid initially and then slows parabolically according to the diffusion of the oxidizing species. The thin silicon nitride foot **56** flexes and permits the rapidly growing silicon oxide expand, thereby providing a means of stress relief which supplements stress relief by plastic flow. Additionally the silicon nitride foot also permits a smooth silicon/silicon oxide profile **25** under the mask edge.

Referring now to Fig. **5B**. the field oxide **58** is shown at a later stage of growth wherein the outward portion of the silicon nitride foot **56** has now butted against the lower edge of the thicker silicon nitride layer **48**. This stiffer layer **48** restrains the flexing of the silicon nitride foot **56** and consequently suppresses

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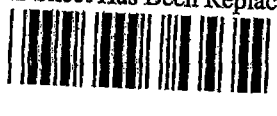


the formation of birds beak. At this point in time the growth rate of the field oxide **52** has slowed substantially, and plastic flow permits timely relief of growth stresses.

The benefits of an approximately 50 fold reduction in the shear stress component as well as the improved smoothness of edge coverage are realized by this method at the expense of a somewhat longer than conventional birds beak. This birds beak encroachment can be compensated by a lithography bias in the photomask processing. It can also be conveniently removed by a dip etch in dilute HF after the photomask is removed.

Narrow channel MOS field effect transistor devices are then fabricated in and over the silicon regions adjacent to the field oxide isolation patterns. A cross section of the channel of such a device is shown in FIG.**6** wherein the self-aligned channel **66** is formed between two field oxide isolation regions(FOX). A thin silicon oxide layer **64** overlies the channel **66** and a conductive gate electrode **68** is positioned over the surface of the field isolation(FOX), and the silicon oxide layer **64**. The source/drain regions (not shown) are located adjacent to the gate region into and out of the plane of the page.

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While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

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CLAIMS

1. A method for forming a local oxide isolation region in the surface of a silicon substrate comprising the steps of:

(a) providing a silicon substrate;

(b) forming a pad oxide over said silicon substrate;

(c) forming a first silicon nitride layer over said pad oxide;

(d) forming an auxiliary layer over said first silicon nitride layer;

(e) forming a second silicon nitride layer over said auxiliary layer;

(f) depositing a photoresist layer over said second silicon nitride layer;

(g) forming a pattern in said photoresist layer to define an opening for said local oxide isolation region;

(h) etching said second silicon nitride layer and said auxiliary layer with an anisotropic etching technique;

(i) forming a lateral cavity in said auxiliary layer; and

(j) subjecting said silicon substrate to thermal oxidation, thereby forming said local oxide isolation region.

2. The method of claim 1 wherein said pattern is biased towards said local isolation region with a bias width of between about 50 and 100 nm.

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3. The method of claim 1 wherein said first silicon nitride layer is between about 30 and 100 nm. thick.

4. The method of claim 1 wherein said auxiliary layer is between about 10 and 100 nm. thick.

5. The method of claim 1 wherein said second silicon nitride layer is between about 100 and 200 nm. thick.

6. The method of claim 1 wherein said lateral cavity is has a depth of between about 300 and 500 nm.

7. The method of claim 1 wherein said local oxide isolation region is between about 300 and 500 nm. thick.

8. The method of claim 1 wherein said opening is between about 350 and 600 nm. wide.

9. The method of claim 1 wherein said auxiliary layer is silicon oxide.

10. The method of claim 9 wherein said lateral cavity is formed using a

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calibrated wet etchant containing HF.

11. The method of claim 1 wherein said auxiliary layer is polysilicon.

12. The method of claim 11 wherein said lateral cavity is formed using a calibrated wet etchant.

13. An oxidation mask for the local oxidation of silicon comprising:

(a) a pad oxide;

(b) a first silicon nitride layer over said pad oxide;

(c) an auxiliary layer over said first silicon nitride layer;

(d) a second silicon nitride layer over said auxiliary layer;

(e) an opening passing through said second silicon nitride layer, said auxiliary layer, and said first silicon nitride layer; and

(f) a lateral cavity between said first silicon nitride layer and said second silicon nitride layer extending from the perimeter of said opening into said auxiliary layer.

14. The oxidation mask of claim 13 wherein said first silicon nitride layer is between about 30 and 100 nm. thick.

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15. The oxidation mask of claim 13 wherein said auxiliary layer is between about 10 and 100 nm. thick.

16. The oxidation mask of claim 13 wherein said second silicon nitride layer is between about 100 and 200 nm. thick.

17. The oxidation mask of claim 13 wherein said lateral cavity is has a depth of between about 300 and 500 nm.

18. The oxidation mask of claim 13 wherein said opening is between about 350 and 600 nm. wide.

19. The oxidation mask of claim 13 wherein said auxiliary layer is selected from the group consisting of silicon oxide and polysilicon.

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