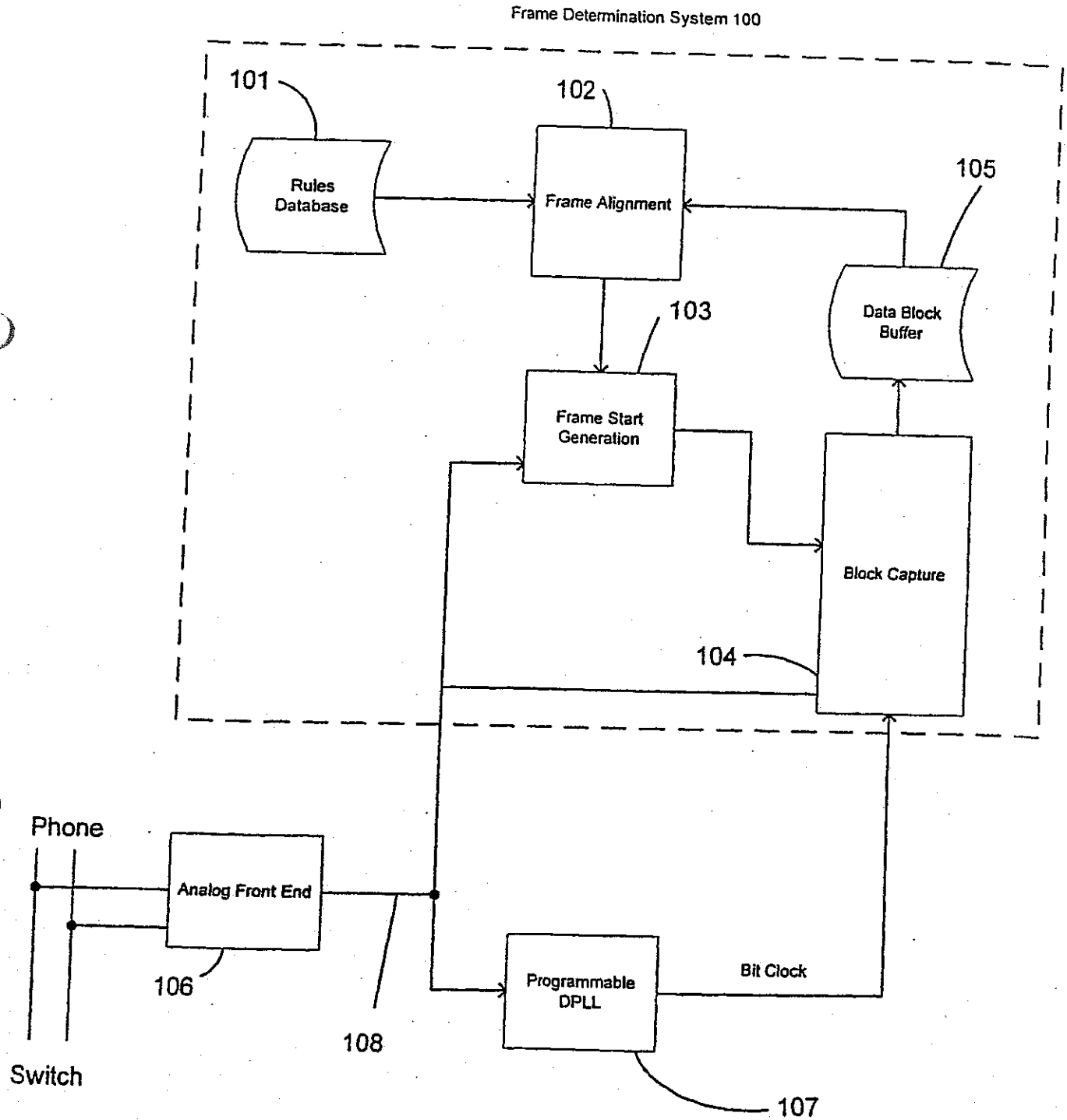

Frame Determination System 100
101
Rules Database
102
Frame Alignment
105
Data Block Buffer
103
Frame Start Generation
Block Capture
104
Phone
Analog Front End
106
108
Switch
Programmable DPLL
Bit Clock
107

FIG. 1

200

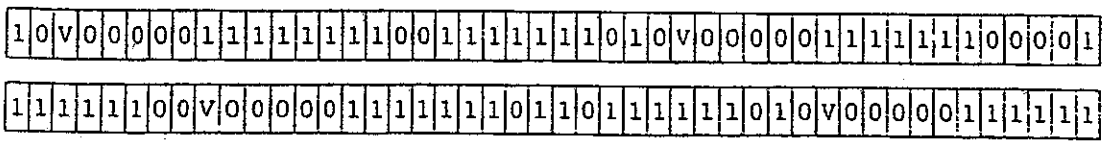


FIG. 2

300

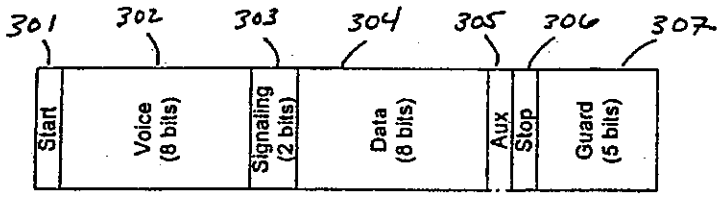


FIG. 3

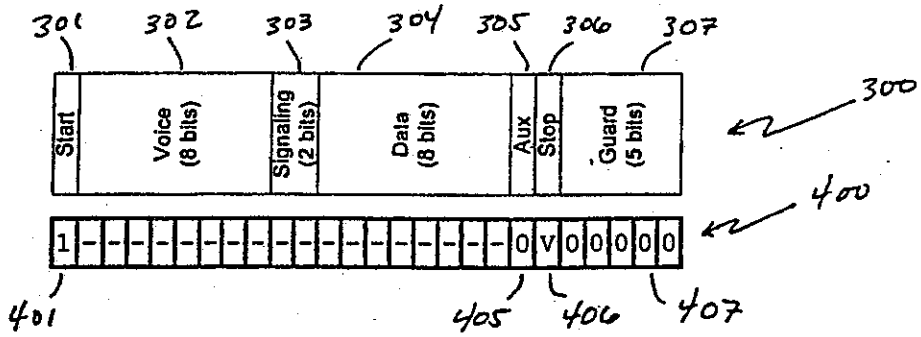


FIG. 4

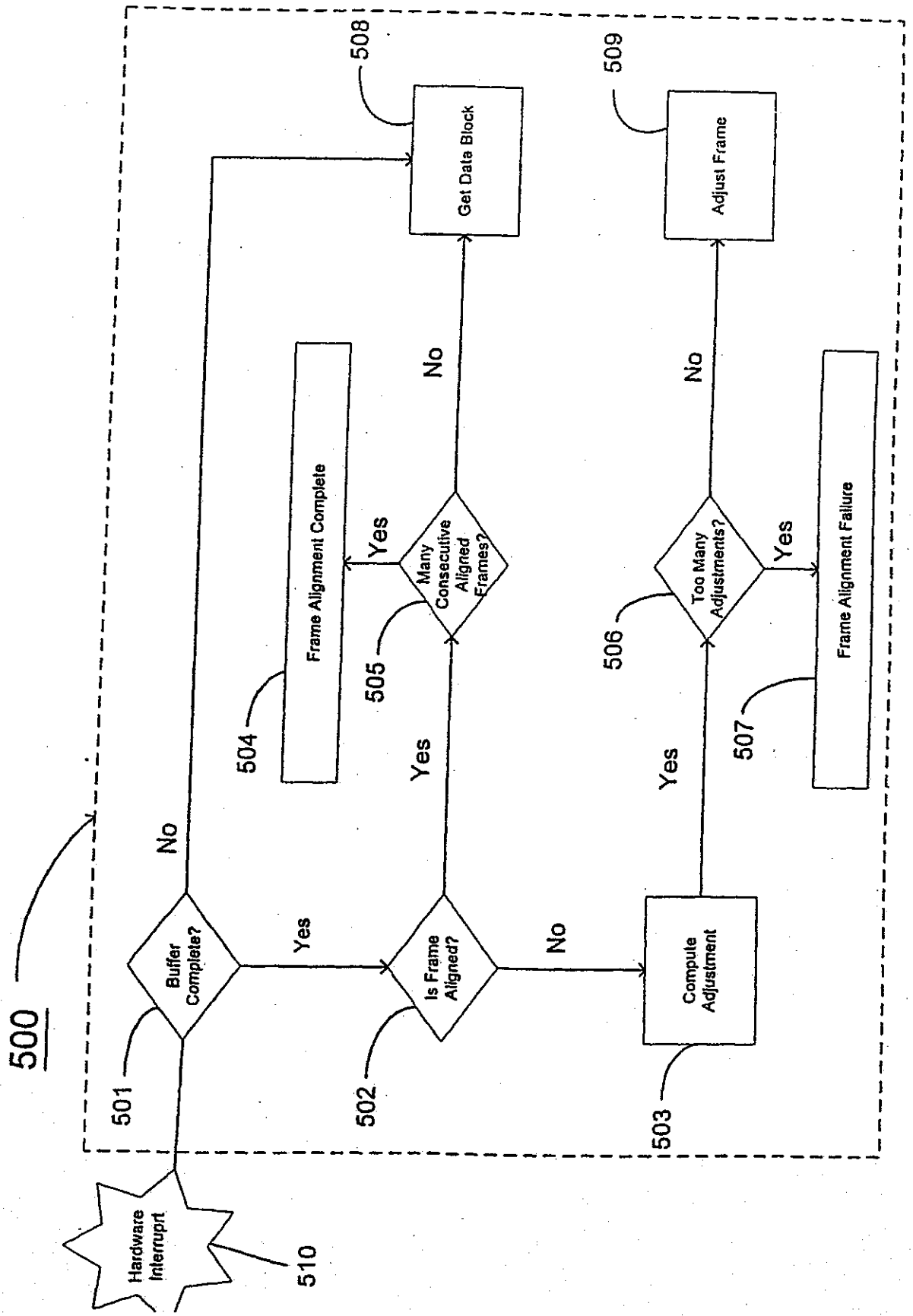

500
Buffer Complete?
501
No
Yes
Is Frame Aligned?
502
No
Compute Adjustment
503
Yes
Too Many Adjustments?
506
Yes
Frame Alignment Failure
507
No
Adjust Frame
509
Many Consecutive Aligned Frames?
505
Yes
Frame Alignment Complete
504
No
Get Data Block
508
Hardware Interrupt
510

FIG. 5

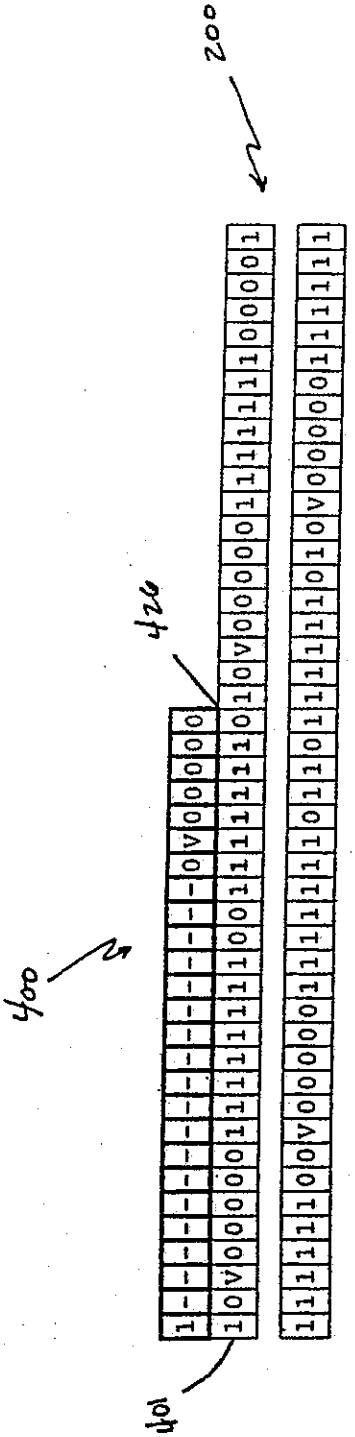


FIG. 6

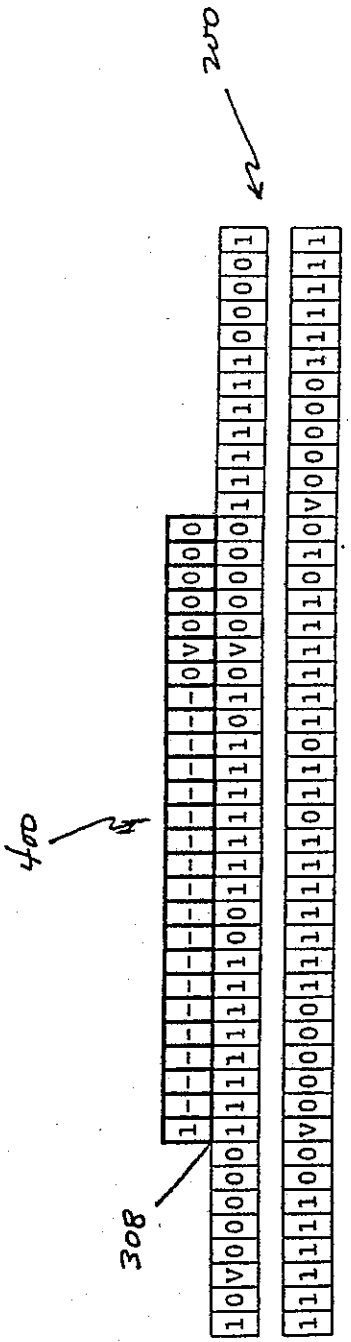


FIG. 7

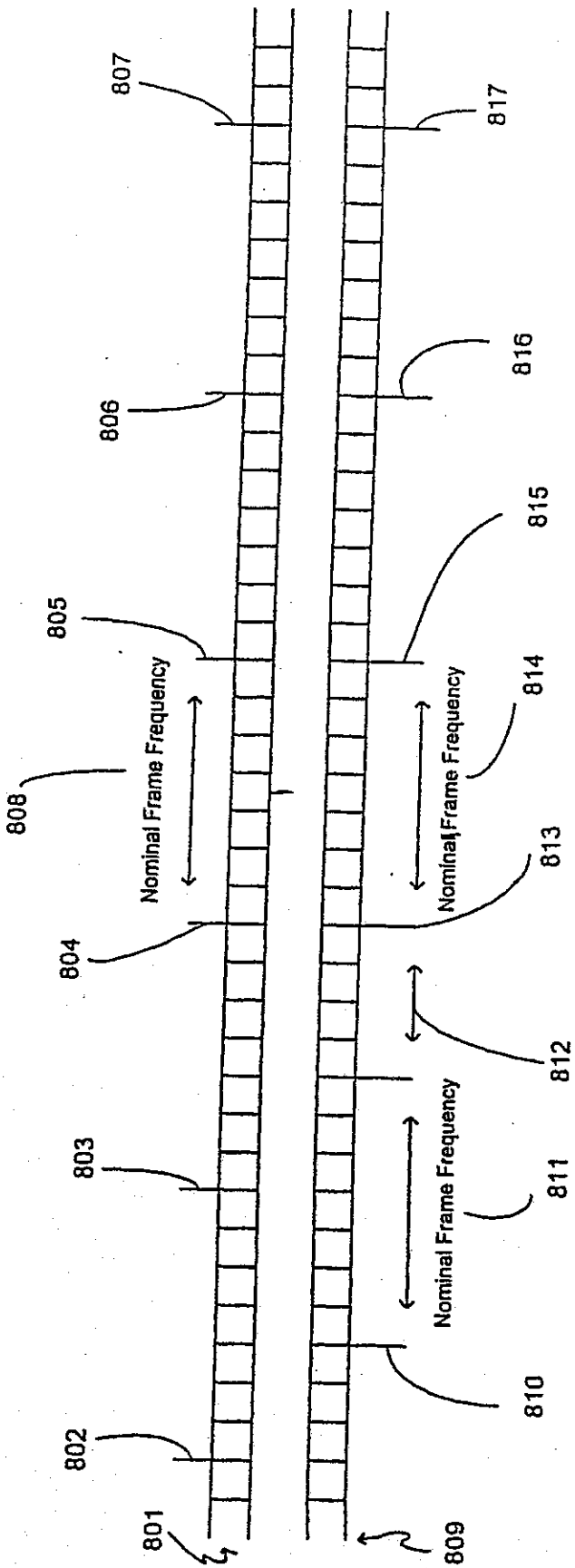

807
817
806
816
805
815
808
Nominal Frame Frequency
814
Nominal Frame Frequency
804
813
812
803
Nominal Frame Frequency
811
802
810
801
809

FIG. 8

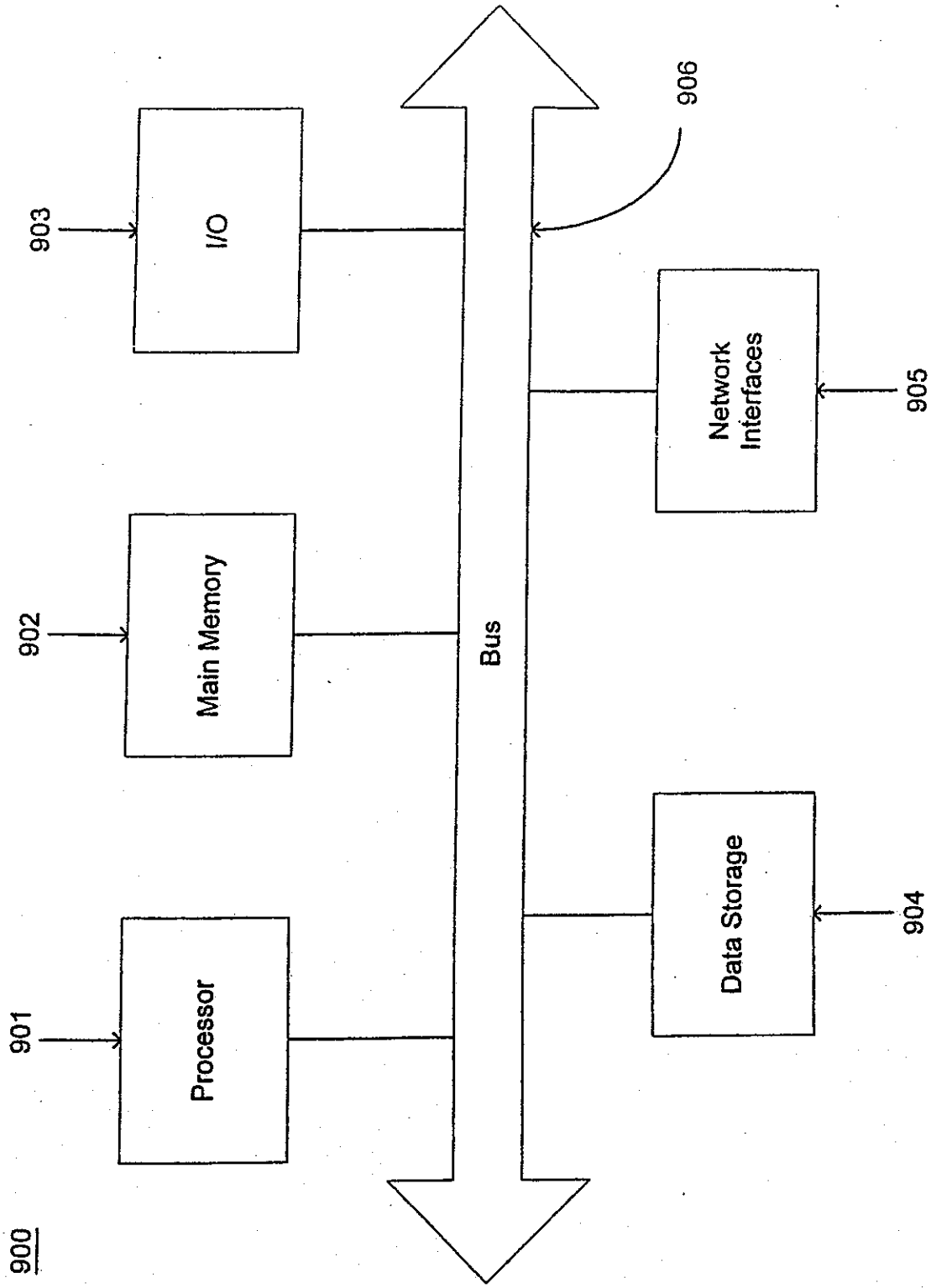

900
Processor
901
Main Memory
902
I/O
903
Data Storage
904
Network Interfaces
905
906
Bus

FIG. 9