ADHESIVE MATERIAL FOR PROGRAMMABLE DEVICE

FIELD

[0001] Programmable devices, including phase change memory devices that can be programmed by modifying the state of a phase change material.

BACKGROUND

[0002] Typical computers, or computer related devices, include physical memory, usually referred to as main memory or random access memory (RAM). Generally, RAM is memory that is available to computer programs and read-only memory (ROM) is memory that is used, for example, to store programs that boot a computer and perform diagnostics. Typical memory applications include dynamic random access memory (DRAM), static random access memory (SRAM), erasable programmable read-only memory (EPROM), and electrically erasable programmable read-only memory (EEPROM).

[0003] Solid state memory devices typically employ micro-electronic circuit elements for each memory bit (e.g., one to four transistors per bit) in memory applications. Since one or more electronic circuit elements are required for each memory bit, these devices may consume considerable chip "real estate" to store a bit of information, which limits the density of a memory chip. The primary "non-volatile" memory element of these devices, such as an EEPROM, typically employ a floating gate field effect transistor device that has limited re-programmability and which holds a charge on the gate of field effect transistor to store each memory bit. These classes of memory devices are also relatively slow to program.

[0004] Phase change memory devices use phase change materials, i.e., materials that can be electrically switched between a generally amorphous and a generally crystalline state, for electronic memory application. One type of memory element originally developed by Energy Conversion Devices, Inc. of Troy, Michigan utilizes a phase change material that can be, in one application, electrically switched between a structural state of generally amorphous and generally crystalline local order or between different detectable states of local order across the entire spectrum between completely amorphous and

completely crystalline states. Typical materials suitable for such application include those utilizing various chalcogenide elements. These electrical memory devices typically do not use field effect transistor devices as the memory storage element, but comprise, in the electrical context, a monolithic body of thin film chalcogenide material. As a result, very little chip real estate is required to store a bit of information, thereby providing for inherently high density memory chips. The state change materials are also truly non-volatile in that, when set in either a crystalline, semi-crystalline, amorphous, or semi-amorphous state representing a resistance value, that value is retained until reprogrammed as that value represents a physical state of the material (e.g., crystalline or amorphous). Thus, phase change memory materials represent a significant improvement in non-volatile memory.

[0005] One characteristic common to solid state and phase change memory devices is limited reprogrammable cycle life from/to an amorphous and crystalline state. Further, over time the phase change material can fail to reliably reprogram from/to an amorphous and a crystalline state. Factors that contribute to these unfavorable characteristics include delamination of phase change materials due to stress of film depositions and heat, and intermixing of phase change materials with adhesion materials. It would be desirable to increase the programmable cycle life of the phase change memory material and avoid the above-stated factors.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Advantages of the invention will become apparent upon reading the following detailed description and upon reference to the drawings, in which:

Fig. 1 is a schematic diagram of an embodiment of an array of memory elements;

Fig. 2 schematically illustrates a cross-sectional planar side view of a portion of a semiconductor substrate having dielectric trenches formed therein defining a z-direction thickness of a memory cell in accordance with one embodiment of forming a memory element on a substrate;

Fig. 3 depicts the structure of Fig. 2, through the same cross-sectional view, after the introduction of dopants to form an isolation device for a memory element;

Fig. 4 depicts the structure of Fig. 3 after forming the trenches;

Fig. 5 depicts a schematic top view of the structure of Fig. 4;

Fig. 6 depicts the structure of Fig. 4 after forming contacts;

Fig. 7 depicts the structure of Fig. 6, through the same cross-sectional view, after forming a masking material and a dielectric material;

Fig. 8 depicts the structure of Fig. 7, through the same cross-sectional view, after forming an adhesive on the dielectric;

Fig. 9 depicts the structure of Fig. 8, through the same cross-sectional view, after forming an opening through the adhesive and the dielectric exposing the contact;

Fig. 10 depicts the structure of Fig. 9, through the same cross-sectional view, after conformally forming a spacer within the opening and on the adhesive;

Fig. 11 depicts the structure of Fig. 10, through the same cross-sectional view, after etching the spacer;

Fig. 12 depicts the same cross-sectional view of the structure of Fig. 11, after forming programmable material, a barrier and a conductor;

Fig. 13 depicts the same cross-sectional view of the structure of Fig. 12, after patterning the programmable material, barrier and conductor;

Fig. 14 depicts another cross-sectional view of the structure of Fig. 13;

Fig. 15 depicts the same cross-sectional view of the structure of Fig. 14, after forming a dielectric material and a signal line;

Fig. 16 depicts the structure of Fig. 7, through the same cross-sectional view, after forming an opening through the dielectric exposing the contact;

Fig. 17 depicts the structure of Fig. 16, through the same cross-sectional view, after forming an electrode on the contact;

Fig. 18 depicts the structure of Fig. 17, through the same cross-sectional view, after forming a dielectric in the opening and removing a horizontal portion of the electrode;

Fig. 19A - Fig. 19E depict the structure of Fig. 18, through the same cross-sectional view, showing the formation and patterning of an adhesive and a programmable material;

Fig. 20 depicts the structure of Fig. 19E, through the same cross-sectional view, after the formation and patterning of a barrier on the programmable material and a conductor on the barrier;

Fig. 21 depicts the structure of Fig. 20, through the same cross-sectional view, after the formation of a dielectric on the conductor, the formation of a via, and the formation of a signal line on the dielectric;

Fig. 22 depicts one method of forming a memory device having a structure similar to that described by Fig. 15;

Fig. 23 depicts another method of forming a memory device having a structure similar to that described by Fig. 21; and

Fig. 24 depicts one system embodiment including a memory having a structure similar to that described by one of Fig. 15 and Fig. 21.

DETAILED DESCRIPTION

[0007] Exemplary embodiments are described with reference to specific configurations. Those of ordinary skill in the art will appreciate that various changes and modifications can be made while remaining within the scope of the appended claims. Additionally, well-known elements, devices, components, circuits, process steps and the like may not be set forth in detail in order to avoid obscuring the invention.

[0008] Currently, in some memory devices, an adhesive is not utilized between the phase change material and the electrode due to, in part, the impact that the adhesive has on the device. However, without an adhesive, the temperatures utilized in processing of memory devices is limited since temperature effects adhesion (e.g., delamination) between the phase change material and at least one of the electrode and the dielectric. Further, without an adhesive, the thickness of thin film deposition is limited since subsequent film depositions add stress, potentially causing delamination between the phase change material and at least one of the electrode and the dielectric.

[0009] Currently, in other memory devices, an adhesive is utilized between the phase change material and the electrode, having a deleterious effect on the programming of the phase change material. For example, in the case that the adhesive is highly conductive, the adhesive can effectively short out the phase change material (when in a highly resistive amorphous state) by shorting the contact to the crystalline phase change material. In the case that the adhesive is insulating, or low conductivity, the opposite problem is encountered, namely, the adhesive adds additional resistance in series with the crystalline programmed phase change material.

[0010] Further, in currently known devices, intermixing of the adhesive and the phase change material can also occur, and becomes more likely with higher temperatures. Such intermixing can cause a programming failure of the phase change material. Therefore, the choice of adhesive utilized is limited, or restricted to adhesive that resists intermixing at a given temperature.

[0011] A memory device utilizing programmable material to determine the state of memory elements of the device is described that reprograms to an amorphous and crystalline state. The described memory device and method provides improved device reliability and improved programmable cycle life relative to previous devices. Further, in an embodiment, the apparatus is manufacturable with conventional process toolsets and facilities.

[0012] In an embodiment, an adhesive is utilized between the phase change material and the dielectric. In an embodiment, concerns of delamination of the phase change material, deleterious effects on programming of the phase change material, and intermixing of the adhesive with the phase change material is controlled and minimized.

[0013] Fig. 1 shows a schematic diagram of an embodiment of a memory array comprised of a plurality of memory elements presented and formed in the context of the description provided herein. In this example, the circuit of memory array 5 includes an xy grid with memory elements 30

electrically interconnected in series with isolation devices 25 on a portion of a chip. Address lines 10 (e.g., columns) and 20 (e.g., rows) are connected, in one embodiment, to external addressing circuitry in a conventional manner. One purpose of the xy grid array of memory elements in combination with isolation devices is to enable each discrete memory element to be read and written without interfering with the information stored in adjacent or remote memory elements of the array.

[0014] A memory array such as memory device 5 of **Fig. 1** can be formed in a portion, including the entire portion, of a substrate. A typical substrate includes a semiconductor substrate such as a silicon substrate. Other substrates including, but not limited to, substrates that contain ceramic material, organic material, or glass material as part of the infrastructure are also suitable. In the case of a silicon semiconductor substrate, memory array 5 can be fabricated over an area of the substrate at the wafer level and then the wafer reduced through singulation into discrete die or chips, some or all of the die or chips having a memory array formed thereon. Additional addressing circuitry (e.g., decoders, etc.) can be formed as known to those of skill in the art.

[0015] **Figs. 2-14** illustrate an embodiment of the fabrication of representative memory element 15 of **Fig. 1**. **Fig. 2** depicts a portion of substrate 100 that is, for example, a semiconductor (e.g., silicon) substrate. In this example, a P-type dopant such as boron is introduced in portion 110. In one example, a suitable concentration of P-type dopant is on the order of about $5x10^{19}$ to $1x10^{20}$ atoms per cubic centimeter (atoms/cm^3) rendering portion 110 of substrate 100 representatively P^{++}. Overlying portion 110 of substrate 100, in this example, is portion 120 of P-type epitaxial silicon. In one example, the dopant concentration is on the order of about 10^{16} to 10^{17} atoms/cm^3.

[0016] **Fig. 2** also depicts shallow trench isolation (STI) structures 130 formed in epitaxial portion 120 of substrate 100. As will become apparent in the subsequent discussion, STI structures 130 serve, in one aspect, to define the z-direction thickness of a memory cell, with at this point only the z-direction

thickness of a memory cell defined. In one embodiment, memory cell z-direction regions 135A and 135B are patterned as strips with the x-direction dimension greater than the z-direction dimension. In another aspect, STI structures 130 serve to isolate individual memory elements from one another as well as associated circuit elements (e.g., transistor devices) formed in and on the substrate. Current state of the art photolithography techniques utilized to pattern STI structures define the z-direction thickness of memory cell regions 135A and 135B can produce feature sizes (z-direction thickness) as small as 0.18 microns (μm).

[0017] **Fig. 3** depicts the structure of **Fig. 2** after further fabrication operations in memory cell regions 135A and 135B. Within each memory cell region (strip), overlying epitaxial portion 120 of substrate 100 is first conductor or signal line material 140. In one example, first conductor or signal line material 140 is N-type doped polysilicon formed by the introduction of, for example, phosphorous or arsenic to a concentration on the order of about 10^{18} to 10^{19} atoms/cm^3 (e.g., N^+ silicon). In this example, first conductor or signal line material 140 serves as an address line, a row line (e.g., row line 20 of **Fig. 1**). Overlying first conductor or signal line material 140 is an isolation device (e.g., isolation device 25 of **Fig. 1**). In one example, the isolation device is a PN diode formed of N-type silicon portion 150 (e.g., dopant concentration on the order of about 10^{14} to 10^{18} atoms/cm^3) and P-type silicon portion 160 (e.g., dopant concentration on the order of about 10^{19} to 10^{20} atoms/cm^3). Although a PN diode is shown, it is to be appreciated that other isolation structures are similarly suitable. Such devices include, but are not limited to, metal oxide semiconductor (MOS) devices.

[0018] **Fig. 4** depicts the structure of **Fig. 3** from an xy perspective after forming trenches 190 in epitaxial portion 120 of substrate 100. Trenches 190 are formed, in this example, orthogonal to STI structures 130. Trenches 190 define the x-direction thickness of a memory cell. According to current photolithographic techniques, a suitable feature size for the x-direction thickness is as small as 0.25 μm. **Fig. 4** also depicts memory cells 145A and

145B separated by trenches 190, having a z-direction thickness defined by STI structures 130 and an x-direction thickness defined by trenches 190. The definition of the x-direction thickness involves, in one embodiment, an etch to the conductor or signal line 140 of the memory line stack to define memory cells 145A and 145B of memory cell region 135A. In the case of an etch, the etch proceeds through the memory line stack to, in this example, a portion of conductor or signal line 140. A timed etch can be utilized to stop an etch at this point. Following the patterning, N-type dopant is introduced at the base of each trench 190 to form pockets 200 having a dopant concentration on the order of about 10^{18} to 10^{20} atoms/cm^3 (e.g., N^+ region) between memory cells 145A and 145B.

[0019] Following the introduction of pockets 200, a dielectric material such as silicon dioxide is introduced in trenches 190 to form STI structures 132. The superior surface (as viewed) may then be planarized with, for example, a chemical-mechanical polish. **Fig. 5** depicts an xz perspective of the structure of **Fig. 4** with memory cells (e.g., memory cells 145A and 145B) separated by STI structures 130 and 132.

[0020] **Fig. 6** depicts the structure of **Fig. 4** (i.e., an xy perspective) following the formation of a material of, in this example, refractory metal silicide such as cobalt silicide ($CoSi_2$) in a portion of p-type silicon portion 160 to define contact 170. Contact 170, in one aspect, serves as a low resistance material in the fabrication of peripheral circuitry (e.g., addressing circuitry) of the circuit structure on the chip.

[0021] **Fig. 7** depicts the structure of **Fig. 6** after the introduction of masking material 180. As will become more clear later, masking material 180 serves, in one sense, as an etch stop for a subsequent etch operation. In one embodiment, a suitable material for masking material 180 is a dielectric material such as silicon nitride (Si_3N_4).

[0022] **Fig. 7** also depicts dielectric material 210 introduced over the structure to a thickness on the order of 100Å to 50,000Å sufficient to blanket

memory cells 145A and 145B. In one embodiment, dielectric material 210 is SiO_2. In another embodiment, dielectric material 210 is a material selected for its reduced thermal conductivity, κ, preferably a thermal conductivity less than κ_{SiO_2}, more preferably three to 10 times less κ_{SiO_2}. As a general convention, SiO_2 and Si_3N_4 have κ values on the order of 1.0. Thus, in addition to SiO_2, suitable materials for dielectric material 210 include those materials that have κ values less than 1.0. Certain high temperature polymers having κ values less than 1.0, include carbide materials, Aerogel, Xerogel (κ on the order of 0.1) and their derivatives.

[0023] **Fig. 8** depicts the structure of **Fig. 7**, after forming adhesive 214 on dielectric 210. While a variety of adhesive materials can be utilized for adhesive 214, in an embodiment, adhesive 214 includes at least one of polysilicon and titanium.

[0024] **Fig. 9** depicts the structure of **Fig. 8**, through the same cross-sectional view, after forming openings 220 through adhesive 214, dielectric 210 and masking material 180, exposing contact 170. In one embodiment, openings 220 are formed by patterning of circular holes etched through adhesive 214, dielectric 210 and masking material 180, using photolithography and dry etching techniques. In terms of state of the art photolithography techniques, circular openings as small as 0.18 μm in diameter can be patterned. It is to be appreciated that, in addition to circular openings, other openings such as rectangular openings could alternatively be employed. By forming openings 220 in this manner (i.e., after introducing adhesive 214) in an embodiment, the result is an absence of an adhesive layer on contact 170 such that current is not shunted from the subsequently introduced programmable material (see **Fig. 12**).

[0025] **Fig. 10** depicts the structure of **Fig.9** , through the same cross-sectional view, after forming optional spacer material 402 within openings 220, on adhesive 214, and on dielectric 210. In one embodiment, spacer material 402 is conformally formed, for example by chemical vapor deposition of tetra-

ethyl-ortho-silicate (TEOS) on the substrate. As shown in **Fig. 10**, spacer material covers contact 170 within openings 220.

[0026] **Fig.11** depicts the structure of **Fig. 10** after spacer material 402 is patterned to form dielectric spacers (spacer material portions 402A) inside openings 220. In one embodiment, spacer material 402 is anisotropically etched using an etching agent that is selective such that the etching agent stops at, or preserves, contact 170. As shown in **Fig. 11**, the etching operation exposes adhesive 214 over the superior surface (as viewed) of dielectric 210. In one aspect, that will become more clear later, spacer material 402 serves to reduce the quantity of programmable material (**Fig. 12**) on contact 170. Spacer material portions 402A are optional in that, in another embodiment, programmable material may be formed within openings 220, without spacer material 402 being introduced within openings 220.

[0027] **Fig. 12** depicts the structure of **Fig. 11** after introducing programmable material 404 on adhesive 214, within openings 220, and on contact 170. In one aspect, programmable material 404 tends to adhere or remain in association with adhesive 400. In one embodiment, programmable material 404 is a phase change material that has a property such that its physical state (e.g., crystalline, amorphous) can be modified with the application of an amount of energy (e.g., electrical energy, thermal energy). Chalcogenide materials having the general formula are known to be suitable for this purpose. In an embodiment, chalcogenide materials suitable as programmable material 404 include at least one element from column VI of the Periodic Table Of The Elements. In an embodiment, $Ge_2Sb_2Te_5$ is utilized as programmable material 404. Other chalcogenide alloys utilized as programmable material 404 include GaSb, InSb, InSe, Sb_2Te_3, GeTe, InSbTe, GaSeTe, $SnSb_2Te_4$, InSbGe, AgInSbTe, (GeSn)SbTe, GeSb(SeTe), and $Te_{81}Ge_{15}Sb_2S_2$. Chalcogenide materials can be introduced on the substrate and on contact 170 by conventional deposition techniques.

[0028] As further illustrated in **Fig. 12**, following the introduction of programmable material 404, barrier material 408 is formed on programmable

material 404 and conductor 410 is formed on barrier material 408. Barrier material 408 serves, in an aspect, to prevent any chemical reaction between programmable material 404 and conductor 410. In an embodiment, programmable material 404, spacer 402, barrier material 408 and conductor 410 are formed using conventional patterning techniques. In an embodiment, barrier material 408 includes at least one of titanium and titanium nitride. Titanium and/or Titanium nitride coatings can be deposited uniformily on a substrate, showing good adhesion in that they resist flaking, blistering, chipping and peeling.

[0029] In the structure illustrated in **Fig. 12**, the contact area of programmable material 404 and contact 170 is minimized by the presence of spacer material portions 402A. In an aspect, the dimensions of openings 220 expose a first contact area of contact 170. In an aspect, a second contact area, less than the first contact area, is exposed by spacer material 402 and/or spacer material portions 402A. By minimizing the quantity of programmable material 404, the quantity of programmable material 404 that undergoes, for example, a phase change from/to amorphous and crystalline on contact 170 (as shown by region 406) is localized. Region 406, shown between spacer material portions 402A, defines a limited and localized programming region of programmable material 404, adding to the programmable reliability from and to an amorphous and crystalline state of programmable material 404. In general, by localizing the phase change area, less current is required through programmable material 404 during programming and reading, and less power consumption results.

[0030] **Fig. 13** depicts the structure of **Fig. 12**, from an xy perspective, after forming openings 416. Openings 416 serve, in one aspect, to define the x-direction thickness of programmable material 404, barrier material 408 and conductor 410. Openings 416 serve, in another aspect, to isolate individual memory elements from one another as well as associated circuit elements (e.g., transistor devices) formed on the substrate. In one embodiment, openings 416 are formed by simultaneously patterning of openings through

conductor 410, barrier material 408, programmable material 404 and adhesive 214. The patterning can be accomplished using conventional photolithographic and etch techniques. In this example, the etching proceeds through conductor 410, barrier material 408, programmable material 404 and adhesive 214, to the exclusion of dielectric 210. According to current photolithographic techniques, a suitable feature size for the x-direction thickness of openings 416 include as small as 0.18 μm. As shown in **Fig. 13**, openings 416 form conductor 410 lines generally orthogonal to first conductor or signal line 140.

[0031] **Fig. 14** depicts another cross-sectional view, from the yz perspective, of the structure of **Fig. 13**. A heat sink, as illustrated by an area generally defined by lines 500 may be introduced adjacent the device structure to maintain a more stable temperature and cooler interface between programmable material 404 and contact 170.

[0032] **Fig. 15** shows the structure of **Fig. 14** after forming dielectric material 412 over conductor 410. Dielectric material 412 is, for example, SiO_2 or other suitable material that is formed on conductor 410 to electronically isolate conductor 410. Following the formation, dielectric material 412 is planarized and a via is formed in a portion of the structure through dielectric material 412, dielectric material 210, and dielectric material 180 to contact 170. The via is filled with conductive material such as tungsten (W) and a barrier material such as a combination of titanium (Ti) and titanium nitride (TiN). Techniques for introducing dielectric material 412, forming and filling conductive vias, and planarizing are known to those skilled in the art. The structure shown in **Fig. 15** also shows additional conductor or signal line material 414 formed and patterned to mirror that of conductor or signal line material 140 (e.g., row line) formed on substrate 100. Mirror conductor line material 414 mirrors conductor or signal line material 140 and is coupled to conductor or signal line material 140 through the conductive via (not shown). By mirroring a doped semiconductor such as N-type silicon, mirror conductor line material 414 serves, in one aspect, to reduce the resistance of conductor or signal line material 140 in a memory array, such as memory array 5

illustrated in **Fig. 1**. A suitable material for mirror conductor line material 414 includes an aluminum material, such as an aluminum alloy.

[0033] **Fig. 16 - Fig. 21** depict another embodiment than that described by **Fig. 8 - Fig. 15. Fig. 16** depicts the structure of **Fig. 7**, through the same cross-sectional view, after forming openings 220 through dielectric 210 and masking material 180, exposing contact 170. The formation of openings 220 may be accomplished using etch patterning with an etchant(s) selective for etching dielectric material 210 and masking material 180 but not contact 170 (e.g., contact 170 serves as an etch stop).

[0034] **Fig. 17** depicts the structure of **Fig. 16** after the conformal introduction of electrode material 230. In one example, electrode material 230 is polycrystalline semiconductor material such as polycrystalline silicon. Other suitable materials include carbon and semi-metals such as transition metals including, but not limited to, titanium, titanium-tungsten (TiW), titanium nitride (TiN) and titanium aluminum nitride (TiAlN). The introduction is conformal in the sense that electrode material 230 is introduced along the side walls and base of openings 220 such that electrode material 230 is in contact with contact 170. The conformal introduction of electrode material 230 that is, for example, polycrystalline silicon may follow conventional introduction techniques known to those skilled in the art including chemical vapor deposition (CVD) techniques.

[0035] **Fig. 18** depicts the structure of **Fig. 17** where only one of the leg portions of electrode material 230 serves as a conductive path between signal line material 140 and a subsequently introduced programmable material. In this example, electrode material 230 is a generally non-conductive intrinsic polycrystalline silicon. After the introduction of a dopant into a portion of electrode material 230, two portions are defined, electrode material 230A and electrode material 230B. Electrode material 230A is doped about its length from reducer material 170 and will act as a conductive path between signal line material 140 and subsequently introduced programmable material. Electrode material 230B is generally non-conductive (e.g., predominantly intrinsic polycrystalline silicon) and thus will generally not serve as a conductive path.

The isolation of a single conductive path (such as electrode material 230A) may be accomplished through an angled introduction of a dopant (i.e., angled away from electrode material 230B).

[0036] **Fig. 18** also shows the structure after the introduction of dielectric material 250 into openings 220. In one embodiment, dielectric material 250 is silicon dioxide (SiO_2). In another embodiment, dielectric material 250 is a material that has a thermal conductivity, κ, that is less than the thermal conductivity of SiO_2, κ_{SiO_2} preferably three to 10 times less than κ_{SiO_2}. Following introduction, the structure is subjected to a planarization that removes the horizontal component of electrode material 230. Suitable planarization techniques include those known to those of skill in the art, such as chemical or chemical-mechanical polish (CMP) techniques.

[0037] **Fig. 19A - Fig. 19E** depict the structure of **Fig. 18**, through the same cross-sectional view, showing the formation and patterning of an adhesive and a programmable material. **Fig. 19A** is an isolated view of a portion of electrode material 230A adjacent the superior surface of the structure as viewed in **Fig. 18**.

[0038] Referring to **Fig. 19B**, adhesive 215 is formed on dielectric 210, dielectric 250, and electrode material 230A. Next, adhesive 215 is patterned off of electrode material 230A (**Fig. 19C**). Subsequently, programmable material 404 is formed on adhesive 215, a portion of dielectric 210, dielectric 250, and electrode material 230A (**Fig. 19D**). In an embodiment, adhesive 215 and programmable material 404 are simultaneously patterned over an area adjacent electrode material 230A (**Fig. 19E**). The patterning can be accomplished using conventional photolithographic and etch techniques. In this example, the etching proceeds through a portion of adhesive 215 and programmable material 404, to the exclusion of dielectric 210 and dielectric 250.

[0039] **Fig. 20** depicts the structure of **Fig. 19E**, through the same cross-sectional view, after the formation and patterning of conductor 410, barrier 408,

programmable material 404, and adhesive 215. Barrier 408 includes one of, for example, titanium (Ti) and titanium nitride (TiN). Barrier 408 serves, in one aspect, to inhibit diffusion between the volume of programmable material 404 and second conductor or signal line material overlying the volume of programmable material 404 (e.g., second electrode 410). Overlying barrier 408 is conductor or signal line material 410. In this example, conductor or signal line material 410 serves as an address line, a column line (e.g., column line 10 of **Figure 1**). Conductor or signal line material 410 is patterned to be, in one embodiment, generally orthogonal to first conductor or signal line material 140 (column lines are orthogonal to row lines). Conductor or signal line material 410 is, for example, an aluminum material, such as an aluminum alloy. Methods for the introduction and patterning of barrier 408 and conductor or signal line material 410 include techniques known to those skilled in the art.

[0040] **Fig. 21** shows the structure of **Fig. 20** after forming dielectric material 412 on conductor 410. Dielectric material 412 is, for example, SiO_2 or other suitable material that is formed on conductor 410 to electronically isolate conductor 410. Following the formation, dielectric material 412 is planarized and Via 340 is formed in a portion of the structure through dielectric material 412, dielectric material 210, and dielectric material 180 to contact 170. Via 340 is filled with conductive material such as tungsten (W) and barrier material 350 such as a combination of titanium (Ti) and titanium nitride (TiN). Techniques for introducing dielectric material 412, forming and filling conductive vias, and planarizing are known to those skilled in the art. The structure shown in **Fig. 21** also shows additional conductor or signal line material 414 formed and patterned to mirror that of conductor or signal line material 140 (e.g., row line) formed on substrate 100. Mirror conductor line material 414 mirrors conductor or signal line material 140 and is coupled to conductor or signal line material 140 through the conductive via. By mirroring a doped semiconductor such as N-type silicon, mirror conductor line material 414 serves, in one aspect, to reduce the resistance of conductor or signal line material 140 in a memory array, such as memory array 5 illustrated in **Fig. 1**. A suitable material for

mirror conductor line material 414 includes an aluminum material, such as an aluminum alloy.

[0041] Fig. 22 describes a method in forming a programmable memory device having a structure similar to that depicted in Fig. 15, in accordance with an embodiment. Fig. 23 describes a method in forming a programmable memory device, having a structure similar to that depicted in Fig. 21, in accordance with an embodiment.

[0042] Further, as depicted in Fig. 24, a memory array such as memory device 5 (Fig. 1) wherein the individual memory cells have a structure similar to that described with reference to at least one of Fig. 15 and Fig. 21 and the accompanying text can be incorporated into a suitable system. In one embodiment, system 700 includes microprocessor 704, input/output (I/O) port 706, and memory 702. Microprocessor 704, I/O port 706, and memory 702 are connected by data bus 712, address bus 716 and control bus 714. Microprocessor 704 fetches instructions or reads data from memory 702 by sending out an address on address bus 716 and a memory read signal on control bus 714. Memory 702 outputs the addressed instruction or data word to microprocessor 704 on data bus 712. Microprocessor 704 writes a data word to memory 702 by sending out an address on address bus 716, sending out the data word on data bus 712, and sending a memory write signal to memory 702 on control bus 714. I/O port 706 is utilized to couple to at least one of input device 708 and output device 710.

[0043] Having disclosed exemplary embodiments, modifications and variations may be made to the disclosed embodiments while remaining within the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. A method comprising:

forming a dielectric on a contact, the contact formed on a substrate;

forming an adhesive on the dielectric;

forming an opening through the adhesive and the dielectric, exposing the contact;

forming a programmable material on the adhesive and on a first portion of the contact; and

forming a conductor coupled to the programmable material.

2. The method of claim 1, further comprising:

patterning the adhesive, the programmable material and the conductor simultaneously.

3. The method of claim 1, wherein forming an adhesive comprises forming at least one of titanium and polysilicon and forming a programmable material comprises forming a chalcogenide memory element.

4. The method of claim 1, further comprising forming at least one spacer on a second portion of the contact.

5. A apparatus comprising:

a dielectric on a contact, the contact on a substrate;

an adhesive on the dielectric, the adhesive and the dielectric having an opening exposing the contact;

a programmable material on the adhesive and on a first portion of the contact; and

a conductor coupled to the programmable material.

6. The apparatus of claim 5, wherein the adhesive comprises at least one of titanium and polysilicon and the programmable material comprises a chalcogenide memory element.

7. The apparatus of claim 5, further comprising at least one spacer on a second portion of the contact.

8. An apparatus, comprising:

a dielectric material;

a conductive material adjacent to the dielectric material;

an adhesive material over the dielectric material; and

a memory material coupled to dielectric material via the adhesive material and directly on the conductive material.

9. The apparatus of claim 8, wherein the memory material is a phase change material.

10. The apparatus of claim 8, further comprising:

a first address line coupled to the memory material; and

a second address line coupled to the conductive material.

11. The apparatus of claim 10, further comprising:

a barrier material, wherein the first address line is coupled to the memory material via the barrier material; and

an isolation device, wherein the second address line is coupled to the conductive material via the isolation device.

12. The apparatus of claim 8, wherein the adhesive material comprises polysilicon.

13. The apparatus of claim 8, wherein the adhesive material comprises titanium.

14. The apparatus of claim 8, the memory material comprises a chalcogenide material.

15. The apparatus of claim 8, wherein the adhesive material is a material adapted to reduce delamination of the memory material during and after formation of the memory material.

16. The apparatus of claim 8, wherein the dielectric material is selected from the group consisting of an oxide, a nitride, or a material having a .kappa. value less than about 1.0.