Specification

[Title of the Invention] Method of Error Correction of Read-out Data from Data Storage Medium and Error Correction Device

[Detailed Description of the Invention]

[0001]

The present invention relates to a method and an apparatus for correcting errors of read-out data read out from a medium in which data is stored.

[0002]

[Background Art]

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As storage medium for storing information such as documents, images and sounds, there have been storage media (media) such as magnetic disks (HD), digital video disks (DVD), magneto-optic disks (MO), compact disks (CD) and laser disks (LD). When data is reproduced from the media such as DVDs and CDs, errors occur in read-out data owing to changes of reflectance of light, interference between waves, noises and the like. As the errors, the probability of occurrence of bit shift of one bit is highest.

[0003]

Fig. 1 is a block diagram showing a flow of a conventional device for reproducing the read-out data which is read out from conventional media. A read-out signal from media 1 is recovered by a read channel 2, and converted to read-out data composed of a bit string. The read-out data after the conversion is sent to a mark detector 3. The mark detector 3 detects "SYNC" and a data area in the read-out data. The detected data is decoded in a decoder 4.

[0004]

The decoder 4 does not detect whether or not the read-out data (bit string) infringes a run length limited (RLL) rule. Furthermore, the decoder 4 corrects does not perform corrections of the error of the read-out data. ECC (Error Correction Code) corrects the error of the read-out data. In this case, the number of errors correctable depends on a processing capability of the ECC and the excessive errors exceeding the processing limit of the ECC can not be corrected. Therefor, all of the data errors are not necessarily corrected by the ECC.

[0005]

[Subjects to be Solved by the Invention]

The object of the present invention is to provide a method and an apparatus, which are capable of correcting errors of read-out data from a data

storage medium, especially bit shift errors, regardless the ECC.

[0006]

Another object of the present invention is to provide a novel decode system capable of correcting errors of read-out data while concurrently decoding the read-out data without degrading its performance.

[0007]

Still another object of the present invention is to provide a storage device capable of enhancing an apparent S/N ratio and decreasing a load of ECC by executing an error correction by a read channel decoder also for a medium onto which data is recorded according to conventional technologies.

[0008]

[Means for Solving the Subjects]

According to the present invention, provided is a method for correcting read-out data errors from a data storage medium, which comprises the steps of:

converting a read signal from the medium to a bit string;

detecting a gray bit having a possibility of errors in the bit string and generating gray bit information;

correcting an error bit in the bit string based on the gray bit information; and

decoding the bit string the error bit of which was corrected.

[0009]

According to the present invention, provided is a device which corrects an error of read-out data from a data storage medium, which comprises:

a circuit for converting a read signal from the medium to a bit string;

a circuit for detecting a gray bit in the bit string, the gray bit having a possibility of the error, and generating gray bit information;

a circuit for detecting the bit string including data;

a circuit for correcting an error bit of the bit string including the data based on the gray bit; and

a circuit for decoding the corrected bit string.

[0010]

According to the present invention, provided is a storage device comprising a read channel for converting a read signal from a medium to a bit string; a mark detector for detecting the bit string including data; and a decoder for decoding the bit string, which comprises:

a gray bit detection circuit for detecting a gray bit having a possibility of an error in the bit string and generating gray bit information; and

a circuit for correcting an error bit based on the gray bit information.

[0011]

[Embodiments]

Fig. 2 is a block diagram showing a flow of a device for correcting errors of read-out data read out from a data storage medium of an embodiment of the present invention. Referring to Fig. 2, the device of Fig. 2 is different from that of the conventional device of Fig. 1 in that a gray bit detection circuit 12 in a read channel 11 is provided and a RLL error correction circuit 17 and an error correction circuit 19 using a conversion table are provided in a decoder 16.

[0012]

A read signal from media 10 is recovered by a read channel 11 and converted to read data composed of a bit string. In this processing, the gray bit detection circuit 12 detects bits (gray bits) in the data bit string by a later described method, which have the possibility of errors. The read-out

data in which the gray bits are detected is sent to a mark detector 15. At the same time, gray bit information which stands the logic "1" at the position of the gray bit is sent to the mark detector 15 as a gray flag. For example, when in the data of "0010" there is the possibility of occurrence of position shift of the value "1" between two and three bits, the bit string "0110" is sent to the mark detector 15 as a gray flag.

[0013]

The mark detector 15 detects "SYNC" and a data area in the read-out data. The data detected by the mark detector 15 is sent to the decoder 16 together with a gray flag sent from the gray bit detection circuit 12. The RLL error correction circuit 17 in the decoder 17 executes the detection for the run-length limited (RLL) of the data based on the gray flag by a later described method. The data error found by the detection is corrected during transferring it to the conversion table 18. In the conversion table 18, the data which is transferred thereto after the correction is decoded. At this time, an error correction is also executed by the error correction circuit 19 using the conversion table by a later described method.

[0014]

So far, the summary of the error correction according to the embodiment of the present invention was described. Since correction according to the present invention is, based on the gray flag, performed for the portion in which the error has been already found, correct data is never changed erroneously, that is, a mis-correction never occurs. Furthermore, since the ECC does not take part in the correction, the number of correctable errors is not limited.

[0015]

Next, the following items will be described in detail below.

(1) A detection of the gray bit by the gray bit detection circuit 12

(2) A detection method and correction of run-length limited by the RLL error correction circuit 17

(3) An error correction by the error correction circuit 19 using the conversion table

[0016]

(1) A detection of the gray bit by the gray bit detection circuit 12

When data is reproduced from a storage medium such as an optical disk on which the data is stored, a read-out signal from the medium must be binarized as bit string (digital) information composed of logics "1" and "0". The read-out signal from the storage medium (media) is binarized in a slice circuit and sent to a decision circuit. The decision circuit compares the changed position binarized with the phase information sent from a PLL circuit and allocates it to a bit cell. The bit cell is sent to a decode circuit according to demand and decoded.

[0017]

Fig. 3 is a diagram showing a method for binarizing the read-out signal by the decision circuit. It should be noted that the storage includes all sorts of storage medium such as a digital video disk (DVD), a magneto-optic disk (MO), a compact disk (CD) and a laser disk (LD). Referring to Fig. 3, reference numeral 20 denotes a read-out signal from the medium, and reference numeral 21 denotes a slice level signal (slice signal) for binarizing the read-out signal. Reference numeral 22 denotes a bit cell. The bit cell 22 is determined ordinarily by the PLL based on a frequency of an output signal from the medium.

[0018]

In Fig. 3, a time cell including the cross point of the read-out signal

20 and the slice signal 21 takes the bit "1". A time cell including no cross point takes the bit "0". Thus, as shown by reference numeral 24 of Fig. 3, the read-out signal 20 is converted (binarized) to the bit string composed of the bits "1" and "0". A precision of the binarization of the read-out data in the decision circuit depends on a magnitude of the change (phase error) of the cross point 23 of the read-out signal 20 and the slice signal 21. Specifically, as the phase error becomes larger, the probability of allocation of the cross point 12 to erroneous bit becomes higher.

[0019]

Fig. 4 is a diagram showing an example of a bit string conversion (binarization) when the read-out signal changes due to influences such as noises and character degradation. In Fig. 4, the read-out signal 30 is made to change to the wave form illustrated by the solid line from the original wave form 31 illustrated by the dotted line. The cross point of the read-out signal 30 and the slice signal 32 shifts from the original cross point 33 to the cross point 34. As a result, the bit cell B which is expected to take the bit "0" is allocated to the bit "1".

[0020]

In the present invention, in order to prevent the occurrence of the situation that the data bit shifts from its original value to other values due to such phase error, the gray bit detection circuit is provided, which detects bits (gray bit) having the possibility of errors. The gray bit detection circuit exhibits the following functions.

(a) The gray bit detection circuit detects the phase error of the cross point of the read-out signal and the slice signal, and stands "the gray flag" in the bit cell having that cross point when the phase error exceeds a specified value.

(b) Moreover, when the event of (a) occurs, the gray bit detection circuit detects the phase error (distance) between the cross point and the bit cell before that bit cell and the phase error (distance) between the cross point and the bit cell behind that bit cell, and stands "the gray flag" also in the bit cell which exhibits the smaller phase error.

[0021]

For example, in the example of Fig. 4, when the cross point 34 of the slice signal 32 and the read-out signal 30 which is illustrated by the solid line is included in "the gray zone" 35 illustrated by the oblique lines, the gray bit detection circuit stands the gray flag "1" in the bit cell B. In other words, the evaluation reference value "ϕ" is compared with the distance "θ 0" between the cross point 34 and the center of the bit cell B. When the absolute value of the distance "θ 0" is larger than the evaluation reference value "ϕ", the gray bit detection circuit stands the gray flag "1" in the bit cell B. Furthermore, the absolute value of the distance "θ +1" between the cross point 34 and the center of the bit cell C is compared with the absolute value of the distance "θ -1" between the cross point 34 and the center of the bit line A, the gray bit detection circuit stands the gray flag "1" in the bit cell C having the smaller absolute value of the distance "θ +1". In the above described manner, a gray bit having the possibility of the error included in the bit string is determined.

[0022]

(2) A detection method and correction of run-length limited (RLL) of data by the RLL error correction circuit 17

The case of RLL (2, 10) will be described as an example below. The same is true of other RLLs (m, n). In accordance with a RLL (2, 10) rule, when the number of bits "0" between bit "1" and bit "1" is not a value

ranging from 2 to 10, the detection result is considered to be erroneous, that is, a contravention against the rule.

The following two cases are given as the sorts of the errors.

(a) the number of the bits "0" is not larger than 1

(b) the number of the bits "0" is not smaller than 11

The RLL error correction circuit 17 performs the correction when the RLL (2, 10) rule is contravened.

[0023]

(a) Correction of the error when the number of the bits "0" is not larger than 1

The following errors are supposed when the correct value is "010010".

Case 1: the bit "1" on the right side shifts to the left by one bit

DATA 010100

GRAY FLAG 000110

RL ERROR 000100

Case 2: the bit "1" on the left side shifts to the right by one bit

DATA 001010

GRAY FLAG 011000

RL ERROR 000010

Case 3: the bit "1" on the right side shifts to the left by one bit and the bit "1" on the left side shifts to the right by one bit

DATA 001100

GRAY FLAG 011100

RL ERROR 000100

[0024]

In such cases, the RLL error correction circuit 17 performs the

following corrections.

(1) When the gray flag (GRAY FLAG) and the rung-length error (RL error) detection position coincide with each other, the data bit in the erroneous position is corrected to "01".

(2) When the gray flag (GRAY FLAG) and the rung-length error (RL error) detection position do not coincide with each other, or when the distance of the gray flag is 1 or less while setting two bits to a unit, a data bit at a position preceding to the disagreement bit is corrected to "01"

[0025]

(b) Correction when the number of bit "0" is large

For example, the following errors are supposed when the correction value is "01000000000010".

Case 1: the bit "1" on the right side shifts to the right by one bit

DATA 010000000000010

GRAY FLAG 000000000000110

RL ERROR 000000000000010

Case 2: the bit "1" on the left side shifts to the left by one bit

DATA 010000000000010

GRAY FLAG 011000000000000

RL ERROR 000000000000010

Case 3: the bit "1" on the right side shifts to the right by one bit and the bit "1" on the left side shifts to the left by one bit

DATA 0100000000000010

GRAY FLAG 0110000000000110

RL ERROR 0000000000000100

[0026]

In such cases, the RLL error correction circuit 17 performs the

correction as described below.

(1) When the gray flag (GRAY FLAG) and the run-length error (RLL error) detection position coincide with each other, the data bit in the error position is corrected to the bit "10".

(2) When the gray flag (GRAY FLAG) and the run-length error (RL error) detection position do not coincide with each other, or when the distance between the gray flag and the run-length error (RL error) detection position is 1 or less while setting two bits to a unit, a data bit at a position preceding to the disagreement bit is corrected to "01"

[0027]

(3) Error correction by the error correction circuit 19 using the conversion table

Data which is corrected according to the RLL rule is decoded by the conversion table 18 in the decoder 16. So far, when the data do not exist in the conversion table, the decoder allowed the data to change to suitable data and the ECC performed the correction. On the contrary, in the present invention, when no data exists in the conversion table and the gray flag is 1, the error correction circuit 19 performs the correction by executing the exclusive OR for the data ("data") and the gray flag ("GRAY FLAG") as follows.

(data) XOR (GRAY FLAG)

[0028]

For example, the situation in which the correction data is "010000100000000" and the bit "1" on the right side shift to the left by one bit is assumed. In this case,

DATA 010001000000000

GRAY FLAG 000011000000000

This data (DATA) does not contravene the RLL (2, 10) rule but does not exist on the conversion table. Here, the error correction circuit 19 performs the exclusive OR for the data ("data") and the gray flag ("GRAY FLAG"). Specifically,

(010001000000000) XOR (000011000000000) = 10000100000000

is established, and the correction value is acquired.

[0029]

As described above, according to the present invention, the following advantages can be obtained.

(1) Since the error correction is executed using the RLL rule and the conversion table, the errors can be corrected regardless the number of the ECC. Therefore, the errors can be corrected regardless the number of the errors. Furthermore, the error correction at the 2 bit and 10 bit portions where the probability that the one bit shift will occur under the RLL (2, 10) rule can be performed with a high probability.

(2) Since the error corrections are performed throughout the data transfer and the data decoding, the error correction can be executed without deteriorating the performance simultaneously with decoding, that is, the on-the-fly-correction can be executed.

[Brief Description of the Drawings]

[Figure 1]

Fig. 1 is a diagram showing a flow chart for reproducing read-out data from conventional media.

[Figure 2]

Fig. 1 is a diagram showing an apparatus for correcting a read-out error from a data storage medium according to an embodiment of the present invention.

[Figure 3]

Fig. 3 is a diagram showing a method to binarize a read-out signal produced from a decision circuit.

[Figure 4]

Fig. 4 is a diagram showing an example of a bit string conversion (binarization) when the read-out signal changes by influences due to noises and characteristic degradation.

[Explanations of Reference Numerals]

1 and 10 media

2 and 11 read channel

3 and 15 mark detector

4 and 16 decoder

5 and 18 conversion table

12 gray bit detection circuit

17 RLL error correction circuit

19 error correction circuit using conversion table

20, 30 and 31 read-out signal

21 and 32 slice level



CLAIMS

[Claim 1] A method for correcting errors of read-out data from a data storage medium, comprising the steps of:

converting a read signal from the medium to a bit string;

detecting a gray bit having a possibility of errors in the bit string and generating gray bit information;

correcting an error bit in the bit string based on the gray bit information; and

decoding the bit string the error bit of which was corrected.

[Claim 2] The method according to claim 1, wherein the step for correcting the error bit comprises the step of correcting the error bit according to a run-length limited (RLL) rule.

[Claim 3] The method according to claim 2, wherein the step for correcting the error bit by said RLL rule comprises the steps of:

checking a run-length of the bit string; and

detecting the error bit in the bit string based on the run-length limited rule; and

correcting the error-bit founded by a detection, based on the gray bit information.

[Claim 4] The method according claim 1, wherein the step for converting said read signal to the bit string comprises the steps of:

obtaining a cycle of a bit cell from a frequency of said read signal;

detecting an intersection of said read signal and a slice signal;

selecting the bit cell including the intersection; and

* C L M S *

setting the selected bit cell to bit '1'.

[Claim 5] The method according to claim 4, wherein the step for detecting said gray bit and generating the gray bit information comprises the steps of:

obtaining a phase difference between a center of the selected bit cell and said intersection;

determining using the obtained phase difference whether or not the selected bit cell is the gray bit cell having the possibility of the errors; and

standing a gray flag at the bit cell determined to be the gray bit cell.

[Claim 6] The method according to claim 5, wherein the step of detecting said gray bit and generating the gray bit information comprises the steps of:

obtaining the phase difference between the center of one bit cell before the selected bit cell and said intersection and the phase difference between the center of the other bit cell after the selected bit cell and said intersection; and

standing the gray flag in any of the two bit cells before and behind the selected bit cell using the obtained two phase differences.

[Claim 7] The method according to claim 1, wherein said data storage medium is selected from a group including a magnetic disk (HD), a digital video disk (DVD), a magneto-optic disk (MO), a compact disk (CD) and a laser disk (LD).

[Claim 8] A device which corrects an error of read-out data from a data storage medium, comprising:

a circuit for converting a read signal from the medium to a bit string;

a circuit for detecting a gray bit in the bit string, the gray bit having a possibility of the error, and generating gray bit information;

a circuit for detecting the bit string including data;

a circuit for correcting an error bit of the bit string including the data, based on the gray bit; and

a circuit for decoding the corrected bit string.

* C L M S *

[Claim 9] The device according to claim 8, wherein the circuit for correcting said error bit comprises a circuit for correcting the error bit by a run-length limited (RLL) rule.

[Claim 10] A storage device which comprises a read channel for converting a read signal from a medium to a bit string, a mark detector for detecting the bit string including data; and a decoder for decoding the bit string, comprising:

a gray bit detection circuit for detecting a gray bit having a possibility of an error in the bit string and generating gray bit information; and

a circuit for correcting an error bit based on the gray bit information.

[Claim 11] The storage device according to claim 10, wherein the circuit for correcting said error bit comprises:

a circuit for correcting the error bit by a run-length limited (RLL) rule; and

a circuit for correcting the error bit using a conversion table.

[Claim 12] The storage device according to claim 10, wherein said data storage medium is selected from a group including a magnetic disk (HD), a digital video disk (DVD), a magneto-optical disk (MO), a compact disk (CD) and a laser disk (LD).