988,902

PATENT SPECIFICATION 988,902

DRAWINGS ATTACHED.

Date of Application and filing Complete Specification:
Feb. 2, 1962. *No. 4150/62.*

Application made in United States of America (No. 87258) on Feb. 6, 1961.

Complete Specification Published: April 14, 1965.

© *Crown Copyright 1965.*

Index at Acceptance:—H1 K(1A1, 1CX, 2S11, 2S20, 3E1, 3E3, 3J, 3M, 3S, 3X).

Int. Cl.:—H 01 l.

COMPLETE SPECIFICATION.

Semiconductor Devices and Methods of Making Same.

We, TEXAS INSTRUMENTS INCORPORATED of 13500 North Central Expressway, Dallas, Texas, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

This invention relates to single crystal semi-conductor devices and methods of making same, and more particularly to semiconductor devices including expitaxial layers over heavily doped zones.

In modern-day electronic packaging, the need for small as well as light-weight electronic devices has become critical. The discovery of the various semiconductor devices such as the transistor and the tunnel diode has made it possible for circuit designers to achieve component densities several orders of magnitude higher than was possible using the vacuum tube circuit components. However, in many applications the size and weight of many electronic systems utilizing the semiconductor devices is much greater than is desired or can be tolerated.

In co-pending British Patent Application No. 3633/60 (Serial No. 945,734), there is disclosed an unique integrated electronic circuit fabricated from single crystal semiconductor material. As described in this co-pending patent application, circuit modules comprising several different circuit components such as transistors, diodes, resistors and capacitors are fabricated from a single crystal semiconductor structure. These circuit modules are referred to as semiconductor networks and for the purposes of this application a semiconductor network is defined as a single crystal semiconductor structure including at least two circuit components of different types which may be interconnected.

The discovery of these semiconductor networks constituted a major breakthrough in the field of circuit miniaturization in that the entire electronic circuit modules, such as multivibrators, amplifiers or oscillators in a space and of a weight usually allocated to one transistor are available.

Many of these semiconductor networks, however, fail to function as well as the same circuit modules comprising individual components and compromises must be made between the desired reduction in size and weight and the desired circuit characteristics and capabilities. The reason many of the semiconductor networks of the prior art fail to perform as well as their counterparts made from individual components is that the components of each semiconductor network are all formed from the same single crystal of semiconductor material. The transistors, diodes and capacitors are all made by diffusing impurities into this crystal and resistors are made by using the resistivity of the semiconductor material of this crystal. Thus the original characteristics of this crystal affects the properties of all the circuit components that are formed therein. The disadvantage of this fact is that for some components it may be desirable to have one characteristic in some portions of the crystal and for others it may be desirable to have the opposite. For example, for resistors it is usually desirable that the resistivity of the semiconductor material be high because higher resistances may be obtained and a given resistance can be obtained in a shorter dimension. On the other hand, it is usually desirable that transistors be formed out of relatively low re-

sistivity material in that in this manner a low saturation voltage is achieved and collector storage is reduced. When such conflicting desires for the characteristics of the crystal of a semiconductor network occur, a compromise must be made resulting in the reduction of the operating quality of the circuit module.

An object of the present invention is to obviate or mitigate the foregoing disadvantage by providing devices and methods of making same enabling the provision of semiconductor networks which do not necessitate a compromise as aforesaid.

The present invention is a semiconductor device comprising a single crystal semiconductor substrate, one or more heavily doped diffused zones in said substrate on a face thereof, and an epitaxial layer on said substrate over the or each heavily doped zone.

The present invention is also a semiconductor device comprising a semiconductor network having two or more circuit elements of at least two different types, comprising a single crystal semiconductor substrate, a plurality of mutually spaced heavily doped diffused zones of one conductivity type in said substrate on one and the same face thereof, and an epitaxial layer of said one conductivity type on said substrate over each heavily doped diffused zone.

The present invention is also a semiconductor device comprising a single crystal semiconductor substrate, a heavily doped diffused zone of one conductivity type in said substrate on a face thereof, an epitaxial layer of said one conductivity type on said substrate over said heavily doped diffused zone, a plurality of mutually spaced regions, in said layer on the surface thereof above said heavily doped diffused zone, each having a conductivity type opposite to that of the semiconductor material immediately underlying it, a plurality of electrical connections attached to the layer surface respectively on said regions, and another electrical connection attached to said layer surface above said heavily doped diffused zone remote from said regions.

The present invention is also a method of fabricating a semiconductor device, comprising providing a single crystal semiconductor substrate, diffusing an impurity into one or more areas on a face of said substrate to form one or more heavily doped zones therein, and thereafter providing an epitaxial layer on said substrate over the or each heavily doped zone.

The present invention is also a method of fabricating a semiconductor device comprising a semiconductor network having two or more circuit elements of at least two different types, comprising providing a single crystal semiconductor substrate, diffusing impurities into a plurality of mutually spaced areas on one and the same face of said substrate to form a plurality of heavily doped zones therein of one conductivity type, thereafter providing an epitaxial layer of said one conductivity type on said substrate over each heavily doped zone, diffusing impurities into said layer above one of said heavily doped zones to form regions of alternating conductivity type having the P-N junctions therebetween terminating at the layer surface, diffusing an impurity into said layer above said one heavily doped zone to form another heavily doped zone of said one conductivity type, and attaching ohmic contacts to said layer surface on said regions of alternating conductivity type, wherein one of said ohmic contacts is on said another heavily doped zone.

Embodiments of the invention will now be described, by way of example with reference to the accompanying drawings wherein:

Fig. 1 shows in cross section a semiconductor network of the prior art;

Fig. 2 is a diagram of a circuit provided by the semiconductor network of Fig. 1;

Fig. 3 is a cross-sectional showing of an intermediate stage in the manufacture of a semiconductor network according to the present invention providing the circuit of Fig. 2;

Fig. 4 is a view in perspective of a semiconductor network according to the present invention providing the circuit of Fig. 2;

Fig. 5 is a cross section through the semiconductor network of Fig. 4 along the line 5—5;

Fig. 6 illustrates in cross section a semiconductor network of the prior art providing a three-way AND gate;

Fig. 7 is a diagram of the circuit provided by the semiconductor network of Fig. 6;

Fig. 8 is a cross-sectional showing of an intermediate stage in the manufacture of a semiconductor network according to the present invention providing the circuit of Fig. 7;

Fig. 9 is a view in elevation of a semiconductor network according to the present invention providing the circuit of Fig. 7; and

Fig. 10 is a cross section through the semiconductor network of Fig. 9 along the line 10—10.

The semiconductor network of the prior art illustrated in Fig. 1 comprises a single crystal 11 of relatively high resistivity semiconductor material such as silicon. In the illustrative example of Fig. 1 the crystal 11 has an N-type conductivity and a resistivity of 10 ohm-centimetres. At one end of the block 11 a region 13 of P-type conductivity is formed by diffusion and a heavily doped region 15 of N-type conductivity is formed by diffusion in the region 13. The top of the block 11 is etched to leave a mesa 16 including the region 13 and the region 15

projecting up from the main body of the block 11. The PN junctions between the N-type conductivity region 15 and the remaining P-type conductivity material of the region 13 and between the remaining N-type conductivity material of the block 11 and the P-type conductivity material of the region 13 form an NPN transistor in the mesa 16 with the P-type conductivity material of the region 13 providing the base, the region 15 providing the emitter and the remaining N-type conductivity material of the block 11 providing the collector. An ohmic contact 17 is provided to the P-type conductivity material of the region 13 and acts as the base electrode of the transistor. An ohmic contact 21 to the block 11 directly beneath the mesa 16 provides the collector electrode of the transistor, and an ohmic contact 23 to the heavily doped region 15 provides the emitter electrode of the transistor. At the opposite end of the block 11 from the mesa 16, an ohmic contact 19 is provided. The relatively high resistivity material between the contacts 19 and 21 in the block 11, in effect, provides a resistor connected to the collector of the transistor in the mesa 16.

Fig. 2 illustrates schematically the circuit provided by the semiconductor network of Fig. 1. As shown in Fig. 2, a resistor 25 is connected between a terminal 18 and the collector of an NPN transistor 27. A terminal 24 is connected to the emitter of the transistor 27, a terminal 22 is connected to the base of the transistor 27, and a terminal 20 is connected to the collector of the transistor 27, or in other words to the junction between the resistor 25 and the collector of the transistor 27. The resistor 25 is provided by the resistivity of the semiconductor material between contacts 19 and 21 and the transistor 27 is provided by the transistor of the mesa 16. The terminals 18, 20, 22 and 24 are provided by the contacts 19, 21, 17 and 23 respectively. Because of the difficulty of forming ohmic contacts on high resistivity material, as a practical matter the resistivity of the block 11 is limited to 10 ohm-centimetres. As a result, the resistor 25 provided by the base 11 has a maximum value of 40,000 ohms in a practical embodiment of this semiconductor network. Furthermore, the use of material of even this high resistivity in the block 11 has resulted in several serious compromises in the design of the transistor 27. Because the relatively high resistivity material of the block 11 provides the collector of the transistor 27, the transistor 27 will have a relatively high value of saturation voltage. This high saturation voltage is undesirable, particularly when the transistor 27 is to be used in a switching application. For in a switching application it is desired that when the transistor 27 is conducting or turned on, the transistor will act as nearly as possible as a short circuit. Because the transistor 27 has a relatively high saturation voltage, it will have a relatively high voltage between its collector and emitter when it is conducting or turned on and thus, will not approach the desired short circuit. Furthermore, the relatively high resistivity of the collector of the transistor 27 provided by the block 11 also permits increased collector storage, which results in a considerable slower switching time for the device.

The present invention enables the circuit of Fig. 2 to be provided by a semiconductor network in which a much high resistivity material provides the resistor 25, thus obtaining a much higher resistance for the resistor 25, whereas the collector region of the transistor 27 is provided by a much lower resistivity material. The improved semiconductor network providing the circuit of Fig. 2 according to the present invention is illustrated in Figs. 3 to 5.

As shown in Fig. 3, which illustrates the semiconductor network in an intermediate stage of manufacture, a high resistivity single crystal of semiconductor material in wafer form designated by the reference number 29 is provided. In the embodiment of Figs. 3 to 5, the wafer 29 will have a resistivity of 100 ohm-centimetres and is of N-type conductivity. Two heavily doped N-type regions or zones 31 and 32 (about 0.1. ohm-centimetres or less) are formed by diffusion into the top surface of the wafer 29 at opposite ends thereof. On top of the wafer or substrate 29 an epitaxial layer 33 of semiconductor material is grown. The layer 33 will be a continuation of the single crystal, which is essential. The term "epitaxial layer" as used herein and in the claims is to be construed as meaning a layer having the same crystalline structure as the substrate on or over which it is epitaxially grown or deposited. One way to produce this epitaxial layer is to vapour deposit semiconductor material on the base or substrate 29 in accordance with the disclosure in "Epitaxial Growth of Silicon" by Wajda et al IBM Journal of Research and Development, 4 pages 288-295 (1960) and "Impurity Introduction During Epitaxial Growth of Silicon" by Glang et al, IBM Journal of Research and Development, 4, pages 299-301 (1960). The characteristics, including the resistivity and the conductivity type of the epitaxial layer, can be freely selected. In the embodiment of Fig. 3 the conductivity is selected to be of N-type and the resistivity is selected to be relatively low, and preferably between 0.5 and 1.0 ohm-centimetres. A P-type region 35 is formed in the N-type epitaxial layer 33 by diffusion. This region 35 is formed over the heavily doped N-type

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a single crystal semiconductor substrate, one or more heavily doped diffused zones in said substrate on a face thereof, and an epitaxial layer on said substrate over the or each heavily doped zone.

2. A semiconductor device according to claim 1, comprising a plurality of said heavily doped diffused zones mutually spaced on one and the same face of said substrate.

3. A semiconductor device according to claim 1 or 2, wherein said layer includes, on its surface above a heavily doped diffused zone, contiguous regions of opposite conductivity types, and ohmic contacts attached to said layer surface respectively on said regions.

4. A semiconductor device according to any preceding claim, wherein said layer includes, on its surface above the or each heavily doped diffused zone, another heavily doped zone having the same conductivity type as the semiconductor material immediately underlying it, and an ohmic contact attached to the layer surface on the or each another heavily doped zone.

5. A semiconductor device comprising a semiconductor network having two or more circuit elements of at least two different types, comprising a single crystal semiconductor substrate, a plurality of mutually spaced heavily doped diffused zones of one conductivity type in said substrate on one and the same face thereof, and an epitaxial layer of said one conductivity type on said substrate over each heavily doped zone.

6. A semiconductor device according to claim 5, wherein one of said layers includes, on its surface above one heavily doped zone, a first region of opposite conductivity type and a second region of said one conductivity type contiguous with said first region, and ohmic contacts attached to said layer surface on said first and second regions respectively, and another ohmic contact attached to said layer surface above said one heavily doped diffused zone.

7. A semiconductor device according to claim 6, wherein said layer includes another heavily doped diffused zone of said one conductivity type under said another ohmic contact.

8. A semiconductor device comprising a single crystal semiconductor substrate, a heavily doped diffused zone of one conductivity type in said substrate on a face thereof, an epitaxial layer of said one conductivity type on said substrate over said heavily doped diffused zone, a plurality of mutually spaced regions, in said layer on the surface thereof above said heavily doped diffused zone, each having a conductivity type opposite to that of the semiconductor material immediately underlying it, a plurality of electrical connections attached to the layer surface respectively on said regions, and another electrical connection attached to said layer surface above said heavily doped diffused zone remote from said regions.

9. A semiconductor device according to claim 8, wherein said layer includes another heavily doped diffused zone of said one conductivity type under said another electrical connection.

10. A semiconductor device according to claim 8 or 9, including another heavily doped diffused zone of said one conductivity type in said substrate on a face thereof, and an epitaxial layer of said one conductivity type on said substrate over said last mentioned heavily doped diffused zone.

11. A method of fabricating a semiconductor device, comprising providing a single crystal semiconductor substrate, diffusing an impurity into one or more areas on a face of said substrate to form one or more heavily doped zones therein, and thereafter providing an epitaxial layer on said substrate over the or each heavily doped zone.

12. A method according to claim 11, wherein said areas are on one and the same face of said substrate.

13. A method according to claim 11 or 12, comprising diffusing an impurity into said layer to form one or more regions each having a conductivity type opposite to that of the semiconductor material immediately underlying it.

14. A method according to any of claims 11 to 13, comprising diffusing an impurity into said layer to form one or more heavily doped zones each having a conductivity type the same as the semiconductor material immediately underlying it.

15. A method according to claim 14, comprising attaching an ohmic contact to the or each last-mentioned heavily doped zone.

16. A method according to any of claims 11 to 15, comprising dividing said layer into a plurality of portions for separating one from the other.

17. A method of fabricating a semiconductor device comprising a semiconductor network having two or more circuit elements of at least two different types, comprising providing a single crystal semiconductor substrate, diffusing impurities into a plurality of mutually spaced areas on one and the same face of said substrate to form a plurality of heavily doped zones therein of one conductivity type, thereafter providing an epitaxial layer of said one conductivity type on said substrate over each heavily doped zone, diffusing impurities into said layer above one of said heavily doped zones to form regions of alternating conductivity type having the P-N junctions therebetween terminating at the layer surface, diffusing an

impurity into said layer above said one heavily doped zone to form another heavily doped zone of said one conductivity type, and attaching ohmic contacts to said layer surface on said regions of alternating conductivity type wherein one of said ohmic contacts is on said another heavily doped zone.

18. A semiconductor device when produced by the method of any of claims 11 to 17.

19. A semiconductor device substantially as hereinbefore described with reference to Figs. 3 to 5 of the accompanying drawings.

20. A semiconductor device substantially as hereinbefore described with reference to Figs. 8 to 10 of the accompanying drawings.

H. D. FITZPATRICK & CO.,
Chartered Patent Agents,
3 Grays Inn Square, London, W.C.1,
and
94 Hope Street, Glasgow C.2.

Abingdon: Printed for Her Majesty's Stationery Office, by Burgess & Son (Abingdon), Ltd.—1965.
Published at The Patent Office, 25 Southampton Buildings, London, W.C.2,
from which copies may be obtained.

