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(21) International Application Number: PCT/US95/16601 (22) International Filing Date: 20 December 1995 (20.12.95) (30) Priority Data: 08/363,735 23 December 1994 (23.12.94) US (71) Applicant: INTEL CORPORATION [US/US]: 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). (72) Inventors: CARMEAN, Douglas, M.; 14815 S.W. Bonnie Brae, Beaverton, OR 97007 (US). CRAWFORD, John; 2754 Glorietta Circle, Santa Clara, CA 95051 (US). (74) Agents: TAYLOR, Edwin, H. et al.; Biakely, Sokoloff, Taylor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025-1026 (US).		(81) Designated States: AL, AM, AT, AT (Utility model), AU, BB, BG, BR, BY, CA, CH, CN, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, HU, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), TJ, TM, TT, UA, UG, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG). Published With international search report.	
(54) Title: A CACHE COHERENT MULTIPROCESSING COMPUTER SYSTEM WITH REDUCED POWER OPERATING FEATURES			
(57) Abstract A multiprocessing system maintains cache coherency during a reduced power mode of operation. The multiprocessing system has a first processor and a second processor (20) coupled to the external bus (60) to perform data transactions with the main memory. During the reduced power mode of operation, the internal clock signal (ICLK) of the second processor (20) is decoupled from a portion of the internal logic of the second processor (20) while the internal clock signal (CLK) remains coupled to a portion of the internal logic of the second processor (20) that is used to monitor and respond to the traffic on the external bus (60) to maintain cache coherency. During the reduced power mode of operation, the second processor (20) continues to perform snoop and write back processes to maintain a cache coherent multiprocessor system.			
<pre> graph TD PA[PA] -- WRITE CYCLE --> Bus[EXTERNAL BUS 60] Bus -- AUTOMATIC SNOOP --> PB[PB] subgraph MRM [MRM] PA end subgraph LRM [LRM] PB end </pre>			