

CLAIMS:

1. A method of preparing a multilayer substrate, the method comprising:

epitaxially depositing an epitaxial layer on the front surface of a single crystal semiconductor handle substrate, wherein the single crystal semiconductor handle substrate comprises two major, generally parallel surfaces, one of which is the front surface of the single crystal semiconductor handle substrate and the other of which is a back surface of the single crystal semiconductor handle substrate, a circumferential edge joining the front surface and the back surface of the single crystal semiconductor handle substrate, a central plane between the front surface and the back surface of the single crystal semiconductor handle substrate, and a bulk region between the front and back surfaces of the single crystal semiconductor handle substrate, wherein the single crystal semiconductor handle substrate has a minimum bulk region resistivity of at least about 500 ohm-cm and further wherein the single crystal semiconductor handle substrate has a handle crystal orientation and wherein the epitaxial layer has a resistivity between about 100 ohm-cm and about 5000 ohm-cm and further wherein the epitaxial layer has a crystal orientation that is the same as the handle crystal orientation;

depositing a charge trapping layer on the epitaxial layer, the charge trapping layer comprising polycrystalline silicon having a resistivity of at least about 3000 ohm-cm; and

bonding a dielectric layer on a front surface of a single crystal semiconductor donor substrate to the charge trapping layer to thereby form a bonded structure, wherein the single crystal semiconductor donor substrate comprises two major, generally parallel surfaces, one of which is the front surface of the semiconductor donor substrate and the other of which is a back surface of the semiconductor donor substrate, a circumferential edge joining the front and back surfaces of the semiconductor donor substrate, and a central plane between the front and back surfaces of the semiconductor donor substrate, wherein the single crystal semiconductor donor substrate comprises a cleave plane.

2. The method of claim 1 wherein the single crystal semiconductor handle substrate has a bulk resistivity between about 1000 Ohm-cm and about 100,000 Ohm-cm.

3. The method of claim 1 wherein the single crystal semiconductor handle substrate has a bulk resistivity between about 1000 Ohm-cm and about 6,000 Ohm-cm.

4. The method of claim 1 wherein the single crystal semiconductor handle substrate comprises an electrically active dopant selected from the group consisting of boron, aluminum, gallium, indium, and any combination thereof.

5. The method of claim 1 or claim 2 wherein the epitaxial layer has a resistivity between about 200 ohm-cm and about 2000 ohm-cm, or between about 400 ohm-cm and about 1000 ohm-cm.

6. The method of claim 1 or claim 2 wherein the epitaxial layer comprises silicon.

7. The method of claim 6 wherein the epitaxial layer comprises silicon and an electrically active dopant selected from the group consisting of arsenic, phosphorus, antimony, and any combination thereof.

8. The method of claim 1 or claim 2 wherein the epitaxial layer comprises silicon doped with carbon at a carbon concentration between about 0.1 mole % and about 5 mole %.

9. The method of claim 1 or claim 2 wherein the charge trapping layer has a resistivity of at least about 7000 ohm-cm.

10. The method of claim 1 or claim 2 further comprising forming an insulating layer on the charge trapping layer prior to bonding with the dielectric layer on the front surface of the single crystal semiconductor donor substrate, wherein the insulating layer comprises semiconductor oxide or semiconductor oxynitride; and

wherein the insulating layer has a thickness between about 2000 angstroms and about 10,000 angstroms.

11. The method of claim 1 or claim 2 wherein the dielectric layer comprises a material selected from the group consisting of silicon dioxide, silicon nitride, silicon oxynitride, hafnium oxide, titanium oxide, zirconium oxide, lanthanum oxide, barium oxide, and a combination thereof; and wherein the dielectric layer has a thickness of at least about 10 nanometer thick, such as between about 10 nanometers and about 10,000 nanometers, between about 10 nanometers and about 5,000 nanometers, or between about 100 nanometers and about 400 nanometers.

12. The method of claim 1 or claim 2 further comprising heating the bonded structure at a temperature and for a duration sufficient to strengthen the bond between the dielectric layer of the single crystal semiconductor donor substrate and the charge trapping layer on the front surface of the single crystal semiconductor handle substrate; and

further comprising mechanically cleaving the bonded structure at the cleave plane of the single crystal semiconductor donor substrate to thereby prepare a cleaved structure comprising the single crystal semiconductor handle substrate, the epitaxial layer, the charge trapping layer, the dielectric layer, and a single crystal semiconductor device layer.

13. A method of preparing a multilayer substrate, the method comprising:

epitaxially depositing an epitaxial layer on the front surface of a single crystal semiconductor handle substrate, wherein the comprises single crystal semiconductor handle substrate two major, generally parallel surfaces, one of which is the front surface of the single crystal semiconductor handle substrate and the other of which is a back surface of the single crystal semiconductor handle substrate, a circumferential edge joining the front surface and the back surface of the single crystal semiconductor handle substrate, a central plane between the front surface and the back surface of the single crystal semiconductor handle substrate, and a bulk region between the front and back

surfaces of the single crystal semiconductor handle substrate, wherein the single crystal semiconductor handle substrate comprises an electrically active p-type dopant selected from the group consisting of boron, aluminum, gallium, indium, and any combination thereof and further wherein the single crystal semiconductor handle substrate has a handle crystal orientation and wherein the epitaxial layer comprises an electrically active n-type dopant selected from the group consisting of arsenic, phosphorus, antimony, and any combination thereof, wherein the concentration of the electrically active n-type dopant is less than about 1×10^{14} atoms/cm³ and further wherein the epitaxial layer has a crystal orientation that is the same as the handle crystal orientation;

depositing a charge trapping layer on the epitaxial layer, the charge trapping layer comprising polycrystalline silicon; and

bonding a dielectric layer on a front surface of a single crystal semiconductor donor substrate to the charge trapping layer to thereby form a bonded structure, wherein the single crystal semiconductor donor substrate comprises two major, generally parallel surfaces, one of which is the front surface of the semiconductor donor substrate and the other of which is a back surface of the semiconductor donor substrate, a circumferential edge joining the front and back surfaces of the semiconductor donor substrate, and a central plane between the front and back surfaces of the semiconductor donor substrate, wherein the single crystal semiconductor donor substrate comprises a cleave plane.

14. The method of claim 13 wherein the single crystal semiconductor handle substrate comprises the electrically active p-type dopant at a concentration of less than about 2×10^{13} atoms/cm³.

15. The method of claim 13 wherein the single crystal semiconductor handle substrate comprises the electrically active p-type dopant at a concentration of less than about 5×10^{12} atoms/cm³.

16. The method of claim 13 or claim 14 wherein the concentration of the electrically active n-type dopant in the epitaxial layer is less than about 1×10^{13} atoms/cm³.

17. The method of claim 13 or claim 14 wherein the concentration of the electrically active n-type dopant in the epitaxial layer is less than about 5×10^{12} atoms/cm³.
18. The method of claim 13 or claim 14 wherein the epitaxial layer comprises silicon.
19. The method of claim 18 wherein the epitaxial layer comprises silicon doped with carbon at a carbon concentration between about 0.1 mole % and about 5 mole %.
20. The method of claim 13 or claim 14 wherein the charge trapping layer has a resistivity of at least about 3000 ohm-cm.
21. The method of claim 13 or claim 14 wherein the charge trapping layer has a resistivity of at least about 7000 ohm-cm.
22. The method of claim 13 or claim 14 further comprising forming an insulating layer on the charge trapping layer prior to bonding with the dielectric layer on the front surface of the single crystal semiconductor donor substrate, wherein the insulating layer comprises semiconductor oxide or semiconductor oxynitride; wherein the insulating layer has a thickness between about 2000 angstroms and about 10,000 angstroms.
23. The method of claim 13 or claim 14 wherein the dielectric layer comprises a material selected from the group consisting of silicon dioxide, silicon nitride, silicon oxynitride, hafnium oxide, titanium oxide, zirconium oxide, lanthanum oxide, barium oxide, and a combination thereof; and wherein the dielectric layer has a thickness of at least about 10 nanometer thick, such as between about 10 nanometers and about 10,000 nanometers, between about 10 nanometers and about 5,000 nanometers, or between about 100 nanometers and about 400 nanometers.
24. The method of claim 13 or claim 14 further comprising heating the bonded structure at a temperature and for a duration sufficient to strengthen the bond

between the dielectric layer of the single crystal semiconductor donor substrate and the charge trapping layer on the front surface of the single crystal semiconductor handle substrate; and

further comprising mechanically cleaving the bonded structure at the cleave plane of the single crystal semiconductor donor substrate to thereby prepare a cleaved structure comprising the single crystal semiconductor handle substrate, the epitaxial layer, the charge trapping layer, the dielectric layer, and a single crystal semiconductor device layer.

25. A multilayer structure comprising:

a single crystal semiconductor handle substrate, wherein the single crystal semiconductor handle substrate comprises two major, generally parallel surfaces, one of which is a front surface of the single crystal semiconductor handle substrate and the other of which is a back surface of the single crystal semiconductor handle substrate, a circumferential edge joining the front surface and the back surface of the single crystal semiconductor handle substrate, a central plane between the front surface and the back surface of the single crystal semiconductor handle substrate, and a bulk region between the front and back surfaces of the single crystal semiconductor handle substrate, wherein the single crystal semiconductor handle substrate comprises an electrically active p-type dopant selected from the group consisting of boron, aluminum, gallium, indium, and any combination thereof and further wherein the single crystal semiconductor handle substrate has a handle crystal orientation, and;

an epitaxial layer in interfacial contact with the front surface of the single crystal semiconductor handle substrate, wherein the epitaxial layer comprises an electrically active n-type dopant selected from the group consisting of arsenic, phosphorus, antimony, and any combination thereof, wherein the concentration of the electrically active n-type dopant is less than about 1×10^{14} atoms/cm³ and further wherein the epitaxial layer has a crystal orientation that is the same as the handle crystal orientation;

a charge trapping layer in interfacial contact with the epitaxial layer, the charge trapping layer comprising polycrystalline silicon;

a dielectric layer in interfacial contact with the charge trapping layer; and
a single crystal semiconductor device layer in interfacial contact with the dielectric layer.

26. The multilayer structure of claim 25 wherein the single crystal semiconductor handle substrate comprises the electrically active p-type dopant at a concentration of less than about 2×10^{13} atoms/cm³.

27. The multilayer structure of claim 25 wherein the single crystal semiconductor handle substrate comprises the electrically active p-type dopant at a concentration of less than about 5×10^{12} atoms/cm³.

28. The multilayer structure of claim 25 or claim 26 wherein the concentration of the electrically active n-type dopant in the epitaxial layer is less than about 1×10^{13} atoms/cm³.

29. The multilayer structure of claim 25 or claim 26 wherein the concentration of the electrically active n-type dopant in the epitaxial layer is less than about 5×10^{12} atoms/cm³.

30. The multilayer structure of claim 25 or claim 26 wherein the epitaxial layer comprises silicon.

31. The multilayer structure of claim 30 wherein the epitaxial layer comprises silicon doped with carbon at a carbon concentration between about 0.1 mole % and about 5 mole %.

32. The multilayer structure of claim 25 or claim 26 wherein the charge trapping layer has a resistivity of at least about 3000 ohm-cm.

33. The multilayer structure of claim 25 or claim 26 wherein the charge trapping layer has a resistivity of at least about 7000 ohm-cm.

34. The multilayer structure of claim 25 or claim 26 wherein the dielectric layer comprises a material selected from the group consisting of silicon dioxide, silicon nitride, silicon oxynitride, hafnium oxide, titanium oxide, zirconium oxide, lanthanum oxide, barium oxide, and a combination thereof; and the dielectric layer has a thickness of at least about 10 nanometer thick, such as between about 10 nanometers and about 10,000 nanometers, between about 10 nanometers and about 5,000 nanometers, or between about 100 nanometers and about 400 nanometers.