What is claimed is:

1. A vertical memory device comprising:

an elongated vertical memory array block including vertical strings of memory cells extending through at least thirty-two conductive tiers; and

a stair step structure including contact regions of respective conductive tiers of the at least thirty-two conductive tiers,

wherein the elongated vertical memory array block has a lateral width of about 5 µm or less.

2. The vertical memory device of claim 1, wherein the elongated vertical memory array block has a lateral width of about 3 µm or less.

3. The vertical memory device of claim 1, wherein the vertical strings of memory cells extend through sixty-four conductive tiers.

4. The vertical memory device of claim 1, wherein the vertical strings of memory cells extend through one hundred twenty-eight conductive tiers.

5. The vertical memory device of any of claims 1 through 4, wherein the vertical memory device comprises multiple stair step structures, each of the multiple stair step structures including contact regions of a portion of the at least thirty-two conductive tiers.

6. The vertical memory device of any of claims 1 through 4, wherein the stair step structure is positioned along a lateral side surface of the elongated vertical memory array block.

7. The vertical memory device of any of claims 1 through 4, further comprising at least thirty-two access lines electrically coupled to the at least thirty-two conductive tiers, respectively, adjacent access lines of the at least thirty-two access lines separated by a distance of at least 100 nm.

8. The vertical memory device of any of claims 1 through 4, further comprising eight or fewer upper select gates extending over the elongated vertical memory array block and coupled to the vertical strings of memory cells.

9. A semiconductor device comprising:

a memory array block including at least sixteen continuous conductive tiers and two stair step structures defining contact regions to the at least sixteen continuous conductive tiers, the two stair step structures located between longitudinal ends and between two longitudinal portions of the at least sixteen continuous conductive tiers of the memory array block; and

sixteen access lines electrically coupled to respective contact regions defined by the two stair step structures,

wherein a portion of the memory array block lacks a stair step structure and is located between the two stair step structures.

10. The semiconductor device of claim 9, wherein the memory array block comprises at least four stair step structures.

11. The semiconductor device of claim 9 or claim 10, wherein the at least sixteen continuous conductive tiers comprise at least sixteen word line tiers.

12. A method of forming a semiconductor device structure, the method comprising:

forming a stack of alternating conductive tiers and insulating materials;

patterning the stack of alternating conductive tiers and insulating materials to form an elongated memory array block; and

forming a stair step structure between longitudinal ends of the elongated memory array block and between lateral side surfaces of the elongated memory array block to define contact regions of respective conductive tiers of the stack of alternating conductive tiers and insulating materials, wherein the alternating conductive tiers of the stack are continuous from one longitudinal side of the stair step structure to an opposing longitudinal side of the stair step structure.

13. The method of claim 12, wherein forming a stair step structure between lateral side surfaces of the elongated memory array block comprises forming the stair step structure along one of the lateral side surfaces of the elongated memory array block.

14. The method of claim 12, further comprising laterally recessing the stair step structure from a plane defined by one of the lateral side surfaces of the elongated memory array block.

15. The method of any of claims 12 through 14, further comprising electrically coupling access lines to respective contact regions defined by the stair step structure.

16. The method of claim 15, further comprising forming the access lines to have a distance between adjacent access lines of at least about 100 nm.

17. The method of any of claims 12 through 14, wherein:

forming a stack of alternating conductive tiers and insulating materials comprises forming at least thirty-two conductive tiers; and

patterning the stack of alternating conductive tiers and insulating materials to form an elongated memory array block comprises forming the elongated memory array block to have a lateral width of about 5 µm or less.

18. A method of operating a semiconductor device, the method comprising accessing a memory cell of a three-dimensional memory array block defined by an elongated stack of continuous conductive tiers, the three-dimensional memory array block including a stair step structure positioned between longitudinal ends of the three-dimensional memory array block, the stair step structure defining contact regions for electrically accessing respective conductive tiers of the elongated stack of continuous conductive tiers, wherein the stair step structure is positioned longitudinally between a first portion of vertical strings of memory cells of the three-dimensional memory array block including the accessed memory cell and a second portion of vertical strings of memory cells of the three-dimensional memory array block.

19. The method of claim 18, wherein accessing a memory cell includes performing an operation that is selected from the group consisting of a read operation, a write operation, and an erase operation.

20. The method of claim 18 or claim 19, wherein accessing a memory cell comprises applying a voltage to at least one access line of access lines respectively coupled to the contact regions of the stair step structure, the access lines being separated from each other by at least about 100 nm and including outer vertical portions extending along a lateral side surface of the three-dimensional memory array block.