CLAIMS:

1. A computing system comprising:

a battery to supply power to the computing system;

a processor to run an operating system (OS);

a basic input/output system (BIOS) comprising:

an interceptor, implemented in one or more of configurable logic or fixed-functionality hardware logic, to assume control over the processor in response to an OS request to transition the processor into a sleeping state;

a transitioner, implemented in one or more of configurable logic or fixed-functionality hardware logic, to transition the processor into an intermediate state that has a shorter wake latency than the sleeping state, wherein the transitioner includes a device power saver, implemented in one or more of configurable logic or fixed-functionality hardware logic, to perform one or more device power lowering operations including issuance of embedded controller (EC) power commands; and

a wake unit, implemented in one or more of configurable logic or fixed-functionality hardware logic, to maintain the processor in the intermediate state until a wake event is detected, wherein the transitioner is to transfer control over the processor to the OS in parallel with the device power saver reversing one or more of the power lowering operations, and without BIOS re-authentication.

2. The computing system of claim 1, wherein the BIOS further includes a resume unit, implemented in one or more of configurable logic or fixed-functionality hardware logic, to reverse one or more power lowering operations in response to the wake event, wherein the one or more power lowering operations are to restore memory configuration data from a non-volatile memory.

3. The computing system of claim 1, wherein the transitioner includes:

a state clearer, implemented in one or more of configurable logic or fixed-functionality hardware logic, to conduct a reset of the processor;

a resume unit, implemented in one or more of configurable logic or fixed-functionality hardware logic, to perform one or more processor resume operations, including to restore memory configuration data;

a processor power saver, implemented in one or more of configurable logic or fixed-functionality hardware logic, to perform one or more processor power lowering operations including power rail modifications to reduce a power consumption of the processor; and

a handoff unit, implemented in one or more of configurable logic or fixed-functionality hardware logic, to transfer control over the processor to the OS in response to the wake event.

4. The computing system of claim 3, wherein the sleeping state is to be an Advanced Configuration and Power Interface (ACPI) S3 state.

5. The computing system of claim 1, wherein the transitioner include:

a processor power saver, implemented in one or more of configurable logic or fixed-functionality hardware logic, to perform one or more processor power lowering operations including power rail modifications to reduce a power consumption of the processor.

6. The computing system of claim 5, wherein the sleeping state is to be an Advanced Configuration and Power Interface (ACPI) S1 state, wherein, when the requested sleeping state is the ACPI S1 state, a state clearer, implemented in one or more of configurable logic or fixed-functionality hardware logic, to conduct a reset of the processor is to be bypassed.

7. A method of operating a basic input/output system (BIOS), comprising:

assuming control over a processor in response to an operating system (OS) request to transition the processor into a sleeping state;

transitioning the processor into an intermediate state that has a shorter wake latency than the sleeping state by performing one or more device power lowering operations including issuance of embedded controller (EC) power commands; and

maintaining the processor in the intermediate state until a wake event is detected, wherein control over the processor is to be transferred to the OS in parallel with the device power saver reversing one or more of the power lowering operations, and without BIOS re-authentication.

8. The method of claim 7, further including reversing one or more power lowering operations in response to the wake event, wherein the one or more power lowering operations include restoring memory configuration data from a non-volatile memory.

9. The method of claim 7, wherein transitioning the processor into the intermediate state includes:

conducting a reset of the processor;

performing one or more processor resume operations, including to restore memory configuration data; performing one or more processor power lowering operations including power rail modifications to reduce a power consumption of the processor; and

transferring control over the processor to the OS.

10. The method of claim 9, wherein the sleeping state is an Advanced Configuration and Power Interface (ACPI) S3 state.

11. The method of claim 7, wherein transitioning the processor into the intermediate state includes:

performing one or more processor power lowering operations including power rail modifications to reduce a power consumption of the processor.

12. The method of claim 11, wherein the sleeping state is an Advanced Configuration and Power Interface (ACPI) S1 state, and wherein, when the sleeping state is the ACPI S1 state, a state clearer, implemented in one or more of configurable logic or fixed-functionality hardware logic, to conduct a reset of the processor is to be bypassed.

13. At least one non-transitory computer readable storage medium comprising a set of basic input/output system (BIOS) instructions which, when executed by a computing system, cause the computing system to:

assume control over a processor in response to an operating system (OS) request to transition the processor into a sleeping state;

transition the processor into an intermediate state that has a shorter wake latency than the sleeping state and perform one or more device power lowering operations including issuance of embedded controller (EC) power commands; and

maintain the processor in the intermediate state until a wake event is detected, wherein control over the processor is to be transferred to the OS in parallel with the device power saver reversing one or more of the power lowering operations, and without BIOS re-authentication.

14. The at least one non-transitory computer readable storage medium of claim 13, wherein the BIOS instructions, when executed, cause a computing system to reverse one or more power lowering operations in response to the wake event, wherein the one or more power lowering operations include restoring memory configuration data from a non-volatile memory.

15. The at least one non-transitory computer readable storage medium of claim 13, wherein the BIOS instructions, when executed, cause a computing system to:

conduct a reset of the processor;

perform one or more processor resume operations, including to restore memory configuration data;

perform one or more processor power lowering operations including power rail modifications to reduce a power consumption of the processor; and

transfer control over the processor to the OS.

16. The at least one non-transitory computer readable storage medium of claim 15, wherein the sleeping state is to be an Advanced Configuration and Power Interface (ACPI) S3 state.

17. The at least one non-transitory computer readable storage medium of claim 13, wherein the BIOS instructions, when executed, cause a computing system to: perform one or more processor power lowering operations including power rail modifications to reduce a power consumption of the processor.

18. The at least one non-transitory computer readable storage medium of claim 17, wherein the sleeping state is to be an Advanced Configuration and Power Interface (ACPI) S1 state, wherein, when the sleeping state is the ACPI S1 state, a state clearer, implemented in one or more of configurable logic or fixed-functionality hardware logic, to conduct a reset of the processor is to be bypassed.

19. A basic input/output system (BIOS) apparatus comprising:

an interceptor, implemented in one or more of configurable logic or fixed-functionality hardware logic, to assume control over a processor in response to an operating system (OS) request to transition the processor into a sleeping state;

a transitioner, implemented in one or more of configurable logic or fixed-functionality hardware logic, to transition the processor into an intermediate state that has a shorter wake latency than the sleeping state, wherein the transitioner includes a device power saver, implemented in one or more of configurable logic or fixed-functionality hardware logic, to perform one or more device power lowering operations including issuance of embedded controller (EC) power commands; and

a wake unit, implemented in one or more of configurable logic or fixed-functionality hardware logic, to maintain the processor in the intermediate state until a wake event is detected, wherein the transitioner is to transfer control over the processor to the OS in parallel with

the device power saver reversing one or more of the power lowering operations, and without BIOS re-authentication.

20. The apparatus of claim 19, further including a resume unit, implemented in one or more of configurable logic or fixed-functionality hardware logic, to reverse one or more power lowering operations in response to the wake event, wherein the one or more power lowering operations include to restore memory configuration data from a non-volatile memory.

21. The apparatus of claim 19, wherein the transitioner includes:

a state clearer, implemented in one or more of configurable logic or fixed-functionality hardware logic, to conduct a reset of the processor;

a resume unit, implemented in one or more of configurable logic or fixed-functionality hardware logic, to perform one or more processor resume operations, including to restore memory configuration data;

a processor power saver, implemented in one or more of configurable logic or fixed-functionality hardware logic, to perform one or more processor power lowering operations including power rail modifications to reduce a power consumption of the processor; and

a handoff unit, implemented in one or more of configurable logic or fixed-functionality hardware logic, to transfer control over the processor to the OS.

22. The apparatus of claim 21, wherein the sleeping state is to be an Advanced Configuration and Power Interface (ACPI) S3 state.

23. The apparatus of claim 19, wherein the transitioner includes:

a processor power saver, implemented in one or more of configurable logic or fixed-functionality hardware logic, to perform one or more processor power lowering operations including power rail modifications to reduce a power consumption of the processor.

24. The apparatus of claim 23, wherein the sleeping state is to be an Advanced Configuration and Power Interface (ACPI) S1 state, wherein, when the sleeping state is the ACPI S1 state, a state clearer, implemented in one or more of configurable logic or fixed-functionality hardware logic, to conduct a reset of the processor is to be bypassed.