

The present invention relates to a device made using MOS technology for detecting a high level of a supply voltage.

In practice, in an integrated circuit made using MOS technology, it is usually very difficult to detect precisely the high level of a voltage, in particular the supply voltage. This results from the fact that the parameters of the transistors are determined with a precision of about $\pm 20\%$, which makes it very difficult to design the provision of a reference voltage. Voltage sources are, however, usually produced with the help of MOS transistors. Furthermore, the higher the voltage is, the more often will there be variations of the reference voltage level. This is particularly objectionable in the case of integrated MOS circuits such as EPROM or EEPROM memories or the like in which a defined voltage V_{pp} is used for programming the cell and a different voltage, generally the supply voltage V_{cc} , is used for reading the cell. These memories are constructed in such a manner that it is possible to program them using a voltage V_{pp} of about 10 volts. This poses a problem if the read voltage V_{cc} can reach this value, because it is then possible to change the state of the memory cells. It is therefore necessary to limit the read voltage, that is to say the supply voltage, to a specific value, in this case less than 10 volts.

The aim of the present invention is to overcome these disadvantages by providing a device made using MOS technology for detecting the high level of a supply voltage which emits a signal when the high voltage level exceeds a predetermined value, it being possible to utilize this signal to block a circuit such as the read circuit in the case of EPROM or EEPROM memories.

Consequently an object of the present invention is a detection device as claimed in claim 1.

It will be noted that patent FR-A-2 254 792 describes a supply voltage threshold detector where the threshold is the sum of the threshold voltages of an N type MOS transistor and a P type MOS transistor.

In one embodiment of the present invention, the voltage source comprises n P type MOS transistors (where n is equal to or greater than 1) each formed in an N type island connected to the source of the corresponding transistor, and connected in series between the voltage V_{cc} and the output junction A and by an N type MOS transistor connected between the output junction A and the low voltage or ground, the gates of the P type and N type transistors being connected directly to the drain or the source of the corresponding transistor. Similarly, the means for providing at the output a logic level which switches over when the high level of the voltage V_{cc} exceeds a predetermined threshold comprises a first N type MOS transistor the gate of which is connected to the voltage source, the source of which is connected to the low voltage or ground through the intermediary of a means for raising its voltage as soon as a current appears, and the drain of which is connected to the supply terminal through the intermediary of a means forming a switch, the output being formed by the drain.

Preferably the means for raising the voltage of the source of the N type MOS transistor comprises another N type MOS transistor of which the gate is connected to the voltage V_{cc} , the source to the low voltage, and the drain to the source of the first N type transistor. The means forming a switch comprises a P type MOS transistor of which the source is connected to the voltage V_{cc} , the gate to the low voltage or ground, and the drain to the drain of the first transistor. In this case the P type MOS transistor has a W/L ratio much less than 1 and the first N type MOS transistor has a W/L ratio much greater than 1 in order to make it possible to obtain at the output either the voltage V_{cc} or the low voltage V_{ss} or ground depending on the conduction or non-conduction of the first N type MOS transistor.

Preferably the output of the means for supplying a logic level output which changes over when the high level of the supply voltage exceeds a predetermined threshold is connected to an inverter. In this case the means forming a switch may comprise a first P type MOS transistor of which the source is connected to the voltage V_{cc} , the gate

to the output of the inverter and the drain to the input of the inverter, and by a second P type MOS transistor which is connected in parallel to the first MOS transistor and the gate of which is connected to a signal allowing the initialization of the device. The first P type MOS transistor will be conductive or blocked depending on the output signal from the inverter. The second P type MOS transistor serves to initialize the circuit.

Other characteristics and advantages of the present invention will emerge on reading the following description of different embodiments with reference to the accompanying drawings in which:

- Figure 1 is a circuit diagram of a first embodiment of a detection circuit in accordance with the present invention, and

- Figure 2 is a circuit diagram of a second embodiment of a detection circuit in accordance with the present invention.

In order to simplify the description, similar elements in the two Figures have been given the same reference symbols.

As shown in Figure 1, the MOS circuit for detecting the high level of a voltage in accordance with the present invention substantially comprises a voltage source 1, a means for supplying at its output a logic level which switches over when the high level of the voltage V_{cc} exceeds a predetermined threshold and optionally an inverter I. More specifically, the voltage source 1 comprises n P type MOS transistors TP1, TP2, TP3, ..., TPn connected in series and by an N type MOS transistor TN1. The number n of P type transistors is chosen in accordance with the voltage V_{cc} the high level of which must be determined and in accordance with the threshold voltages of the different transistors.

More specifically, the P type transistor TP1 is connected in such a manner that its source is connected to the voltage V_{cc} and its drain is connected to the source of the P type transistor TP2, the drain of which

is connected to the source of the P type transistor TP3 and so on. The drain of the P type transistor TPn is connected to the junction point A forming the output of the voltage source. On the other hand, the gates of the transistors TP1 to TPn are each connected to the drain of the corresponding transistor. In accordance with the present invention, each transistor TP1 to TPn is formed in an independent N type island and each island is connected to the source of the corresponding P type transistor. Because of this, the threshold voltage of the P type transistors is determined exactly, because the substrate effect, that is to say the variation in the threshold voltage as a function of the source-substrate potential difference, is eliminated. On the other hand, the voltage source comprises an N type transistor TN1 the source of which is connected to a low voltage Vss or to ground, and the drain of which is connected to the output junction A. The gate of the transistor TN1 is connected to its drain. Preferably the transistors TP1 to TPn have the same threshold value.

In this case, the voltage at the junction A will have a value between Vss and VTN if $V_{cc} < n.V_{TP} + V_{TN}$ (transistors TN1 and TP1 are blocked) and will be equal to $V_{cc} - n.V_{TP}$ if $V_{cc} > n.V_{TP} + V_{TN}$, VTP being the threshold voltage of the P type transistors and VTN that of the N type transistor.

The said voltage source 1 is connected to the means 2 which comprises a first N type transistor TN2 the source of which is connected to the low voltage or ground through the intermediary of a second N type MOS transistor TN3 the gate of which is connected to the voltage Vcc which makes it permanently conductive. On the other hand, the drain of the transistor TN2 is connected to the drain of a P type transistor TP0 the source of which is connected to the voltage Vcc and the gate of which is connected to the low voltage or ground. The output of the means 2 is connected to the junction B between the transistors TP0 and TN2. Preferably, as shown in Figure 1, the junction B is connected to an inverter I and the output signal of the device is obtained from the output C of the inverter. The operation of the circuit shown in Figure 1 will now be explained.

With the circuit shown in Figure 1 it is possible to detect a voltage V_{cc} equal to $n.V_{TP} + V_{TN}$. If the voltage V_{cc} is less than $n.V_{TP} + V_{TN}$, there is no continuous current in any of the branches. The voltage at the junction A is less than V_{TN} , that is to say less than the threshold voltage of the N type transistor $TN1$. Because of this the transistor $TN2$ is blocked. On the other hand, the junction B has the value V_{cc} . In fact the transistor $TP0$ the gate of which is connected to ground is conductive and applies the voltage V_{cc} to the point B. Because the transistor $TN3$, the gate of which receives the voltage V_{cc} , is itself also conductive, it prevents conduction by the transistor $TN2$ by raising the voltage of its source as soon as a current appears.

If the voltage V_{cc} exceeds $n.V_{TP} + V_{TN}$ the voltage at the junction A increases and follows the rise in V_{cc} . The transistor $TN2$ then becomes unblocked and causes the voltage at the junction B to become V_{ss} . In fact the transistor $TN2$ has been designed in such a manner that its W/L ratio is very much greater than 1 whereas the W/L ratio of the transistor $TP0$ is very much less than 1, which makes it possible to compel the voltage at the junction B to change when the transistor $TN2$ conducts. By way of example, using 2 micron C-MOS technology, the P type MOS transistor $TP0$ has a W/L ratio = $2/25$ whereas the N type MOS transistor $TN2$ has a W/L ratio = $10/2$. The junction B being at V_{ss} , that is to say at the logic level "0", at the output of the inverter a logic level "1" is obtained, that is to say a detection signal which may be used to block a circuit.

In order to block the P type transistor $TP0$ after the detection of a voltage V_{cc} greater than $n.V_{TP} + V_{TN}$, the circuit shown in Figure 2 may be used. In this case the inverter I forms an integral part of the circuit for detecting the high level and the gate of the P type transistor $TP5$ used instead of the transistor $TP0$ is connected to the output C of the inverter I instead of being connected to the low voltage or ground. However, in order to initialize the system, a P type transistor $TP6$ is used the source of which is connected to the voltage V_{cc} and the drain of which is connected to the junction B, the gate of the transistor $TP6$ being connected to a signal R for resetting to

zero. The transistor TP6 makes it possible to set the junction B at the voltage V_{cc} at the start of operation of the detection circuit. Then, when the junction changes to V_{ss} , the level on the output C of the inverter changes to the level 1 which blocks the transistor TP5 and maintains the junction B at V_{ss} .

The circuit described above with reference to Figures 1 and 2 has numerous advantages:

- the detection voltage is such that $V = (nV_{TP} + V_{TN}) \pm 10\%$. In fact the threshold voltages of the P type transistors or the N type transistors are in general controlled very precisely especially in the case of well stabilized manufacturing processes.

- the static consumption of the circuit is zero until the circuit detects that the voltage V_{cc} exceeds the predetermined threshold. In normal operation the above circuit is not used. In financial applications using plastic cards the circuit may be used as a security device.



CLAIMS

1. A device made using MOS technology for detecting a high level of a supply voltage V_{CC} comprising, between a supply terminal receiving this voltage and a ground terminal, a series connected arrangement of an N type MOS transistor (TN1) and a reference voltage source, characterized in that the reference voltage source comprises a plurality of P type MOS transistors (TP1 to TPn) each formed in an N type island separated from the others, the island being connected to the source of the corresponding transistor, the gate and the drain of each transistor being connected so that the device supplies at its output a logic level which switches when the high level of the voltage V_{CC} exceeds a predetermined threshold.

2. A device as claimed in claim 1, characterized in that it comprises a second N type MOS transistor (TN2) the gate of which is connected to the junction point between the first N type transistor and the P type transistors, the source of which is connected to ground through the intermediary of a means (TN3) raising its voltage as soon as a current appears, and the drain of which, forming the output of the device, is connected to the supply terminal through the intermediary of a switch (TP0; TP5, TP6).

3. A device as claimed in claim 2, characterized in that the means for raising the voltage at the source of the second MOS transistor of N type conductivity (TN2) comprises a third MOS transistor of the same type (TN3) of which the gate is connected to the supply terminal, the source to ground, and the drain to the source of the second N type transistor.

4. A device as claimed in claim 2, characterized in that the switch comprises a P type MOS transistor (TP0) of which the source is connected to the supply terminal, the gate to ground, and the drain to the drain of the second N type transistor.



5. A device as claimed in claim 4, characterized in that the transistor (TP0) comprising the switch has a channel width to channel length ratio W/L much less than 1 and the second N type transistor has a channel width to channel length ratio W/L much greater than 1.

6. A device as claimed in claim 5, characterized in that in the case of the transistor comprising the switch the width to length ratio W/L much smaller than 1 is $2/25$ and in the case of the second N type transistor the ratio W/L much greater than 1 is 5.

7. A device as claimed in claim 2, characterized in that the switch comprises a first P type conductivity transistor (TP5), the source of which is connected to the supply terminal, the gate being connected to the output of an inverter the input of which is connected to the drain of the second N type transistor (TN2), and the drain being connected to the input of the inverter, and by a second P type conductivity transistor (TP6) which is connected in parallel to the first and the gate of which can receive a signal allowing the initialization of the device.