WHAT IS CLAIMED IS:

1. An integrated circuit device comprising:

a plurality of conductive lines extending in a horizontal direction parallel to a main surface of a substrate and overlapping one another in a vertical direction vertical to the main surface, on the substrate;

a plurality of insulation layers each between two adjacent conductive lines of the plurality of conductive lines to extend in the horizontal direction;

a channel layer extending in the vertical direction in a channel hole passing through the plurality of conductive lines and the plurality of insulation layers;

a plurality of outer blocking dielectric layers between the plurality of conductive lines and the channel layer, the plurality of outer blocking dielectric layers surrounding at least some of the plurality of conductive lines; and

a plurality of inner blocking dielectric layers extending in an extension direction of the channel layer between the plurality of conductive lines and the channel layer, in the channel hole,

wherein a width of each of the plurality of outer blocking dielectric layers in the horizontal direction increases toward the main surface.

2. The integrated circuit device of claim 1,

wherein the channel hole has a tapered shape of which a diameter is reduced toward the main surface of the substrate, and

a width of each of the plurality of inner blocking dielectric layers in the horizontal direction decreases toward the main surface.

3. The integrated circuit device of claim 1 or claim 2, wherein

the plurality of outer blocking dielectric layers are not provided in a conductive line at an upper end among the plurality of conductive lines.

4. The integrated circuit device of claim 3, wherein

the conductive line at the upper end is inserted into a portion of a corresponding inner blocking dielectric layer and comprises a sidewall convex toward the channel layer.

5. The integrated circuit device of any one of claims 1 to 4, wherein

a thickness of each of the plurality of conductive lines in the vertical direction decreases toward the main surface.

6. The integrated circuit device of any one of claims 1 to 4, wherein

thicknesses of the plurality of conductive lines in the vertical direction are substantially the same.

7. The integrated circuit device of any one of claims 1 to 6, wherein

a material comprised in each of the plurality of inner blocking dielectric layers is substantially the same as a material comprised in each of the plurality of outer blocking dielectric layers, and

an etch rate of each of the plurality of inner blocking dielectric layers differs from an etch rate of each of the plurality of outer blocking dielectric layers.

8. The integrated circuit device of any one of claims 1 to 7, further comprising

a semiconductor pattern at a lower end of the channel layer to partially fill the channel hole,

wherein each of the plurality of outer blocking dielectric layers is between the semiconductor pattern and a corresponding conductive line.

9. The integrated circuit device of claim 8, further comprising

a gate dielectric layer at a portion where the semiconductor pattern contacts each of the plurality of outer blocking dielectric layers,

wherein the gate dielectric layer is inserted into a portion of the semiconductor pattern and comprises a convex sidewall.

10. The integrated circuit device of any one of claims 1 to 9, further comprising

a tunneling dielectric layer and a charge storage layer each extending in the extension direction of the channel layer, between the channel layer and each of the plurality of inner blocking dielectric layers.

11. An integrated circuit device comprising:

a first stacked structure comprising a plurality of first conductive lines extending in a first direction in parallel with a main surface of a substrate and overlapping one another in a vertical direction vertical to the main surface, on the substrate;

a second stacked structure comprising a plurality of second conductive lines extending in the first direction in parallel with the main surface of the substrate and overlapping one another in the vertical direction vertical to the main surface, on the first stacked structure;

a channel layer extending in the vertical direction in a channel hole passing through the first and second stacked structures;

a plurality of outer blocking dielectric layers between the plurality of first and second conductive lines and the channel layer, the plurality of outer blocking dielectric layers surrounding all of the plurality of first conductive lines and at least some of the plurality of second conductive lines; and

an inner blocking dielectric layer extending in an extension direction of the channel layer between the plurality of first and second conductive lines and the channel layer, in the channel hole,

wherein a width of each of the plurality of outer blocking dielectric layers in a horizontal direction increases toward the main surface.

12. The integrated circuit device of claim 11, wherein

the channel hole comprises:

a first channel hole passing through the first stacked structure; and

a second channel hole passing through the second stacked structure,

each of the first and second channel holes has a tapered shape of which a diameter is reduced toward the main surface, and

a width of the inner blocking dielectric layer in the horizontal direction decreases toward the main surface.

13. The integrated circuit device of any one of claims 11 to 12, wherein

the plurality of outer blocking dielectric layers are not provided in a second conductive line at an upper end among the plurality of second conductive lines.

14. The integrated circuit device of any one of claims 11 to 13, wherein

a material comprised in the inner blocking dielectric layer is substantially the same as

a material comprised in each of the plurality of outer blocking dielectric layers, and

an etch rate of the inner blocking dielectric layer differs from an etch rate of each of the plurality of outer blocking dielectric layers.

15. An integrated circuit device comprising:

a plurality of conductive lines extending in a horizontal direction parallel to a main surface of a substrate and overlapping one another in a vertical direction vertical to the main surface, on the substrate;

a plurality of insulation layers each between two adjacent conductive lines of the plurality of conductive lines to extend in the horizontal direction;

a channel layer extending in the vertical direction in a channel hole passing through the plurality of conductive lines and the plurality of insulation layers;

a charge storage layer and a first blocking dielectric layer each extending in an extension direction of the channel layer between the plurality of conductive lines and the channel layer, in the channel hole; and

a plurality of second blocking dielectric layers between the plurality of conductive lines and the first blocking dielectric layer and between the plurality of conductive lines and the plurality of insulation layers, in at least some of the plurality of conductive lines,

wherein, with respect to the channel hole, a first width of a second blocking dielectric layer of an uppermost conductive line among the plurality of conductive lines operating as a memory cell is set in the horizontal direction,

a second width of a second blocking dielectric layer of a lowermost conductive line among the plurality of conductive lines operating as a memory cell is set in the horizontal direction,

a third width of a second blocking dielectric layer of a center conductive line closest to the uppermost conductive line and the lowermost conductive line in the vertical direction is set in the horizontal direction,

the third width is greater than the first width, and

the second width is greater than the third width.

16. The integrated circuit device of claim 15, wherein

the first blocking dielectric layer is continuous along an inner portion of the channel hole, with respect to the channel hole.

17. The integrated circuit device of any one of claims 15 to 16, wherein

a sum of a vertical-direction thickness of each of the plurality of conductive lines and a vertical-direction thickness of a second blocking dielectric layer surrounding a corresponding conductive line is substantially constant, with respect to the channel hole.

18. The integrated circuit device of any one of claims 15 to 17, wherein

the charge storage layer comprises silicon nitride,

the first blocking dielectric layer and the plurality of second blocking dielectric layers each comprise silicon oxide, and

an etch rate of the first blocking dielectric layer differs from an etch rate of each of the plurality of second blocking dielectric layers.

19. The integrated circuit device of any one of claims 15 to 18, wherein

a width of each of the plurality of second blocking dielectric layers in the horizontal direction is about 100nm or less, and

a width of each of at least some of the plurality of second blocking dielectric layers in the horizontal direction is about 60nm or less.