is an integer equal to or greater than six), and the parity data PRT includes (p+2)-bit parity bits. In other exemplary embodiments, the main data MD includes $3*2^q$-bit off the data bits (where q is an integer equal to or greater than five), and the parity data PRT includes (q+2)-bit parity bits.

**[0063]** FIG. 9 illustrates relationships of the first ECC, and the parity bits used in the error correction circuit of FIG. 7, according to exemplary embodiments of the present disclosure. In FIG. 9, it is assumed that the main data MD includes a plurality of sub data units SDU1~SDUx, and the parity data PRT includes 8-bit parity bits PB1~PB8. In FIG. 9, it is assumed that x is a natural number equal to or greater than six. Referring to FIG. 9, the first ECC 415 may be divided into a plurality of code groups CG1~CGx corresponding to the plurality of sub data units SDU1~SDUx.

**[0064]** FIG 10 illustrates an example of the first ECC according to exemplary embodiments of the present disclosure. In FIG. 10, it is assumed that the main data MD includes 64-bit data bits d0~d63. That is, it is assumed that x is six (6) in FIG. 10. Referring to FIG. 10, the data bits d0~d63 of the main data MD may be divided into first through eighth sub data units SDU11~SDU18. Each of the first through eighth sub data units SDU11~SDU18 includes 8-bit data bits. A first ECC ECC1a includes first through eighth code groups CG11~CG18 corresponding to the first through eighth sub data units SDU11~SDU18.

**[0065]** FIGS. 11A and 11B illustrate the first through eighth code groups in FIG. 10.

**[0066]** Referring to FIG. 11A and 11B, the first code group CG11 includes column vectors CV11~CV18 corresponding to the data bits d0~d7 of the first sub data unit SDU11, the second code group CG12 includes column vectors CV21~CV28 corresponding to the data bits d8~d15 of the second sub data unit SDU12, the third code group CG13 includes column vectors CV31~CV38 corresponding to the data bits d16~d23 of the third sub data unit SDU13, and the fourth code group CG14 includes column vectors CV41~CV48 corresponding to the data bits d24~d31 of the fourth sub data unit SDU14.

**[0067]** In addition, the fifth code group CG15 includes column vectors CV51~CV58 corresponding to the data bits d32~d39 of the fifth sub data unit SDU15, the sixth code group CG16 includes column vectors CV61~CV68 corresponding to the data bits d40~d47 of the sixth sub data unit SDU16, the seventh code group CG17

What Is Claimed Is:

1. An error correction circuit, comprising:

an error correction code (ECC) memory configured to store an ECC represented by a generation matrix; and

an ECC engine configured to generate parity data from main data using the ECC, and to use the parity data to detect and/or correct at least one error bit in the main data;

wherein the main data includes a plurality of data bits divided into a plurality of sub data units;

wherein the ECC includes a plurality of column vectors divided into a plurality of code groups corresponding to respective ones of the sub data units;

wherein the column vectors have elements configured to gather a mis-corrected bit and multiple error bits in one symbol; and

wherein the mis-corrected bit is generated when the multiple error bits are present in the main data,

wherein the one symbol includes one of the sub data units or two adjacent sub data units of the sub data units; wherein the multiple error bits include odd error bits; and wherein the column vectors have elements configured to place the mis-corrected bit in a sub data unit including the multiple error bits.

2. The error correction circuit of claim 1,

wherein the multiple error bits include a first error bit, a second error bit and a third error bit;

wherein when a first sub data unit of the sub data units includes the first error bit, the second error bit and the third error bit, a first code group corresponding to the first sub data unit includes a plurality of first column vectors; and

wherein the plurality of first column vectors are configured such that a result of a bit-wise exclusive OR operation on three different column vectors of the first column vectors matches one of the column vectors of the first column vectors except the three different column vectors.

3. The error correction circuit of claim 1,

wherein the multiple error bits include a first error bit, a second error bit and a third error bit;

wherein when a first sub data unit and a second sub data unit of the sub data units includes the first error bit, the second error bit and the third error bit, a first code group of the plurality of code groups, corresponding to the first sub data unit, includes a plurality of first column vectors, and a second code group of the plurality of code groups, corresponding to the second sub data unit, includes a plurality of second column vectors; and

wherein the plurality of first column vectors and the plurality of second column vectors are configured such that a result of a bit-wise exclusive OR operation on three different column vectors of the first column vectors and the second column vectors matches one of column vectors of the first column vectors and the second column vectors except the three different column vectors.

4. The error correction circuit of any one of claims 1 to 3, wherein the main data includes $2^p$-bits of the data bits, wherein p is an integer equal to six; wherein the parity data includes (p+2)-bit parity bits; wherein the ECC is a single error correction and double error detection (SECDED) code; wherein the sub data units include first through eighth sub data units, and each of the first through eighth sub data units includes (p+2) bits; and wherein the code groups include first through eighth code groups corresponding to the first through eighth sub data units, respectively.

5. The error correction circuit of claim 4, wherein each of the first through eighth code groups includes first through (p+2)-th column vectors; and wherein each of the first through (p+2)-th column vectors includes (p+2) elements.

6. The error correction circuit of any one of claims 1 to 3, wherein the main data includes $3*2^q$-bit of the data bits, wherein q is an integer equal to five; wherein the parity data includes (q+2)-bit parity bits; wherein the ECC is a single error correction and double error detection (SECDED) code; wherein the sub data units include first through twelfth sub data units, and each of the first through twelfth sub data units includes (q+3) bits; and wherein the plurality of code groups include first through twelfth code groups corresponding to the first through twelfth sub data units, respectively.

7. The error correction circuit of claim 6, wherein each of the first through twelfth code groups includes first through (q+3)-th column vectors; and wherein each of the first through (q+3)-th column vectors includes (q+3) elements.

8. The error correction circuit of any one of claims 1 to 7, wherein the ECC engine comprises:

an ECC encoder configured to perform an ECC encoding operation on the main data using the ECC to generate the parity data during a memory write operation; and

an ECC decoder configured to perform an ECC decoding operation on the main data based on the parity data using the ECC during a memory read operation.

9. The error correction circuit of claim 8, wherein the ECC decoder comprises:

a check bit generator configured to generate check bits based on the main data using the ECC;

a syndrome generator configured to generate syndrome data based on a comparison of the check bits and the parity data; and

a data corrector configured to correct the at least one error bit in the main data.

10. A semiconductor memory device, comprising:

a memory cell array including a plurality of bank arrays that respectively comprise a normal cell region, which stores main data, and a redundancy cell region, which stores first parity data associated with the corresponding main data and each of the plurality of bank arrays includes a plurality of dynamic memory cells coupled to word-lines and bit-lines;

an error correction circuit configured to generate the parity data based on the main data using an error correction code (ECC), and to correct at least one error bit in the main data using the parity data, wherein the ECC is represented by a generation matrix; and

a control logic circuit configured to control the error correction circuit based on a command and an address;

wherein the main data includes a plurality of data bits divided into a plurality of sub data units;

wherein the ECC includes a plurality of column vectors divided into a plurality of code groups corresponding to the sub data units; and

wherein the column vectors have elements configured to gather a mis-corrected bit and multiple error bits in one symbol, wherein the mis-corrected bit is generated due to the multiple error bits in the main data,

wherein the one symbol includes one of the sub data units or two adjacent sub data units of the sub data units;

the multiple error bits include odd error bits; and

the column vectors have elements configured to place the mis-corrected bit in a sub data unit including the multiple error bits.

11. The semiconductor memory device of claim 10, wherein the multiple error bits include a first error bit, a second error bit and a third error bit; wherein when a first sub data unit of the sub data units includes the first error bit, the second error bit and the third error bit, a first code group corresponding to the first sub data unit includes a plurality of first column vectors; and wherein the plurality of first column vectors are configured such that a result of a bit-wise exclusive OR operation on three different column vectors of the first column vectors matches one of the column vectors of the first column vectors except the three different column vectors.

12. The semiconductor memory device of claim 10 or claim 11, wherein the main data includes $2^p$-bit of the data bits, wherein p is an integer equal to six; wherein the parity data includes (p+2)-bit parity bits; wherein the ECC is a single error correction and double error detection (SECDED) code; wherein the sub data units include first through eighth sub data units, and each of the first through eighth sub data units includes (p+2) bits; and wherein the code groups include first through eighth code groups corresponding to the first through eighth sub data units, respectively.

13. The semiconductor memory device of any one of claims 10 to 12, comprising:

at least one buffer die; and

a plurality of memory dies, the plurality of memory dies being stacked on the at least one buffer die and conveying data through a plurality of through silicon via (TSV) lines;

wherein each of the plurality of memory dies includes the memory cell array, and

wherein the at least one buffer die includes the error correction circuit.

14. A memory system, comprising:

a semiconductor memory device; and

a memory controller configured to control the semiconductor memory device;

wherein the semiconductor memory device includes:

a memory cell array including a plurality of bank arrays,

wherein each of the plurality of bank arrays includes a normal cell region that stores main data, and a redundancy cell region that stores first parity data associated with the main data, and wherein each of the plurality of bank arrays includes a plurality of dynamic memory cells coupled to word-lines and bit-lines;

an error correction circuit configured to generate the parity data based on the main data using a first error correction code (ECC), and to correct at least one error bit in the main data using the parity data, wherein the first ECC is represented by a generation matrix; and

a control logic circuit configured to control the error correction circuit based on a command and an address provided from the memory controller;

wherein the main data includes a plurality of data bits divided into a plurality of sub data units;

wherein the first ECC includes a plurality of column vectors divided into a plurality of code groups corresponding to the sub data units, and

wherein the column vectors have elements configured to gather a mis-corrected bit and multiple error bits in one symbol, wherein the mis-corrected bit is generated due to the multiple error bits in the main data,

wherein the one symbol includes one of the sub data units or two adjacent sub data units of the sub data units;

the multiple error bits include odd error bits; and

the column vectors have elements configured to place the mis-corrected bit in a sub data unit including the multiple error bits.

15. The memory system of claim 14, wherein:

the first ECC is a single error correction and double error detection (SECDED) code.

16. The memory system of claim 14 or claim 15,

wherein the memory controller includes a second error correction circuit;

wherein the second error correction circuit includes:

a parity generator configured to generate a system parity data based on the main data to be transmitted to the semiconductor memory device using a second ECC;

a buffer configured to store the system parity data; and

an ECC decoder configured to generate check bits based on a read main data received from the semiconductor memory device using the second ECC, and configured to correct multiple error bits in the read main data based on comparison of the check bits and the system parity data.

17. The memory system of claim 16, wherein the second ECC is a code that corrects the multiple error bits in the read main data by symbol basis.

18. The memory system of claim 17, wherein:

the ECC decoder is configured to assign one or two of a plurality sub data units in the read main data as one symbol, and is further configured to correct the multiple error bits in the one symbol.