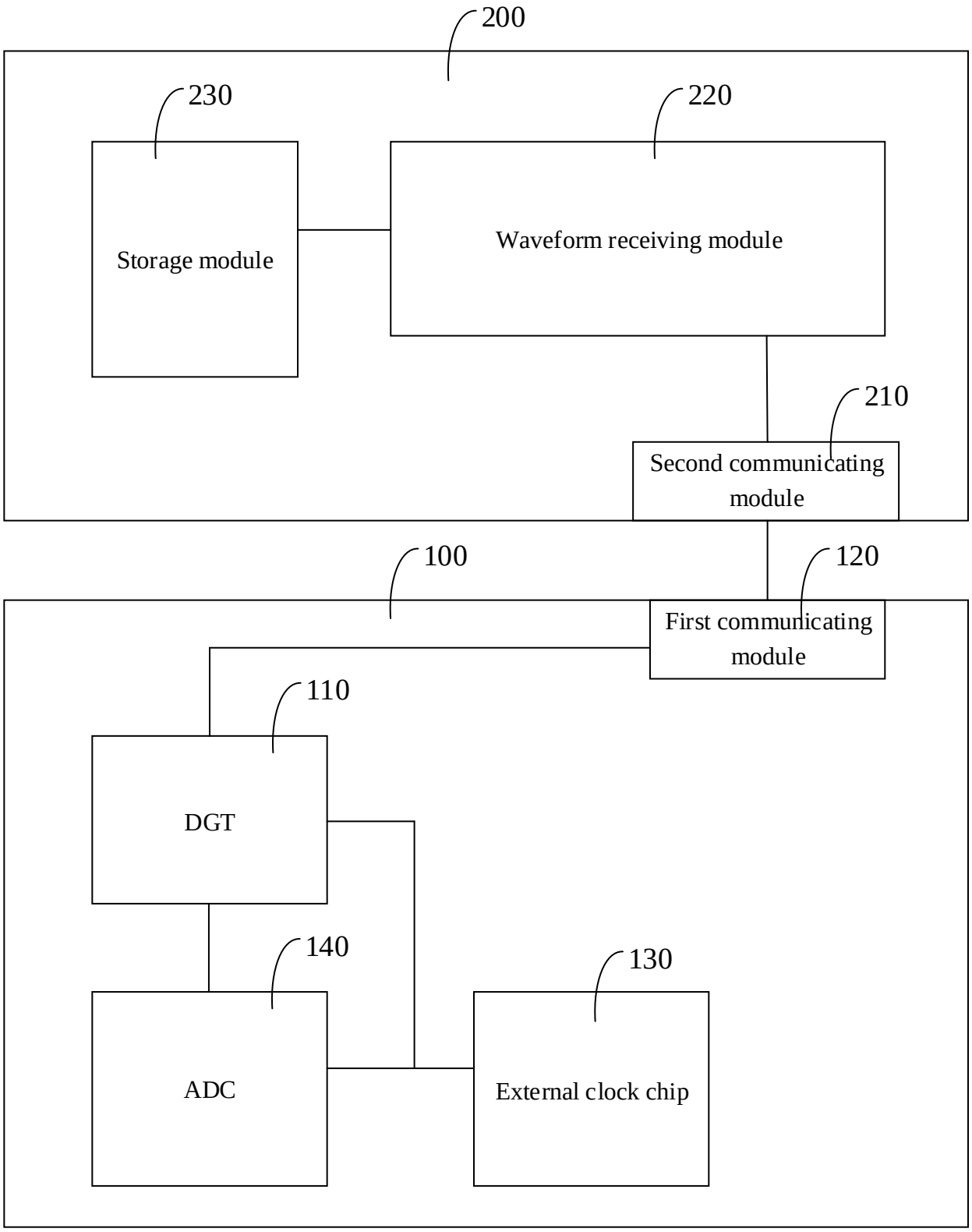

200
230
220
Storage module
Waveform receiving module
210
Second communicating module
100
120
First communicating module
110
DGT
140
130
ADC
External clock chip

FIG. 1

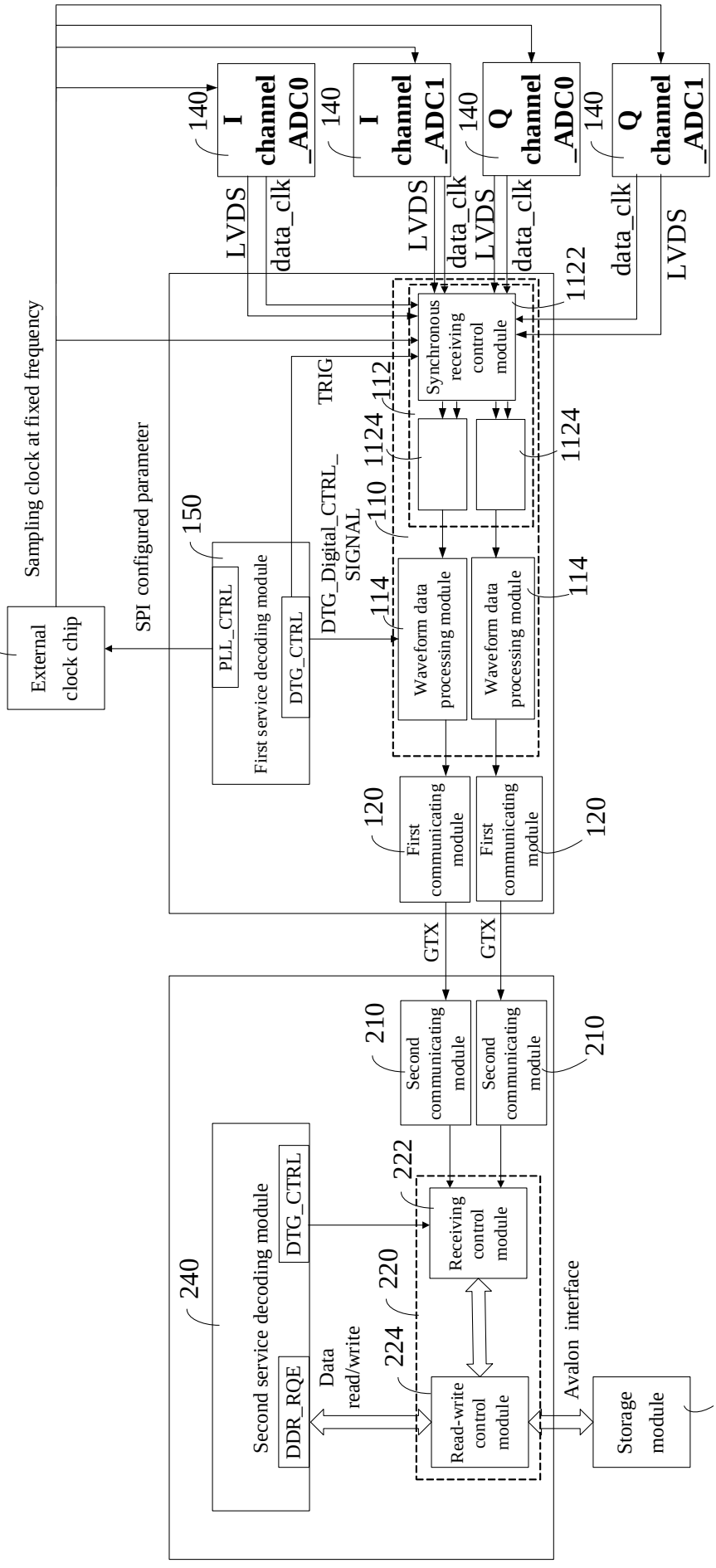

130
External clock chip
Sampling clock at fixed frequency
SPI configured parameter
150
First service decoding module
PLL_CTRL
DTG_CTRL
DTG_Digital_CTRL_SIGNAL
TRIG
110
112
Synchronous receiving control module
1122
1124
1124
114
Waveform data processing module
Waveform data processing module
114
120
First communicating module
First communicating module
120
GTX
GTX
210
Second communicating module
Second communicating module
210
240
Second service decoding module
DDR_RQE
DTG_CTRL
Data read/write
222
Receiving control module
220
224
Read-write control module
Avalon interface
230
Storage module
140
I channel _ADC0
140
I channel _ADC1
140
Q channel _ADC0
140
Q channel _ADC1
LVDS
data_clk
LVDS
data_clk
LVDS
data_clk
data_clk
LVDS

FIG. 2

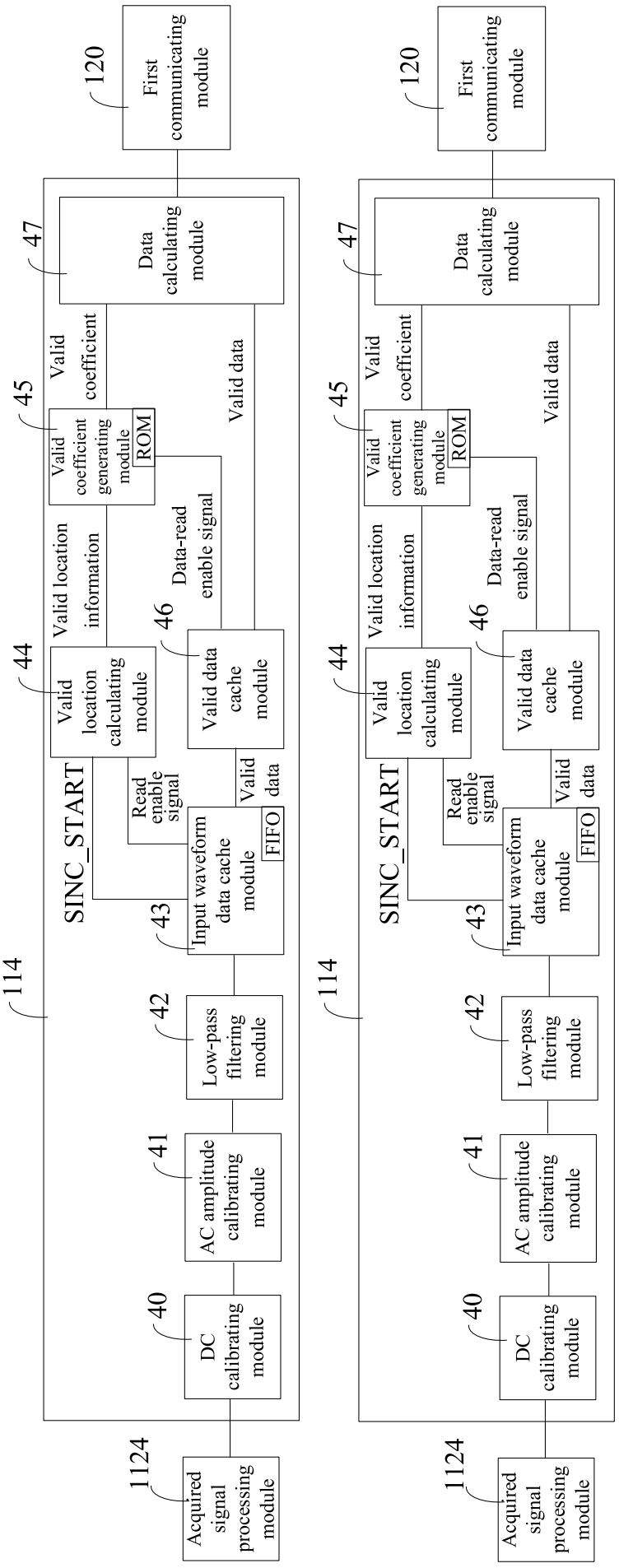

120
First communicating module
47
Data calculating module
45
Valid coefficient
Valid coefficient generating module
ROM
Valid location information
Data-read enable signal
Valid data
44
Valid location calculating module
46
Valid data cache module
SINC_START
Read enable signal
Valid data
43
Input waveform data cache module
FIFO
114
42
Low-pass filtering module
41
AC amplitude calibrating module
40
DC calibrating module
1124
Acquired signal processing module

FIG. 3

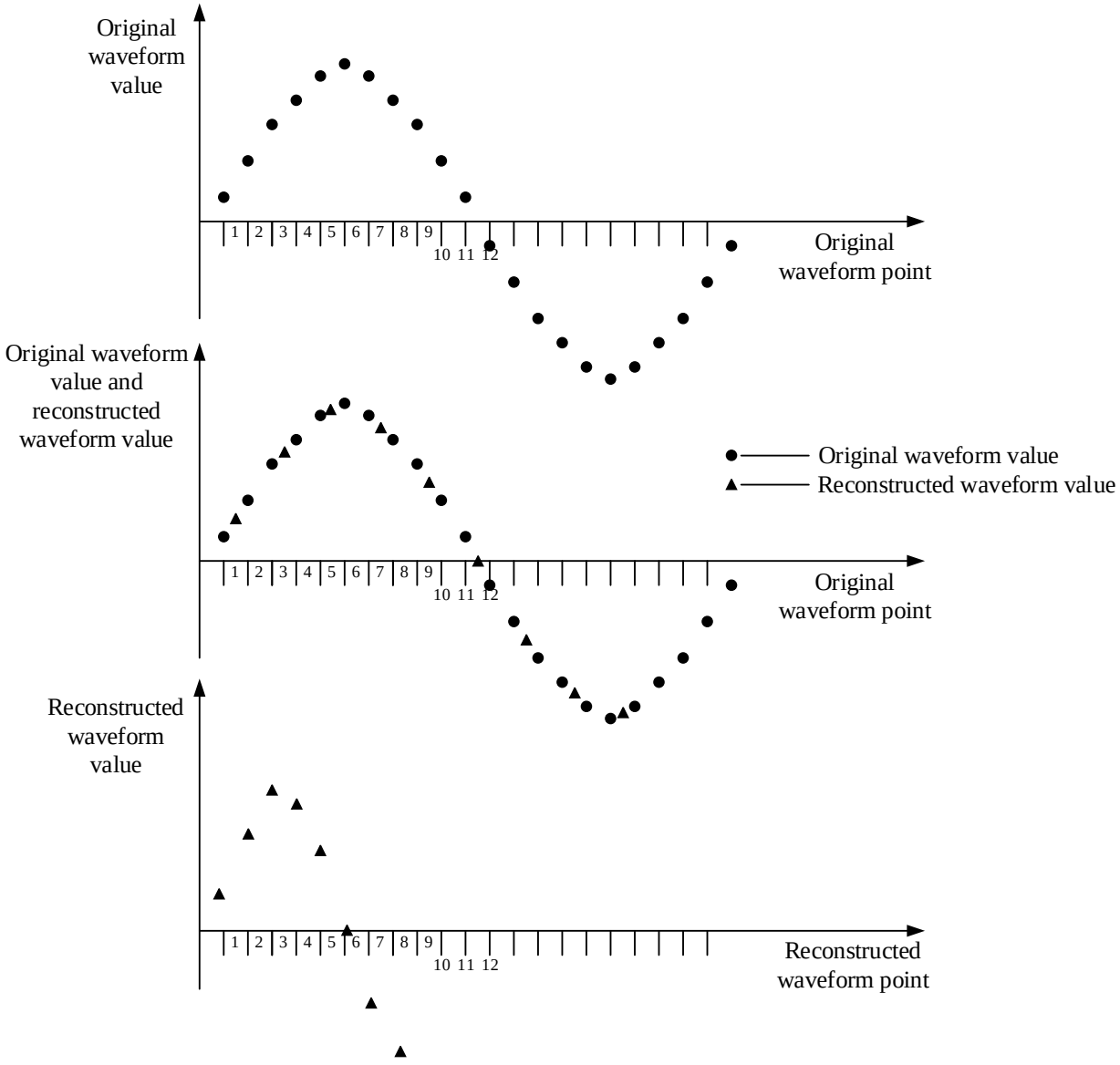

Original waveform value
1 2 3 4 5 6 7 8 9 10 11 12
Original waveform point
Original waveform value and reconstructed waveform value
Original waveform value
Reconstructed waveform value
1 2 3 4 5 6 7 8 9 10 11 12
Original waveform point
Reconstructed waveform value
1 2 3 4 5 6 7 8 9 10 11 12
Reconstructed waveform point

FIG. 4

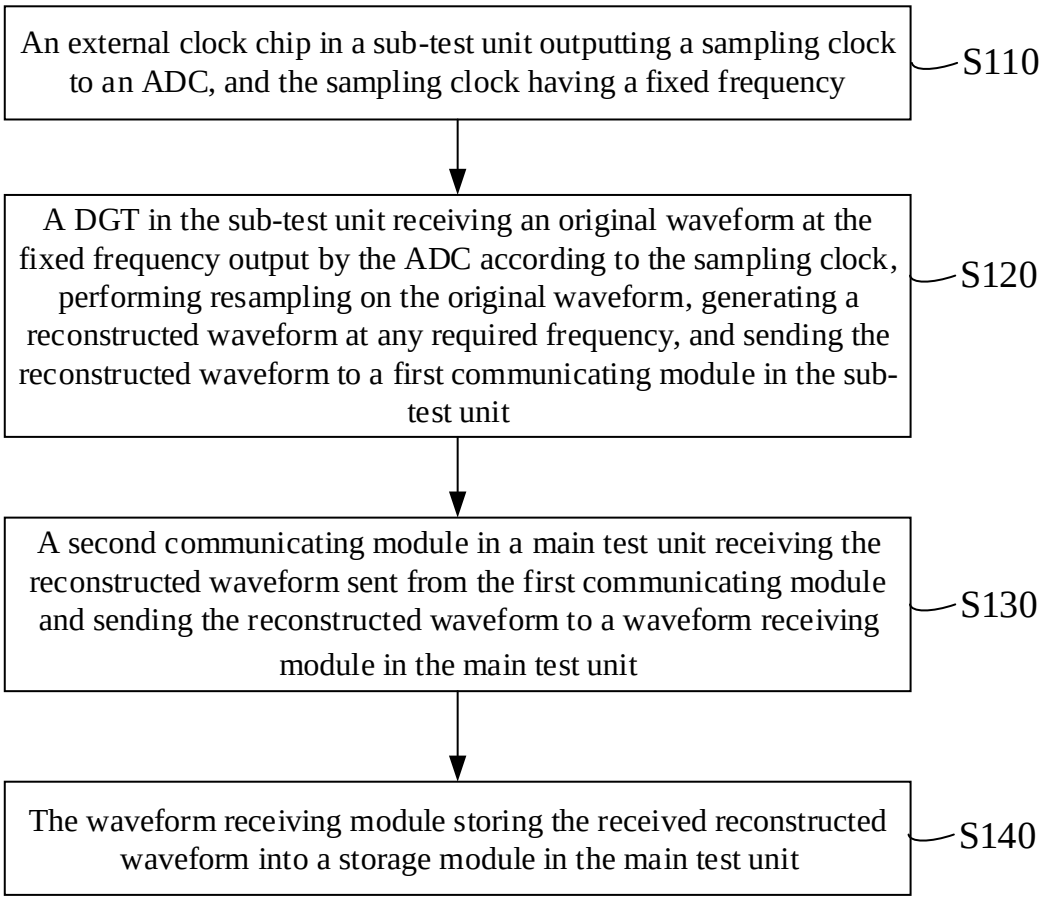

An external clock chip in a sub-test unit outputting a sampling clock to an ADC, and the sampling clock having a fixed frequency
S110
A DGT in the sub-test unit receiving an original waveform at the fixed frequency output by the ADC according to the sampling clock, performing resampling on the original waveform, generating a reconstructed waveform at any required frequency, and sending the reconstructed waveform to a first communicating module in the sub-test unit
S120
A second communicating module in a main test unit receiving the reconstructed waveform sent from the first communicating module and sending the reconstructed waveform to a waveform receiving module in the main test unit
S130
The waveform receiving module storing the received reconstructed waveform into a storage module in the main test unit
S140

FIG. 5