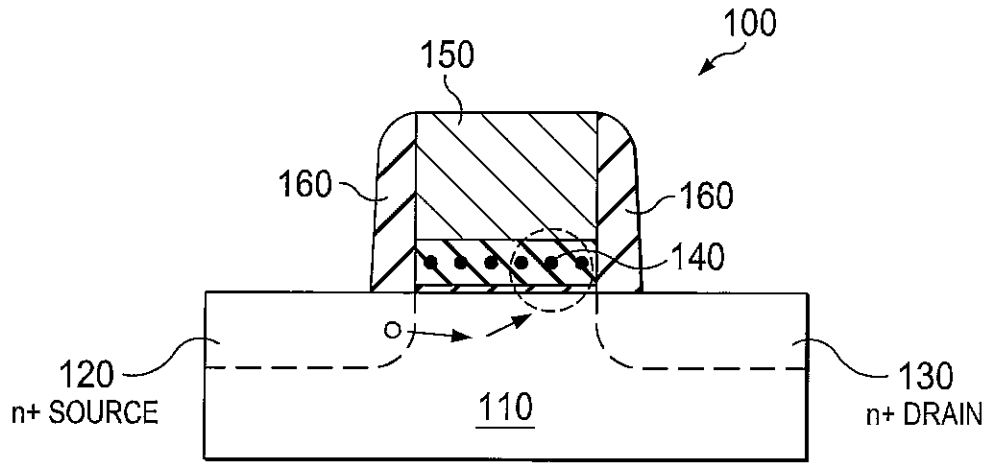


FIG. 1
(PRIOR ART)

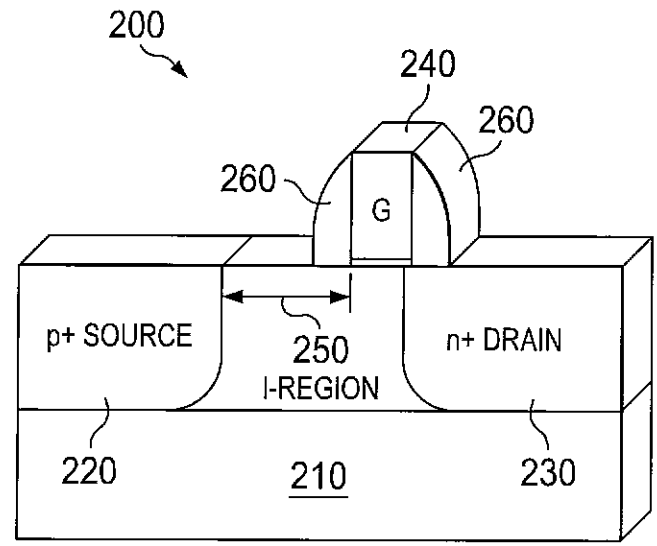


FIG. 2
(PRIOR ART)

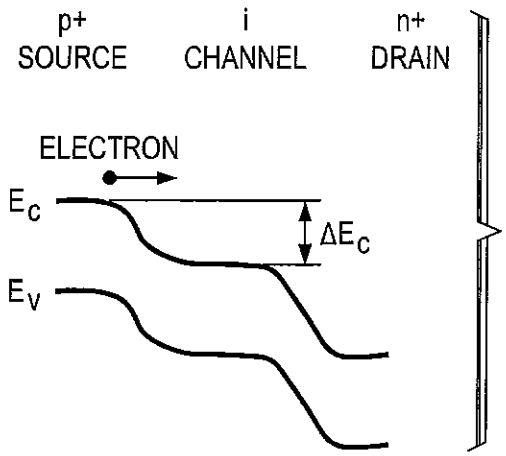


FIG. 3A
(PRIOR ART)

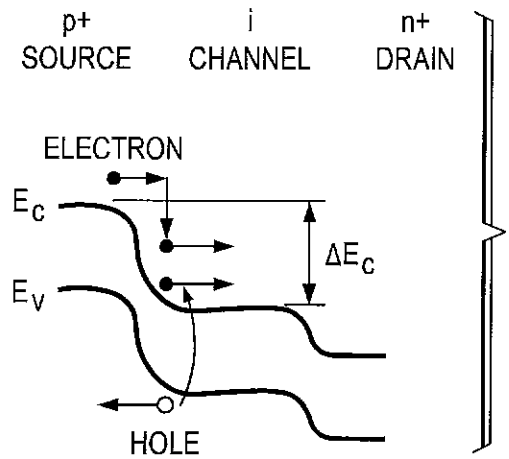


FIG. 3B
(PRIOR ART)

MODE	V_S	V_D	V_G
OFF	(--)	(+)	GND
ON	(--)	(+)	(+)

FIG. 4
(PRIOR ART)

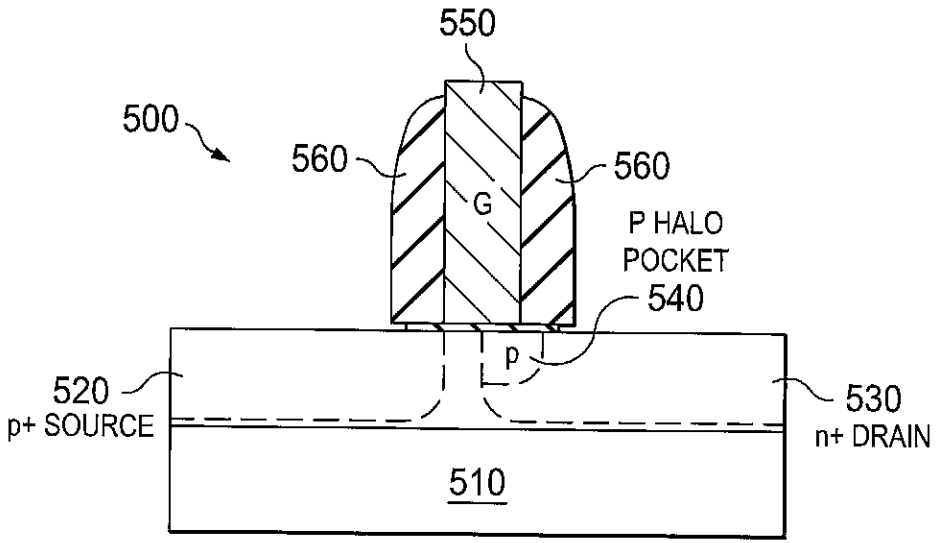


FIG. 5
(PRIOR ART)

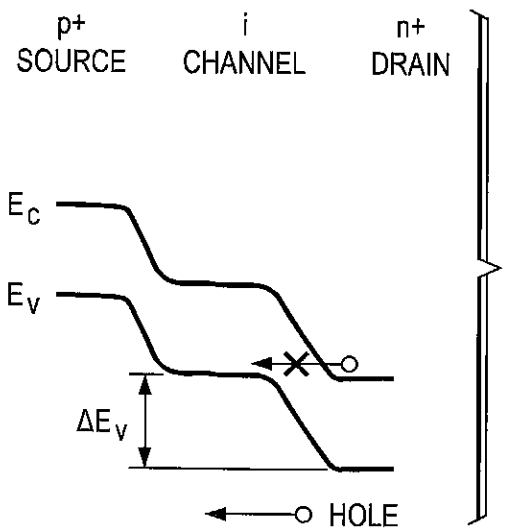


FIG. 6A
(PRIOR ART)

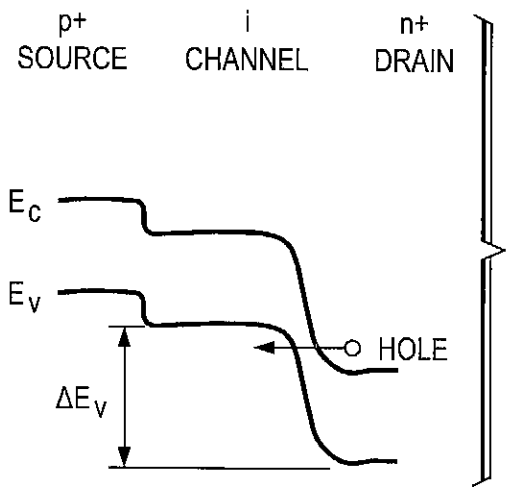


FIG. 6B
(PRIOR ART)

MODE	V_S	V_D	V_G
OFF	(-)	GND	GND
ON	(-)	GND	(-)

FIG. 7
(PRIOR ART)

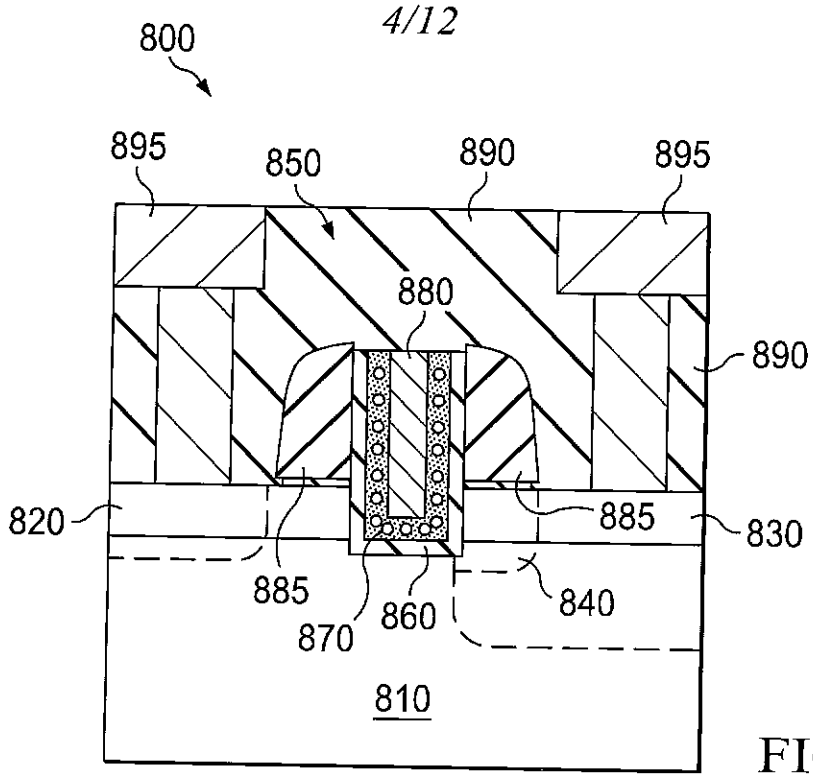


FIG. 8

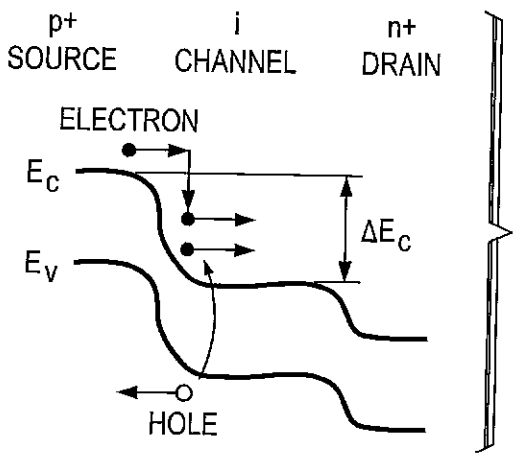


FIG. 9A

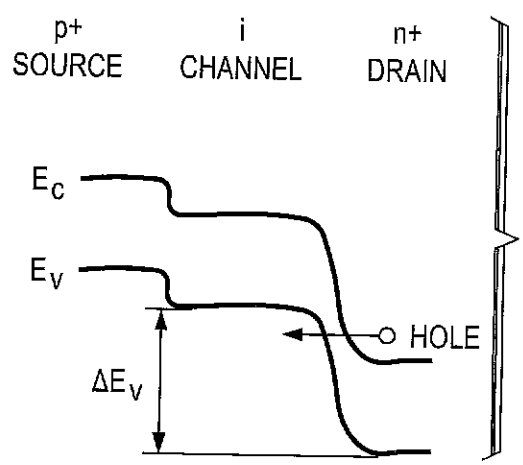


FIG. 9B

	MODE	V_S	V_D	V_G	V_{sub}
I-MOS →	PROGRAM	(--)	(+)	(+)	GND
	ERASE	GND	GND	(++)	GND
TFET →	READ	(-)	GND	(-)	GND

FIG. 10

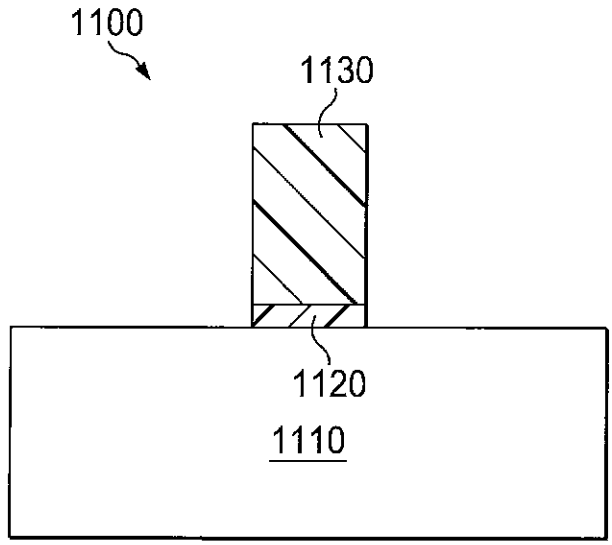


FIG. 11

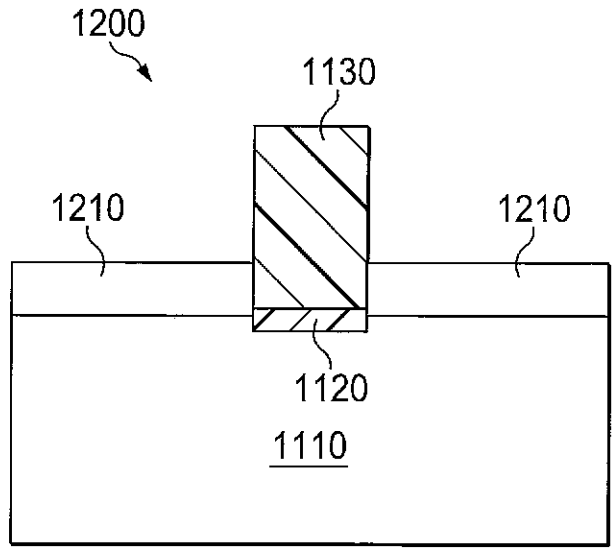


FIG. 12

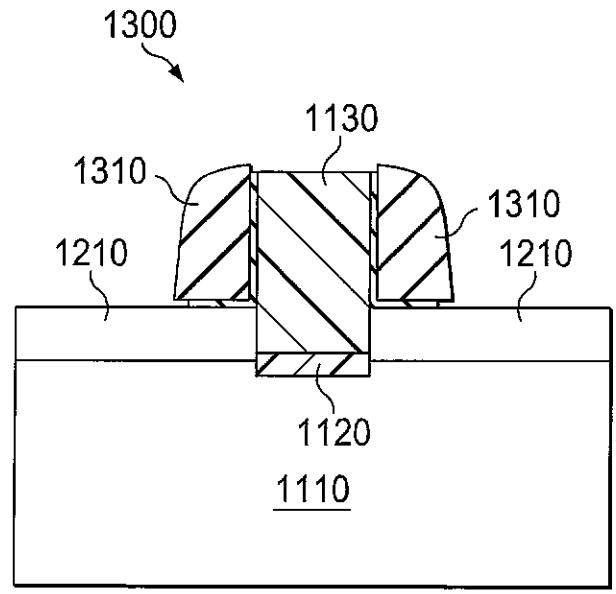


FIG. 13

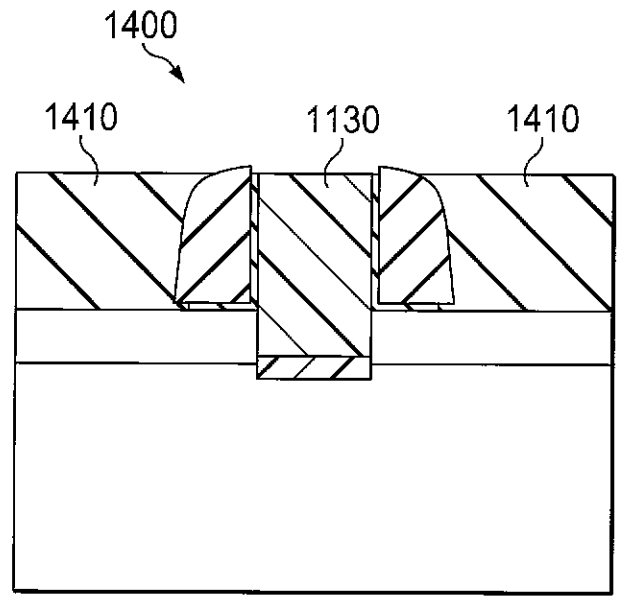


FIG. 14

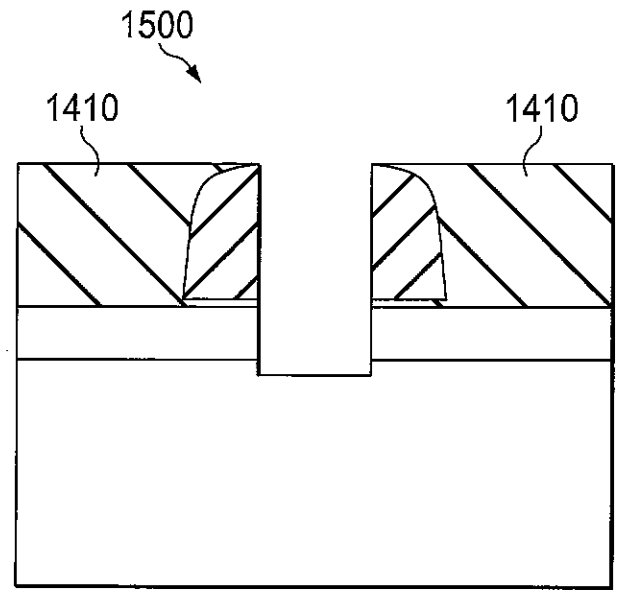


FIG. 15

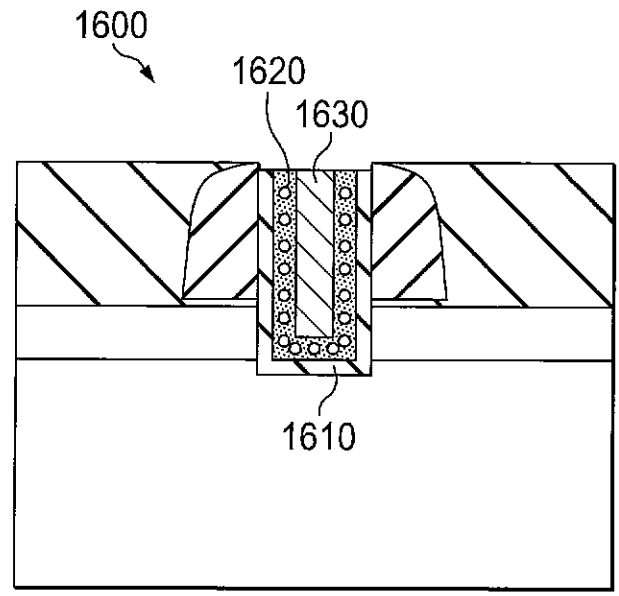


FIG. 16

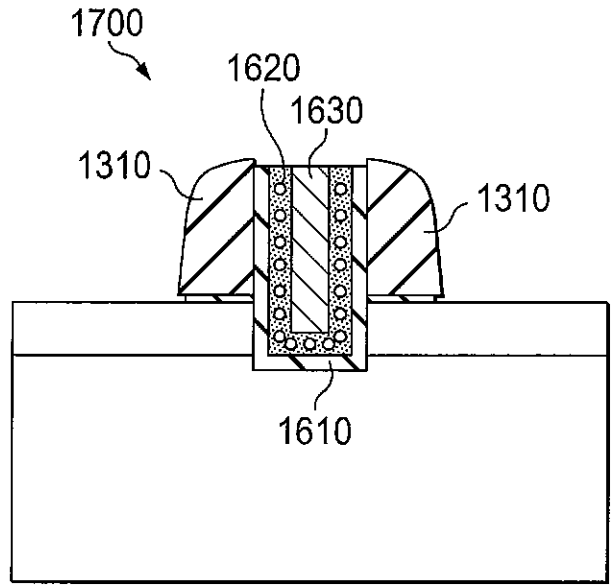


FIG. 17

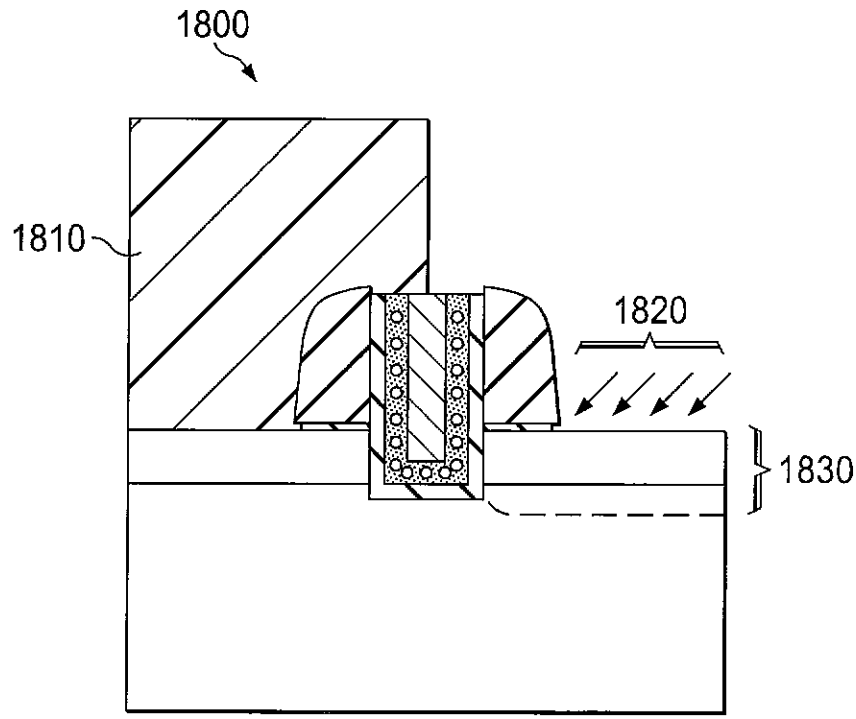


FIG. 18

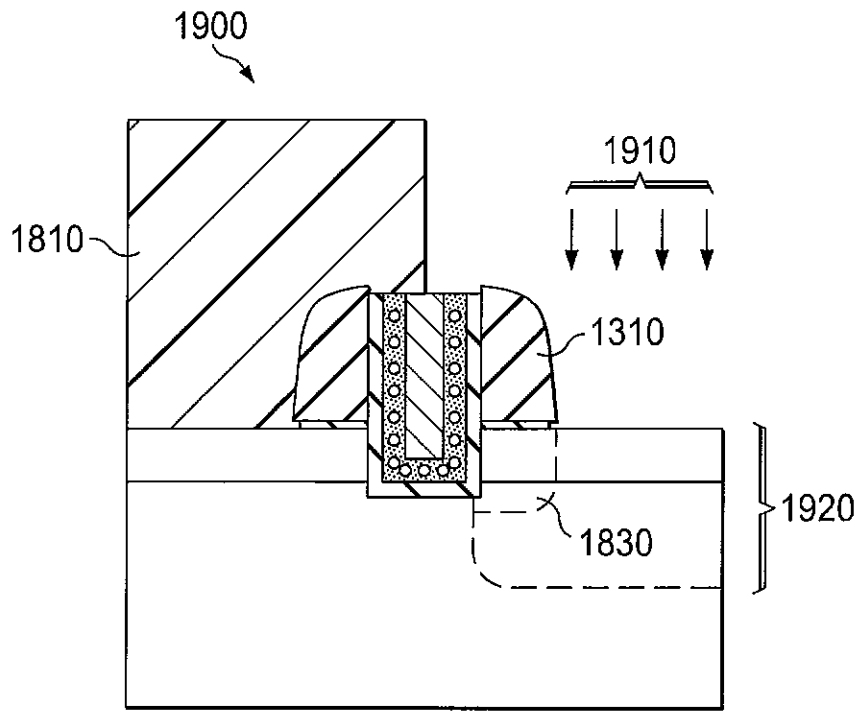


FIG. 19

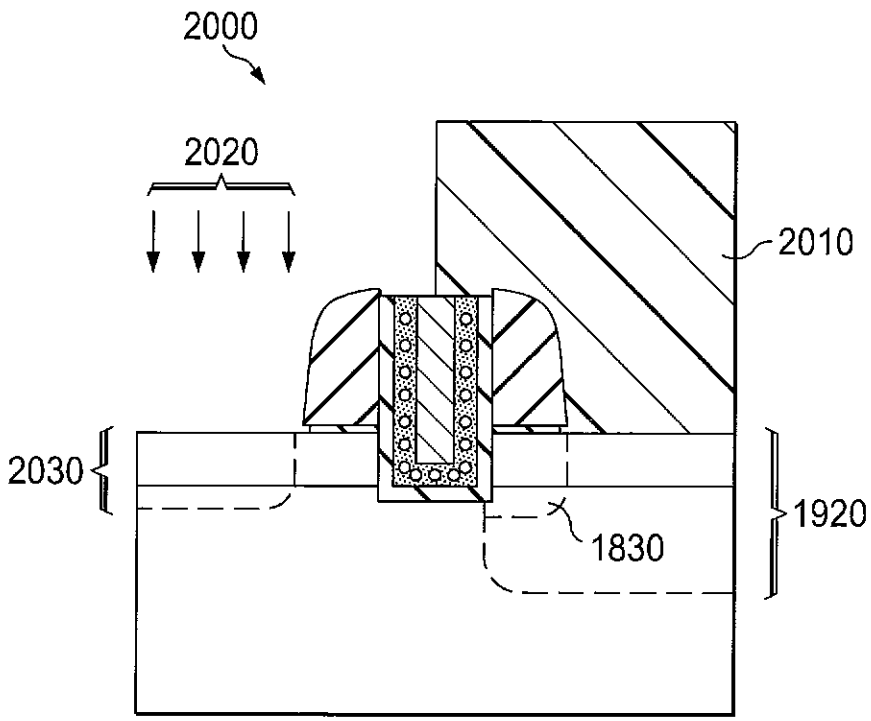


FIG. 20

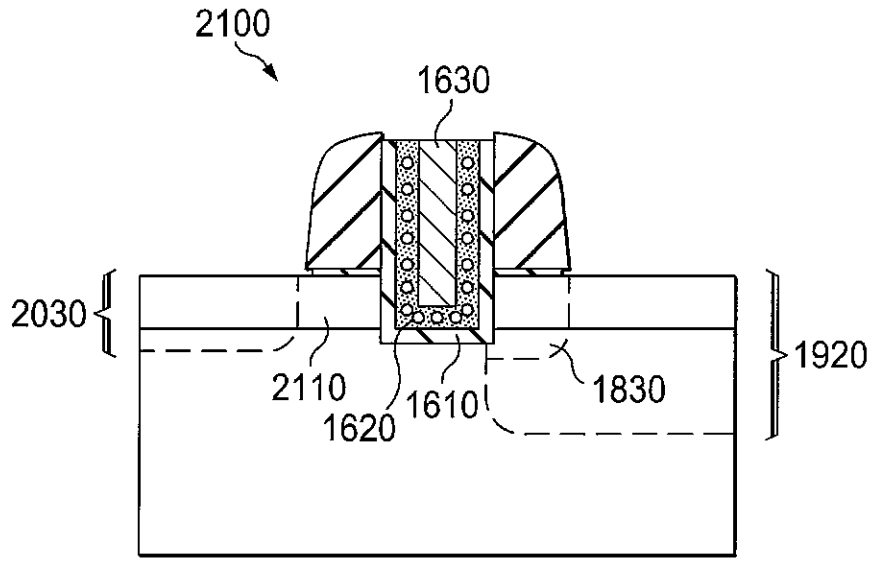

2100
1630
2030
1920
2110
1610
1830
1620

FIG. 21

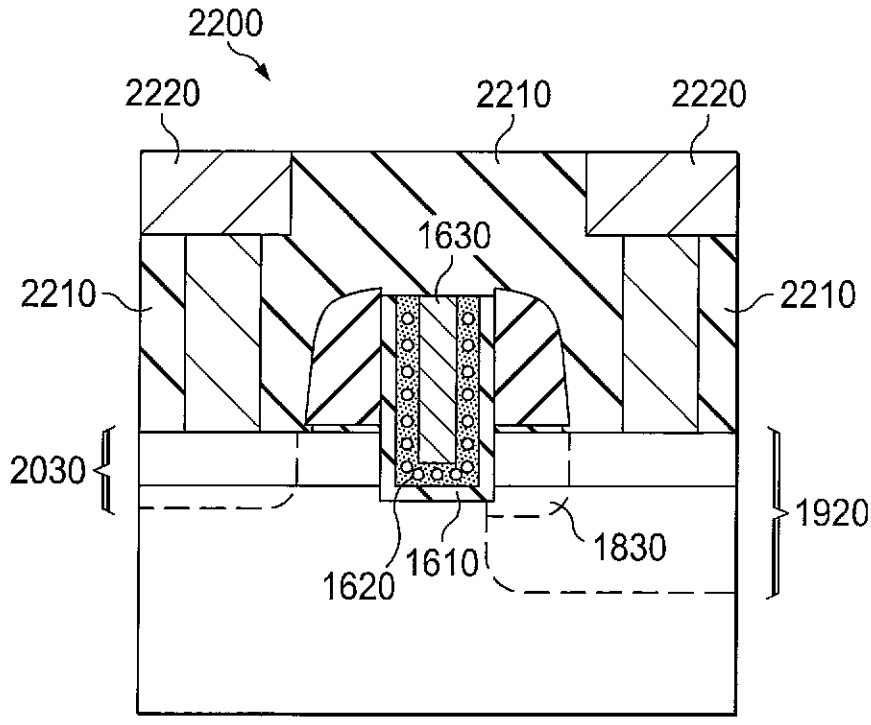

2200
2220
2210
2220
1630
2210
2210
2030
1920
1620
1610
1830

FIG. 22

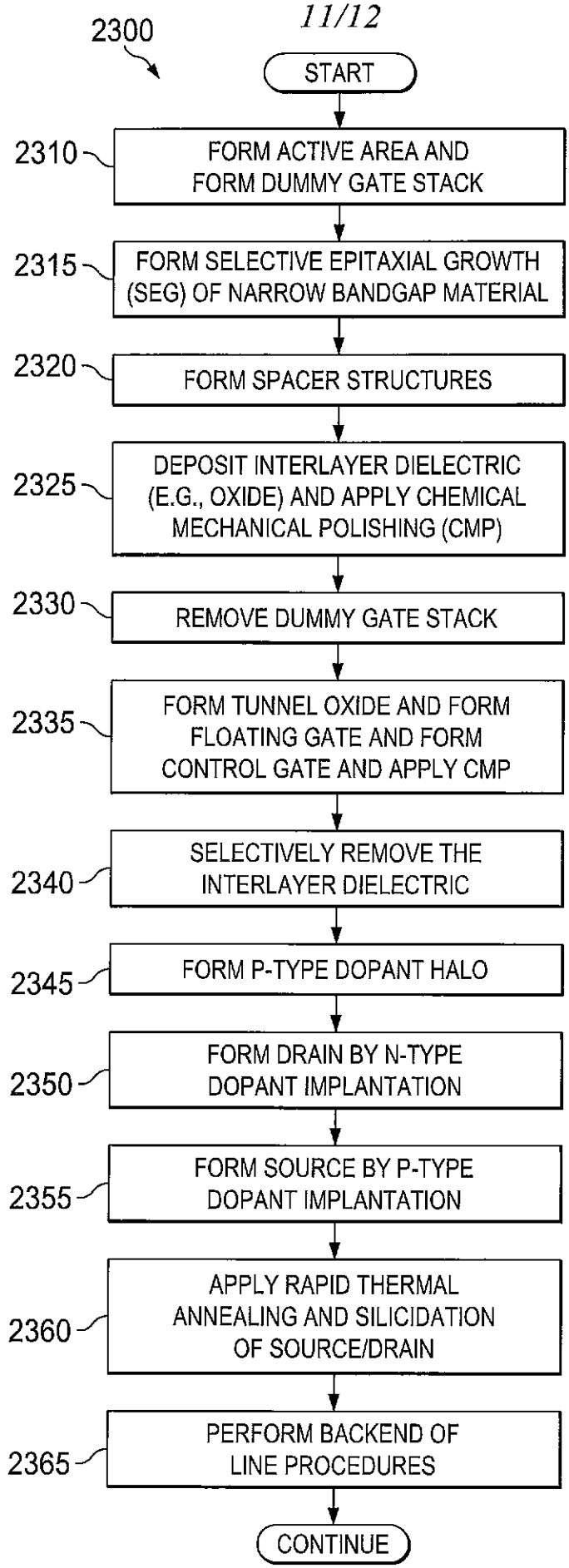

2300
START
2310
FORM ACTIVE AREA AND FORM DUMMY GATE STACK
2315
FORM SELECTIVE EPITAXIAL GROWTH (SEG) OF NARROW BANDGAP MATERIAL
2320
FORM SPACER STRUCTURES
2325
DEPOSIT INTERLAYER DIELECTRIC (E.G., OXIDE) AND APPLY CHEMICAL MECHANICAL POLISHING (CMP)
2330
REMOVE DUMMY GATE STACK
2335
FORM TUNNEL OXIDE AND FORM FLOATING GATE AND FORM CONTROL GATE AND APPLY CMP
2340
SELECTIVELY REMOVE THE INTERLAYER DIELECTRIC
2345
FORM P-TYPE DOPANT HALO
2350
FORM DRAIN BY N-TYPE DOPANT IMPLANTATION
2355
FORM SOURCE BY P-TYPE DOPANT IMPLANTATION
2360
APPLY RAPID THERMAL ANNEALING AND SILICIDATION OF SOURCE/DRAIN
2365
PERFORM BACKEND OF LINE PROCEDURES
CONTINUE

FIG. 23

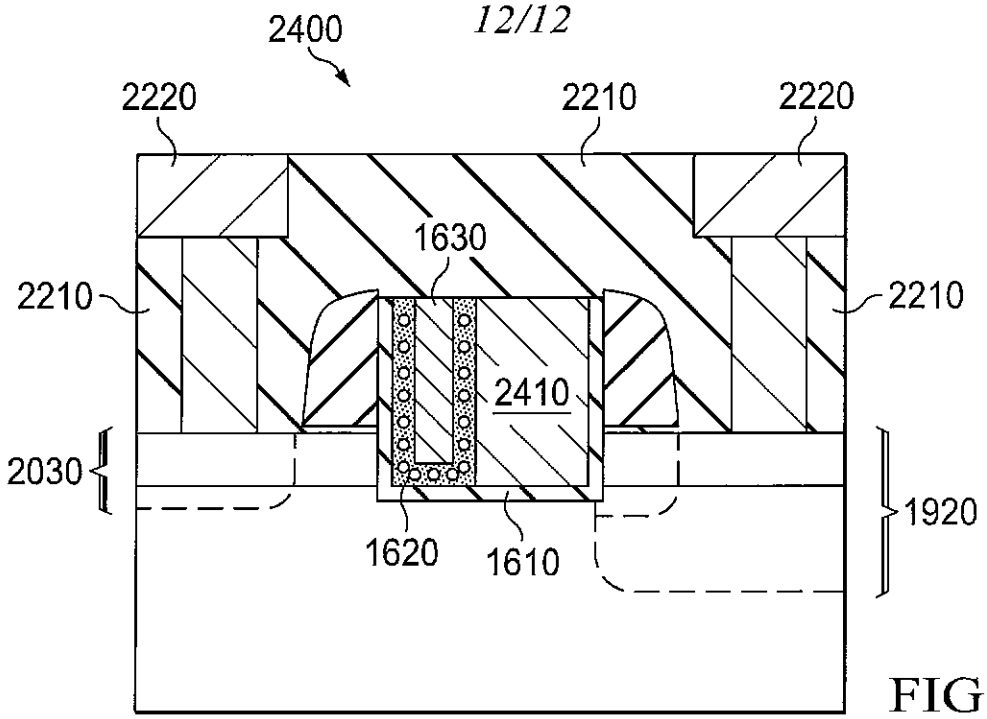

2400
2220
2210
2220
1630
2210
2210
2410
2030
1920
1620
1610

FIG. 24

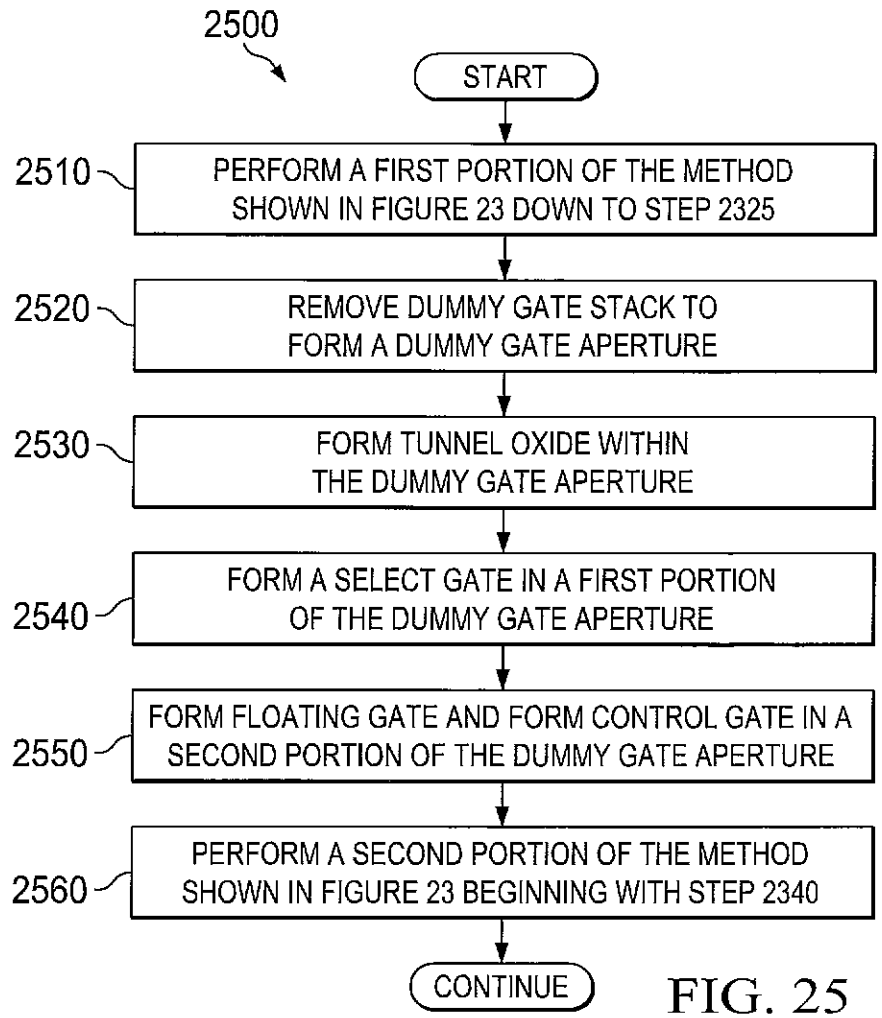

2500
START
2510
PERFORM A FIRST PORTION OF THE METHOD SHOWN IN FIGURE 23 DOWN TO STEP 2325
2520
REMOVE DUMMY GATE STACK TO FORM A DUMMY GATE APERTURE
2530
FORM TUNNEL OXIDE WITHIN THE DUMMY GATE APERTURE
2540
FORM A SELECT GATE IN A FIRST PORTION OF THE DUMMY GATE APERTURE
2550
FORM FLOATING GATE AND FORM CONTROL GATE IN A SECOND PORTION OF THE DUMMY GATE APERTURE
2560
PERFORM A SECOND PORTION OF THE METHOD SHOWN IN FIGURE 23 BEGINNING WITH STEP 2340
CONTINUE

FIG. 25