

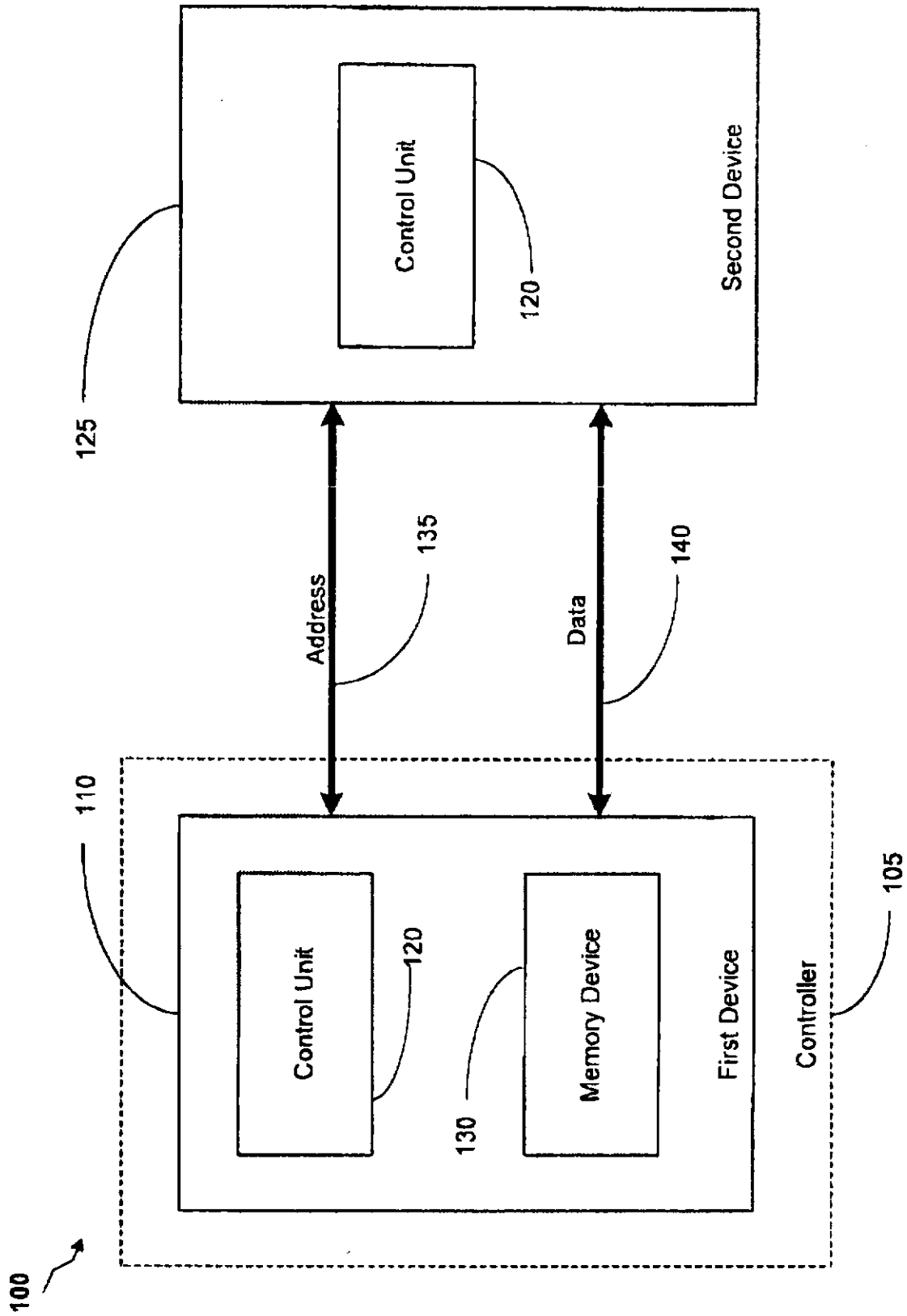
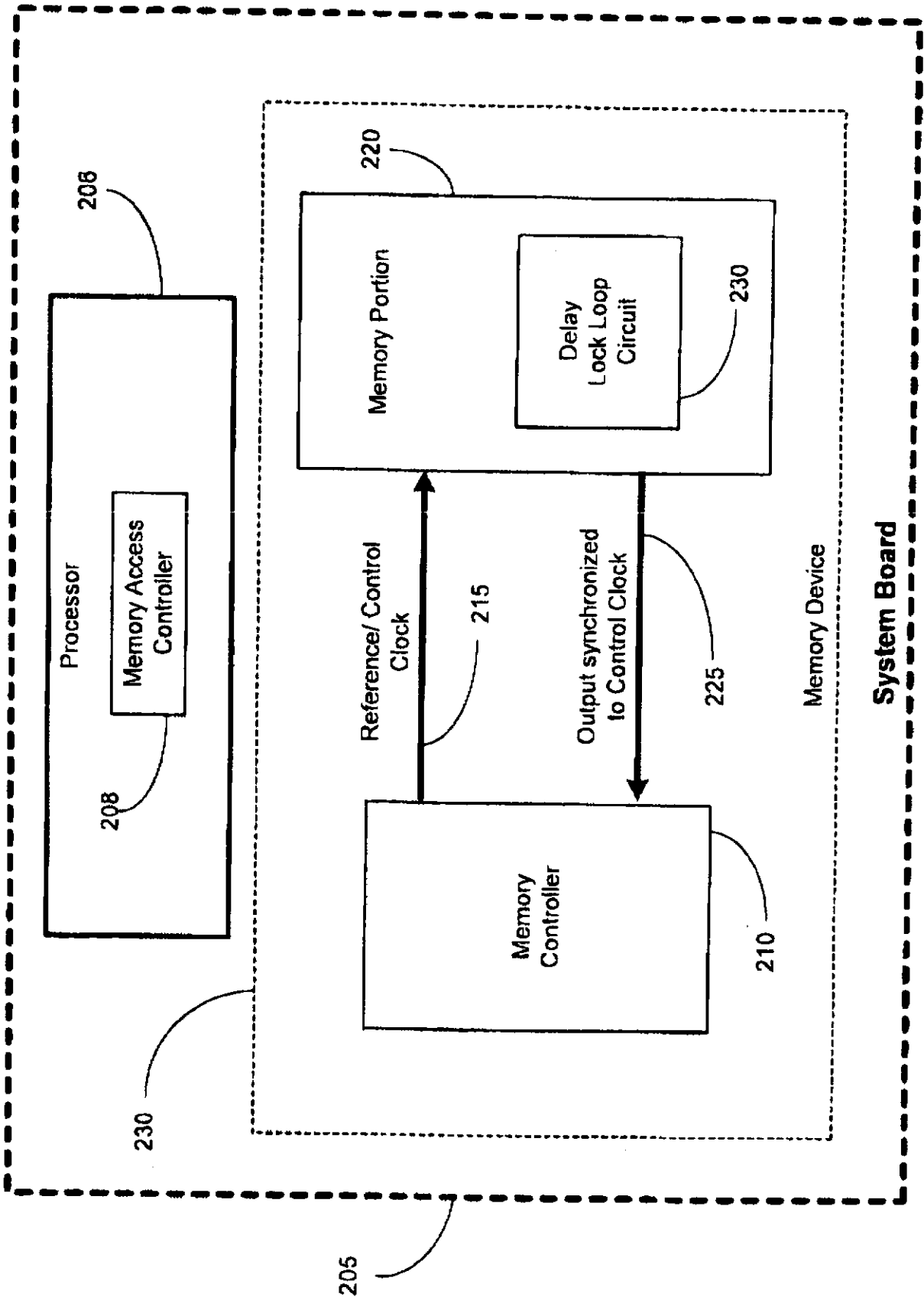


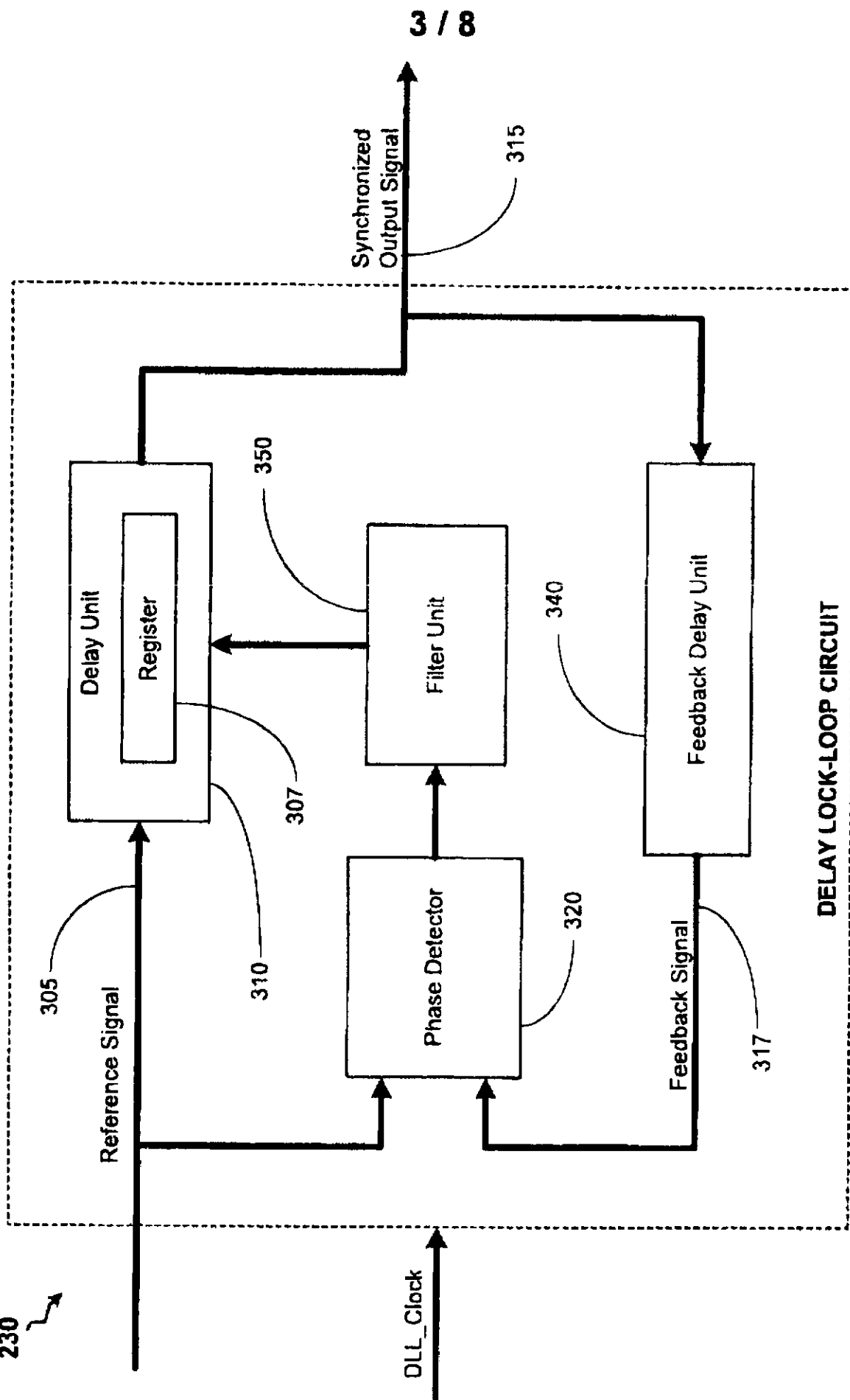
FIGURE 1



System Board

FIGURE 2

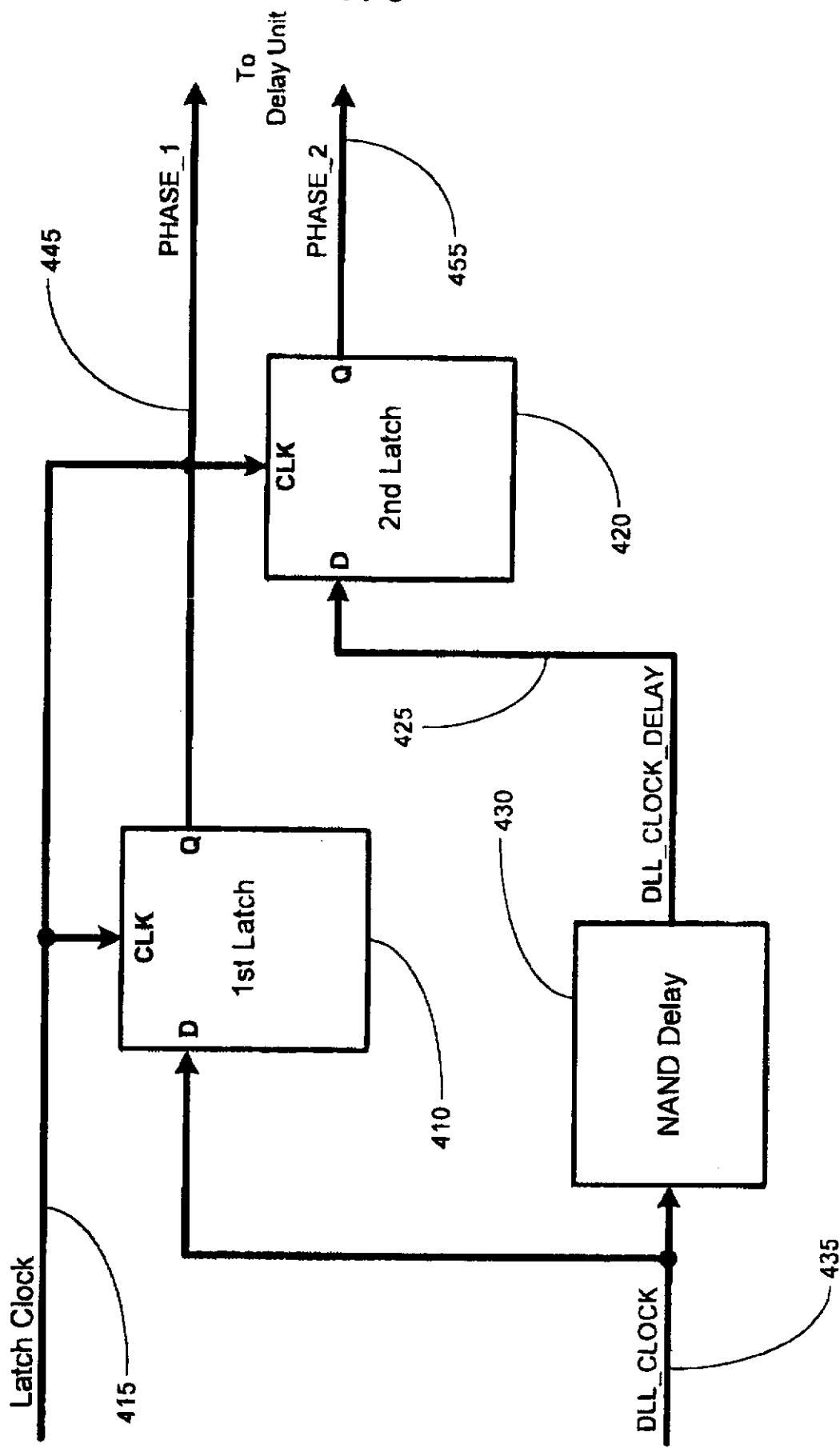
230



DELAY LOCK-LOOP CIRCUIT

FIGURE 3

400



4 / 8

FIGURE 4

PHASE_1	PHASE_2	Result
1 (logic high)	1 (logic high)	Shift-Left
1 (logic high)	0 (logic low)	Phase-Equal
0 (logic low)	0 (logic low)	Shift-Right
0 (logic low)	1 (logic high)	Shift-Right-180

FIGURE 5

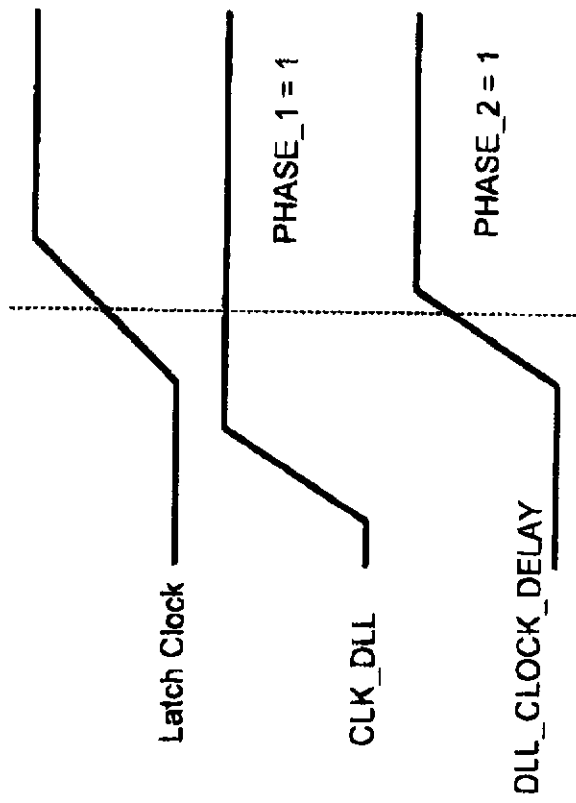


FIGURE 6A

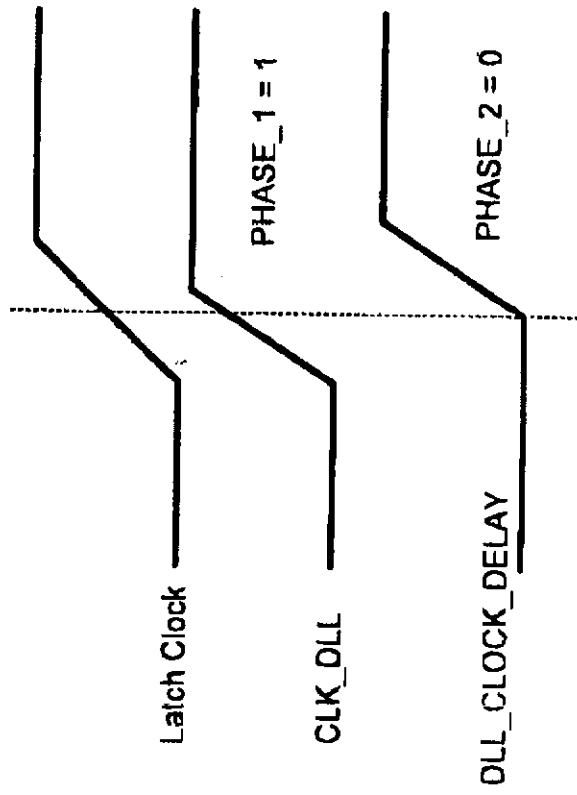


FIGURE 6B

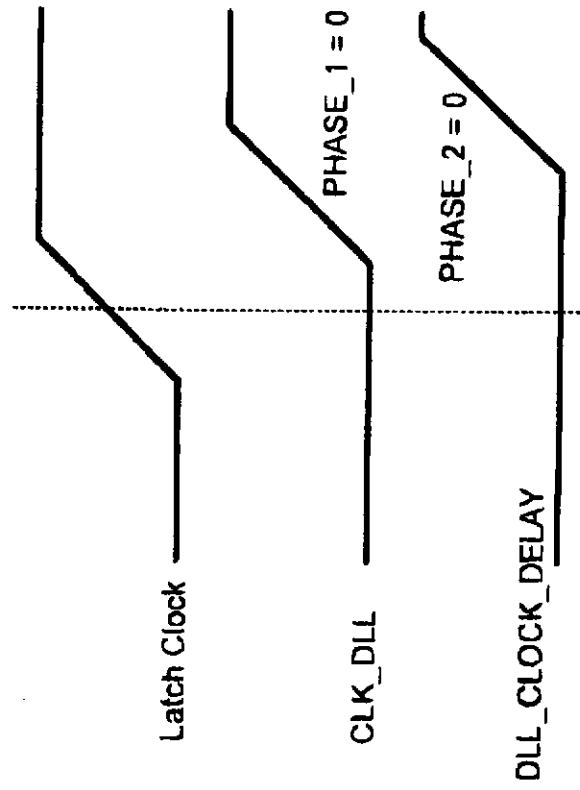


FIGURE 6C

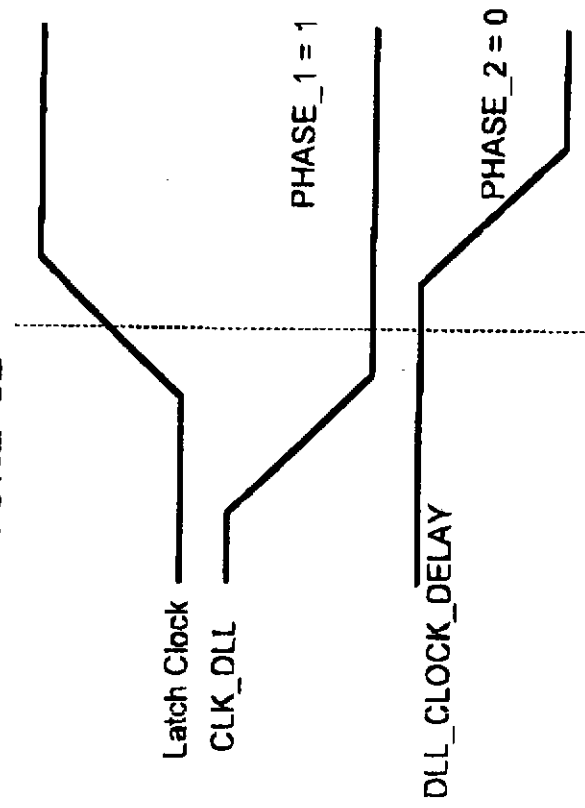


FIGURE 6D

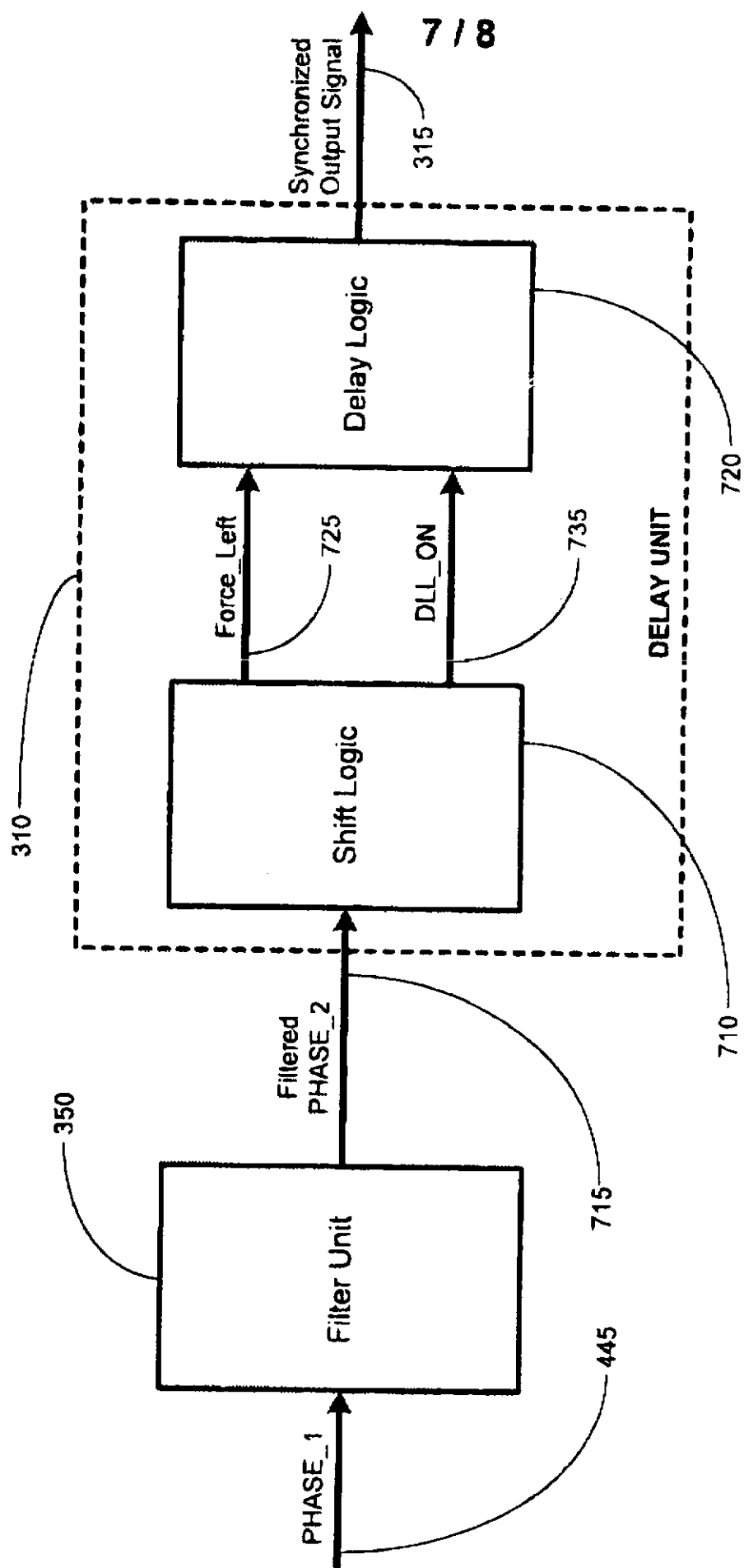


FIGURE 7

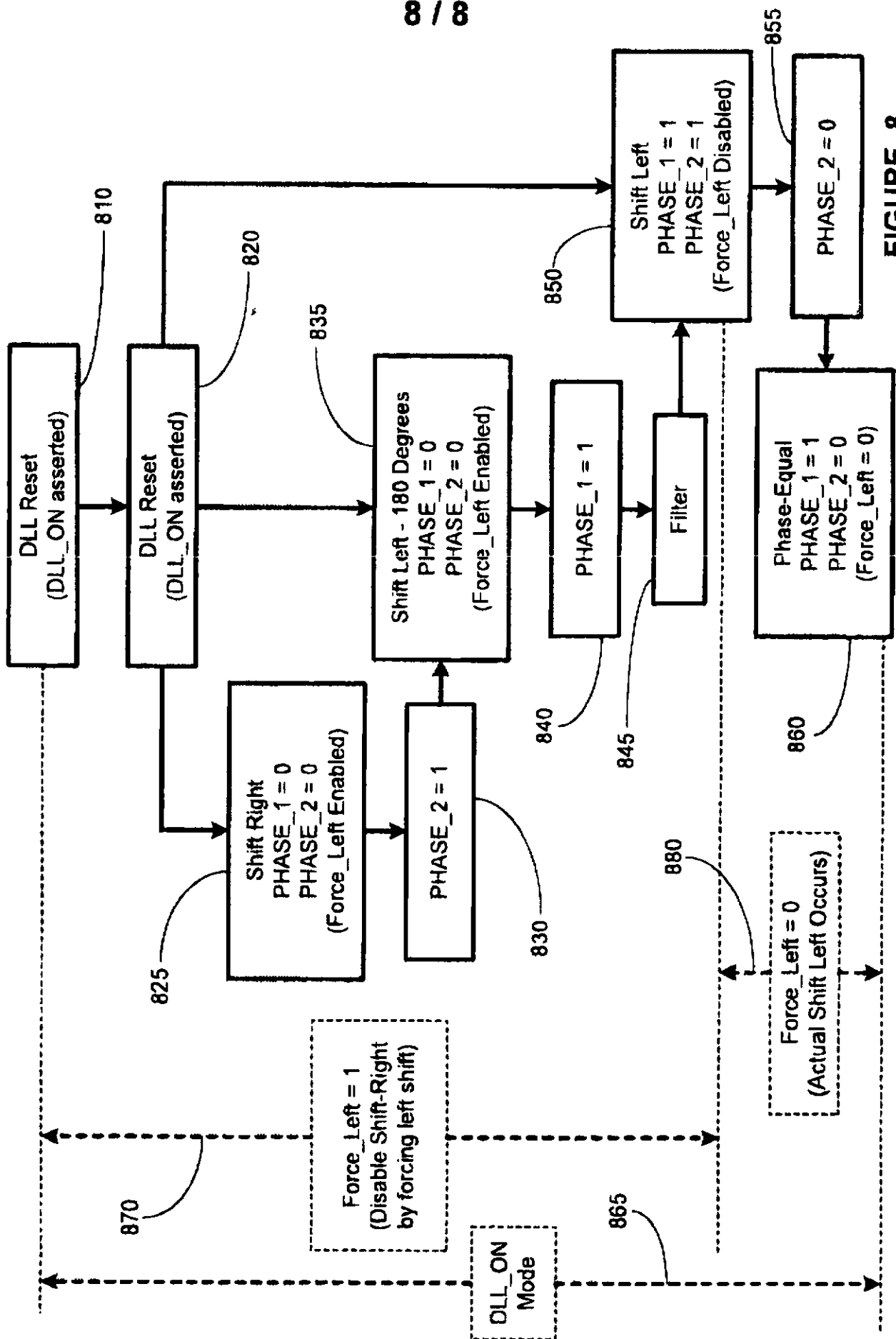


FIGURE 8