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— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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(54) Title: METHODS AND APPARATUS FOR POWER REDUCTION IN A TRANSCEIVER

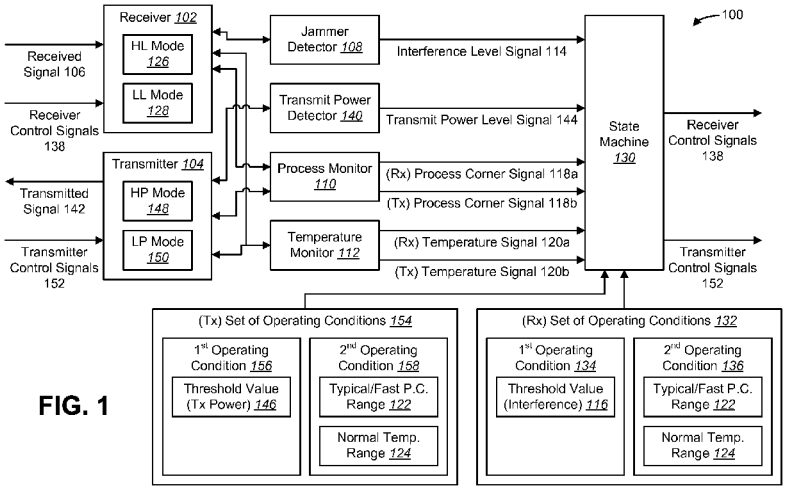


FIG. 1

(57) Abstract: An integrated circuit for achieving power reduction in a transceiver may include a jammer detector that determines an interference level corresponding to a received signal, and a transmit power detector that determines a required transmit power level for a transmitted signal. The integrated circuit may also include at least one of the following: a process monitor that determines process corners of components within the receiver and/or the transmitter, and a temperature monitor that determines a temperature of the receiver and/or the transmitter. The integrated circuit may also include a state machine. The state machine may transition the receiver from a high linearity mode to a low linearity mode if a set of operating conditions is satisfied. Similarly, the state machine may transition the transmitter from a high power mode to a low power mode if a set of operating conditions is satisfied.

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