ABSTRACT

METHOD TO FORM, AND STRUCTURE OF, A DUAL DAMASCENE INTERCONNECT DEVICE

A method of fabricating a dual damascene interconnect structure in a semiconductor device, comprises the following steps. A first level via photo sensitive dielectric layer is deposited and exposed over a semiconductor structure. A first level trench photo sensitive dielectric layer is deposited and exposed over the first via photo sensitive dielectric layer. The exposed first level via photo sensitive dielectric and trench photo sensitive dielectric layers are patterned and etched to form a first level dual damascene opening. The first level dual damascene opening comprises an integral first level via and metal line openings. A first level metal layer is deposited over the first level trench photo sensitive dielectric layer, filling the first level dual damascene opening. The first level metal layer is planarized to form at least one first level dual damascene interconnect having a first level horizontal metal line and a first level vertical via stack. The above steps are repeated n - 1 times to form n - 1 more dual damascene interconnects over the first level dual damascene interconnect where n is the number of interconnect levels desired. A passivation layer is deposited and patterned over the nth metal dual damascene interconnect layer to form openings in the passivation layer. The n number of via photo sensitive dielectric and trench photo sensitive dielectric layers are stripped and removed beneath the passivation layer openings and between the plurality of dual damascene structures wherein the portion of the via photo sensitive dielectric underneath the horizontal metal lines of the stripped trench photo sensitive dielectric layers remains.

(FIGURE 1A IS SUGGESTED FOR PUBLICATION)