

A CORING AND PEAKING CIRCUIT

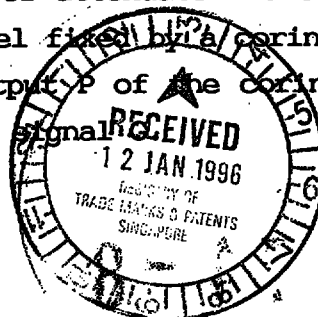
BACKGROUND OF THE INVENTIONField of the Invention

The present invention relates to a peaking/depeaking circuit for accentuating the outlines of the objects in a television picture, or on the contrary, for attenuating the outlines. The present invention more particularly relates to a coring circuit for disabling the peaking when the level of the signal to process is too low.

Discussion of the Related Art

Fig. 1 is a functional diagram of a conventional peaking/depeaking circuit. In this circuit, a signal Y, generally a television luminance signal is delayed a first time by a delay circuit 10 and delayed a second time by a delay circuit 11. A circuit 13 provides a signal D2 that is twice the output Y2 of delay circuit 10 minus signal Y and the output Y3 of delay circuit 11. As indicated in Fig. 1, if signal Y is a square pulse, signal D2 has, at the beginning of the square pulse, a negative pulse immediately followed by a positive pulse and, at the end of the square pulse, a positive pulse immediately followed by a negative pulse.

Signal D2 is applied to the input of an attenuator 15, which multiplies signal D2 by a coefficient 0.125, and to the input of an attenuator 16 which multiplies signal D2 by a coefficient 0.375. The output DP of attenuator 15 is provided to a subtractor 18 which subtracts signal DP to the output of attenuator 16 which is previously processed by a coring circuit 20 and by a multiplier 22. The coring circuit 20 transmits at its output P the output signal of attenuator 16 only if this signal exceeds a predetermined level fixed by a coring signal C. Multiplier 22 multiplies the output P of the coring circuit 20 by a coefficient fixed by a gain signal G.



An adder 24 receives the output of subtractor 18 and the delayed luminance signal Y2, and provides the processed signal Yp.

5 Signal DP, which is a depeaking signal, is permanently subtracted from signal Y2, whereas signal P, which is a peaking signal, is more or less amplified, depending upon the gain signal G provided to multiplier 22, and added to signal Y2. If the multiplication coefficient of multiplier 22 is lower than $1/3$, the subtraction of signal DP is dominant, and signal Yp has, as indicated in A, progressive step-form rising and falling edges. In contrast, if the multiplication coefficient of multiplier 22 exceeds $1/3$, the addition of signal P is dominant. Then, signal Yp has, as indicated in B, a rising edge preceded by a negative pulse and followed by an overshoot, and a falling edge preceded by an overshoot and followed by a negative pulse.

15 Up to now, the functions of the block diagram of Fig. 1 have been achieved with elements operating in voltage mode.

SUMMARY OF THE INVENTION

20 An object of the present invention is to provide a peaking/depeaking circuit, and more particularly a coring circuit, of a particularly simple structure.

 In embodiments of the present invention, some functions, shown in Fig. 1, are achieved in a particularly simple way, due to a specific structure formed with elements operating in current mode.

25 Embodiments of the invention more particularly relate to a coring circuit for an input signal in the form of a differential input current having two components in phase opposition. The coring circuit comprises a first pair of cascode transistors biased by a same reference voltage, for applying a first fraction of the components of the differential current to first two respective resistors; a second pair of cascode transistors biased by this reference voltage, for providing a second fraction of the components of this differential current to a differential current output of the circuit and to two respective branches of a differential stage receiving the voltages across the first re-

sistors; and two coring current sources which respectively connect two transistors forming the differential stage to a supply voltage, the two coring current sources being interconnected through a second resistor.

5 According to an embodiment of the invention, the ratio between the value of the second resistor and the value of the first resistors is twice the ratio of the first and second fractions.

10 A peaking/depeaking circuit according to one embodiment of the invention comprises the above-mentioned coring circuit; a third pair of cascode transistors biased by the reference voltage, for injecting a third fraction of the components of the differential current respectively into an input branch and an output branch of a current mirror; and a differential multiplier
15 receiving a differential multiplication voltage and the differential current output of the coring circuit, two output branches of the multiplier being respectively connected to the branches of the current mirror.

20 According to an embodiment of the invention, the differential input current of the coring circuit is obtained from an input voltage, this input voltage delayed once and this input voltage delayed twice. A differential stage receives the voltage of the output branch of the current mirror and the input voltage delayed once, the two branches of this differential stage being
25 respectively connected to the input and output branches of the current mirror. The voltage of the output branch of the current mirror constitutes the output signal of the peaking/depeaking circuit.

30 According to an embodiment of the invention, the differential input current of the coring circuit is provided by two parallel connected output branches of two differential stages, one of which receives the input voltage and the input voltage delayed once, the other stage receiving the input voltage delayed once and the input voltage delayed twice.

35 The foregoing and other objects, features, aspects and advantages of the invention will become apparent from the follow-

ing detailed description of illustrative embodiments of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

5 Fig. 1, above described, represents a conventional functional diagram of a peaking/depeaking circuit;

 Fig. 2 represents an embodiment of a coring circuit according to one embodiment of the present invention;

10 Fig. 3 represents a transfer diagram illustrating the operation of the circuit of Fig. 2;

 Fig. 4 represents circuitry to add to the coring circuit of Fig. 2 to realize a peaking/depeaking circuit; and

15 Fig. 5 represents an embodiment of a circuit for providing a current signal required by the circuits of embodiments of the present invention.

DETAILED DESCRIPTION

20 According to the invention, the signal D2 of Fig. 1 is in the form of a differential current having components D2+ and D2-. From this signal D2-/D2+, all the other signals are processed as differential currents until the output voltage Yp is provided.

25 Fig. 2 represents an embodiment of a coring circuit according to the invention. It is in particular the specific structure of the coring circuit according to the invention that provides a significant simplification of the peaking/depeaking circuit.

30 A pair of PNP cascode transistors Q1 and Q2 transmits a fraction of the differential current D2-/D2+ to two resistors 30 and 31. The bases of transistors Q1 and Q2 are biased by a constant reference voltage Vr. Transistors Q1 and Q2 receive respectively on their emitters the components D2- and D2+, and their collectors are connected to ground GND through resistors 30 and 31, respectively.

35 A second pair of PNP cascode transistors Q3 and Q4 transmits a fraction of the differential current D2-/D2+ to the respective branches of a differential stage formed by two NPN

transistors Q5 and Q6. Transistors Q3 and Q4 are connected in parallel by their emitters and their bases to transistors Q1 and Q2. The collectors of transistors Q5 and Q6 are respectively connected to the collectors of transistors Q3 and Q4 and respectively provide the components P^- and P^+ of a differential current which corresponds to the peaking signal P of Fig. 1. The bases of transistors Q5 and Q6 are connected to the collectors of transistors Q1 and Q2, respectively. The differential stage Q5, Q6 is a low gain stage; for this purpose, the emitters of transistors Q5 and Q6 are connected to ground through respective current sources 33 and 34, and connected to each other through a resistor 36. The current I_c of sources 33 and 34, i.e., a coring current which can be adjusted by a signal C , determines the width of the coring range of signal $D2^+/D2^-$, i.e., the amplitude of signal $D2^+/D2^-$ below which the output P^+/P^- of the circuit is zero.

A pair of PNP cascode transistors Q7 and Q8 transmits a fraction of the differential current $D2^-/D2^+$ as a differential current DP^-/DP^+ which corresponds to the depeaking signal DP of Fig. 1. Transistors Q7 and Q8 are connected in parallel by their bases and their emitters to transistors Q1 and Q2, respectively, and the collectors of transistors Q7 and Q8 provide the components DP^- and DP^+ . The cascode transistors Q1-Q4 and Q7, Q8 distribute the currents of components $D2^-$ and $D2^+$ as a function of the sizes of these transistors. Thus, the attenuation coefficients of attenuators 15 and 16 of Fig. 1 are obtained by selecting transistors Q3 and Q4 three times larger than transistors Q7, Q8, and transistors Q1 and Q2 four times larger than transistors Q7 and Q8. The relative sizes of these transistors are indicated in brackets in Fig. 2.

Thus, if components $D2^-$ and $D2^+$ have values $8(I-i)$ and $8(I+i)$, respectively, (where I is a constant quiescent current, and i is a variable current representative of signal $D2$), currents $4(I-i)$, $4(I+i)$, $3(I-i)$, $3(I+i)$, $I-i$, and $I+i$ circulate respectively in the collectors of transistors Q1-Q4 and Q7 and Q8. The collector currents of transistors Q1 and Q2 generate volt-

ages across resistors 30 and 31. The difference between voltages across resistors 30 and 31 is applied to the terminals of resistor 36. In the example of Fig. 2, resistors 30 and 31 have a value $3R$ and resistor 36 has a value $8R$. With these values, there is a current $3i$ in resistor 36, provided that this current $3i$ is lower than the current I_c of source 33 or 34. Then, the collector current of transistor Q5 has a value of $I_c - 3i$, and the collector current of transistor Q6 has a value of $I_c + 3i$. As a result, the components P_- and P_+ each have a value $3I - I_c$, which is independent of i ; the differential current P_+/P_- is zero for any value of i . This operation mode is obtained within a "coring" range.

Generally, the differential current P_+/P_- is canceled in the coring range by selecting the ratio between the value of resistor 36 and the value of resistors 30 and 31 equal to twice the size ratio between transistors Q1 (or Q2) and Q3 (or Q4). Otherwise, the differential current P_+/P_- will vary with a slight positive or negative slope.

Now, if current $3i$ in resistor 36 tends to exceed value I_c (goes outside the coring range), the excess current cannot be absorbed by source 33. Thus, in the example of Fig. 2, the collector current of transistor Q5 is zero and the collector current of transistor Q6 establishes at $2I_c$, independently of the value of current i , provided that it is higher than $I_c/3$. Then, the component P_- establishes at $3(I - i)$ and the component P_+ establishes at $3(I + i) - 2I_c$.

Fig. 3 illustrates the variation of the differential current P_+/P_- as a function of current i . Between values $-I_c/3$ and $I_c/3$ of current i (within the coring range), the current P_+/P_- is zero. Beyond value $I_c/3$, current P_+/P_- varies according to a straight which intersects the vertical axis at a point $-2I_c$. Below value $-I_c/3$, current P_+/P_- varies according to a straight which intersects the vertical axis at a point $2I_c$.

If the ratio between the value of resistor 36 and the value of resistors 30 and 31 differs from twice the size ratio between transistors Q1 and Q3 (or Q2 and Q4), the slope of sig-

nal $P+/P-$ within the coring range becomes positive or negative instead of being zero, which is undesirable. Such a slope variation cannot occur in a circuit according to the invention when the temperature varies or when the fabrication technology changes, because the above-mentioned ratios are determined by elements of same nature (resistors or transistors) which have identical variation characteristics as a function of the temperature or the fabrication technology. In addition, these ratios are easy to achieve accurately in integrated technology.

Fig. 4 represents an embodiment using the circuit of Fig. 2 for realizing a peaking/depeaking circuit according to the invention. The components $DP+$ and $DP-$ drawn from the collectors of transistors Q7 and Q8 are provided to an input branch and an output branch, respectively, of a current mirror including PNP transistors Q9 and Q10. The emitters of transistors Q9 and Q10 are connected to a high supply voltage V_{cc} . The collectors of these transistors, which form the input and output branches of the current mirror, are connected to ground GND through respective current sources 40 and 41 of same value. The bases of transistors Q9 and Q10 are connected to each other and are connected to the collector of transistor Q9.

The components $P-$ and $P+$ are injected in two biasing branches of two respective differential stages forming a multiplier. One stage comprises two NPN transistors Q11 and Q12, and the other stage comprises two NPN transistors Q13 and Q14. The emitters of transistors Q11 and Q12, receiving the component $P-$, are connected to ground GND through a current source 43. The emitters of transistors Q13 and Q14, receiving the component $P+$, are connected to ground GND through a current source 44 of same value as source 43. The collectors of transistors Q12 and Q13 are connected to voltage V_{cc} and their bases receive a component $G+$ of a differential control voltage $G+/G-$ which determines the multiplication coefficient of the multiplier. Transistors Q11 and Q14 receive at their bases the component $G-$ and their collectors are connected to the input branch and to the output branch of the current mirror Q9, Q10, respectively.

With this configuration, the difference between the differential output current of the multiplier (provided by the collectors of transistors Q11 and Q14) and of the differential current $DP+/DP-$ is obtained on the input and output branches of mirror Q9, Q10. The functions of multiplier 22 and of subtractor 18 of Fig. 1 are thus achieved.

In addition, the output voltage Y_p of the peaking/ depeaking circuit is provided by a follower transistor Q15 which receives at its base the voltage of the output branch of the current mirror Q9, Q10 (i.e., the collector voltage of transistor Q10). Transistor Q15 has its collector connected to voltage V_{cc} and its emitter, which provides voltage Y_p , connected to ground through a current source 46. Voltage Y_p and a voltage Y_2 , which corresponds to the delayed signal Y_2 of Fig. 1, are applied to the bases of transistors Q16 and Q17, which form a low gain differential stage. The emitters of transistors Q16 and Q17 are connected to ground by respective current sources 48 and 49 of same value and that are connected to each other through a resistor 50. The collectors of transistors Q16 and Q17 are connected to the input branch and output branch of the current-mirror Q9, Q10. This differential stage provides the function of the adder 24 of Fig. 1.

To ensure that transistors Q7 and Q8 (Fig. 2) are constantly conductive, NPN cascode transistors (not shown) biased by voltage V_r can be connected between transistors Q9 and Q10 and terminals $DP+$ and $DP-$. This also isolates multiplier Q11-Q14 from transistors Q7 and Q8, and thus allows to bias the multiplier with a different voltage.

Fig. 5 represents an embodiment of a circuit providing the differential current $D2+/D2-$ from voltages Y , Y_2 and Y_3 of Fig. 1. The output branches of two low gain differential stages are connected in parallel and provide components $D2+$ and $D2-$, respectively. One of the stages comprises PNP transistors Q18 and Q19 whose emitters are connected to voltage V_{cc} through respective current sources 52 and 53 of same value, and are connected to each other through a resistor 54. The other differential

stage comprises PNP transistors Q20 and Q21 whose emitters are connected to voltage Vcc through respective current sources 56 and 57 of same value as sources 52 and 53, and are connected to each other through a resistor 58 of same value as resistor 54.
5 The collectors of transistors Q18 and Q21 provide the component D2+ and the collectors of transistors Q19 and Q20 provide the component D2-. The bases of transistors Q18 and Q21 receive voltages Y and Y3, respectively, and the bases of transistors Q19 and Q20 both receive voltage Y2.

10 A complete peaking/depeaking circuit according to the present invention, achieved from elements operating in current mode, comprises approximately 55 transistors and 41 resistors, whereas conventional circuits using elements operating in voltage mode and furthermore not comprising the depeaking function,
15 include approximately 75 transistors and 48 resistors.

Having thus described at least one illustrative embodiment of the invention, various alterations, modifications and improvements will readily occur to those skilled in the art. Such alterations, modifications, and improvements are intended to be
20 within the spirit and scope of the invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is:



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CLAIMS

1. A coring circuit for an input signal (D2) in the form of a differential input current having two components in phase opposition (D2+, D2-), the coring circuit comprising:

5 - a first pair of cascode transistors (Q1, Q2) biased by a first reference voltage (Vr), for applying a first fraction of each of the components of the differential current to respectively first and second resistors (30, 31);

10 - a second pair of cascode transistors (Q3, Q4) biased by the first reference voltage, for providing a second fraction of each of the components of said differential current to a differential current output (P+, P-) of the coring circuit and respectively to first and second branches of a differential stage (Q5, Q6) that also receives voltages across the first and second resistors; and

15 - two coring current sources (33, 34) are respectively connected to first and second outputs of the differential stage (Q5, Q6) to a supply voltage (GND), the two coring current sources being connected to each other through a third resistor (36).

20 2. The coring circuit of claim 1, wherein the ratio between the value of the second resistor (36) and the value of the first resistors is twice the ratio between the first and second fractions.

3. A peaking/depeaking circuit comprising:

25 - the coring circuit of claim 1;
- a third pair of cascode transistors (Q7, Q8) biased by said reference voltage (Vr), for injecting a third fraction of the components of said differential current respectively into an input branch and an output branch of a current mirror (Q9, Q10);
30 and

- a differential multiplier (Q11, Q14) receiving a differential multiplication voltage (G+, G-) and the differential current output (P+, P-) of the coring circuit, two output branches

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of the multiplier being respectively connected to the branches of the current mirror.

5 4. The peaking/depeaking circuit of claim 3, wherein the differential input current (D2+, D2-) of the coring circuit is obtained from an input voltage (Y), said input voltage delayed once (Y2) and said input voltage delayed twice (Y3), and comprising a differential stage (Q16, Q17) receiving the voltage of the output branch of the current mirror (Q9, Q10) and said input voltage (Y2) delayed once, the two branches of said differential stage being respectively connected to the input and output branches of the current mirror, the voltage of the output branch of the current mirror constituting the output signal (Yp) of the peaking/depeaking circuit.

15 5. The peaking/depeaking circuit of claim 4, wherein the differential input current (D2+, D2-) of the coring circuit is provided by two parallel connected output branches of two differential stages, one of which receives the input voltage (Y) and the input voltage delayed once (Y2), the other stage receiving the input voltage delayed once (Y2) and the input voltage delayed twice (Y3).

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A CORING AND PEAKING CIRCUIT

Abstract of the Disclosure

A coring circuit for an input signal in the form of a differential input current having two components in phase opposition. A first pair of cascode transistors biased by a first reference voltage applies a first fraction of each of the components of the differential current to respectively first and second resistors. A second pair of cascode transistors biased by the first reference voltage provides a second fraction of each of the components of the differential current to a differential current output of the coring circuit and respectively to first and second branches of a differential stage that also receives voltages across the first and second resistors. Two coring current sources respectively connect first and second outputs of the differential stage to a supply voltage and are connected to each other through a third resistor.

Figure 2

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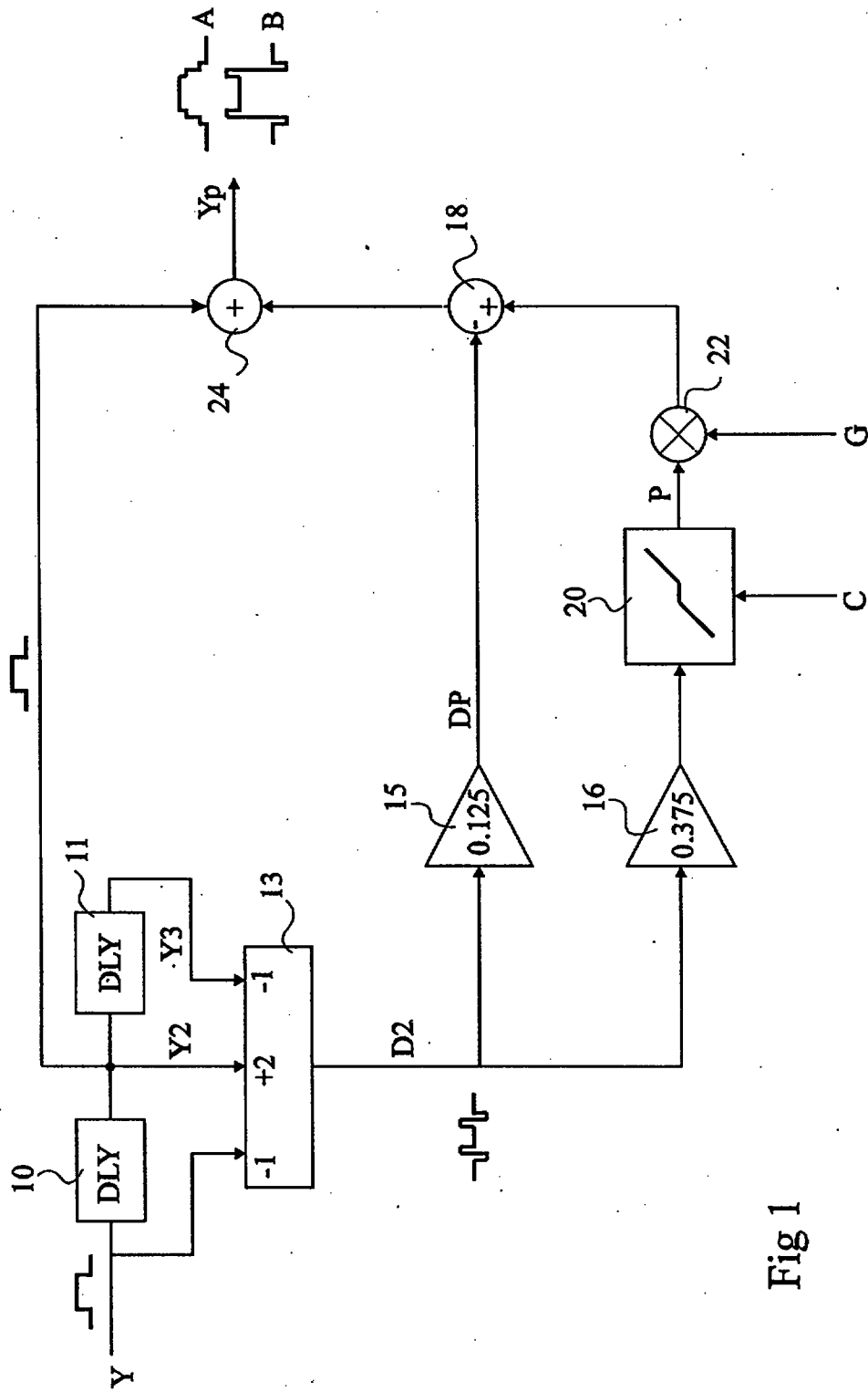
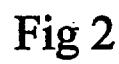


Fig 1



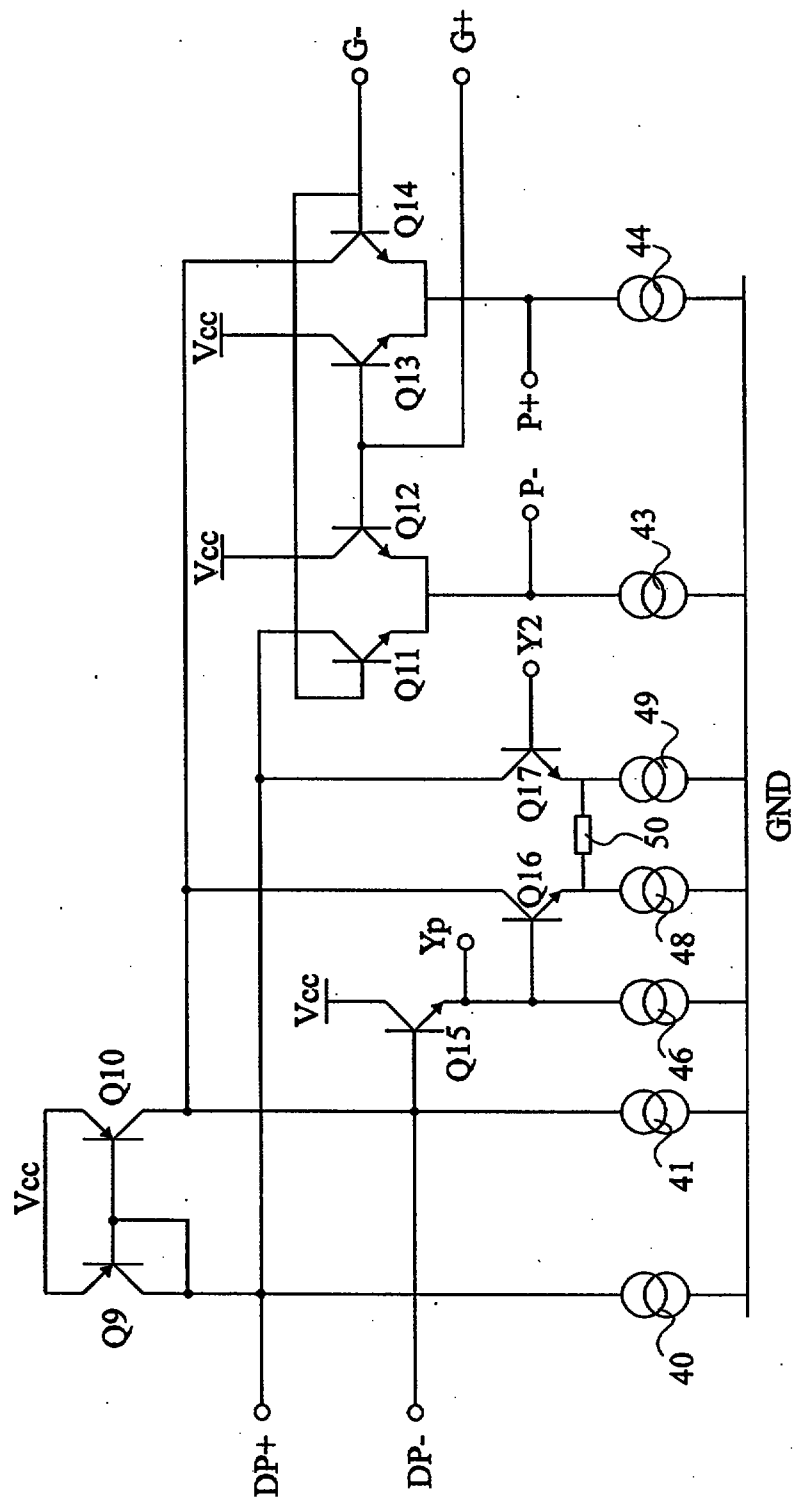


Fig 4

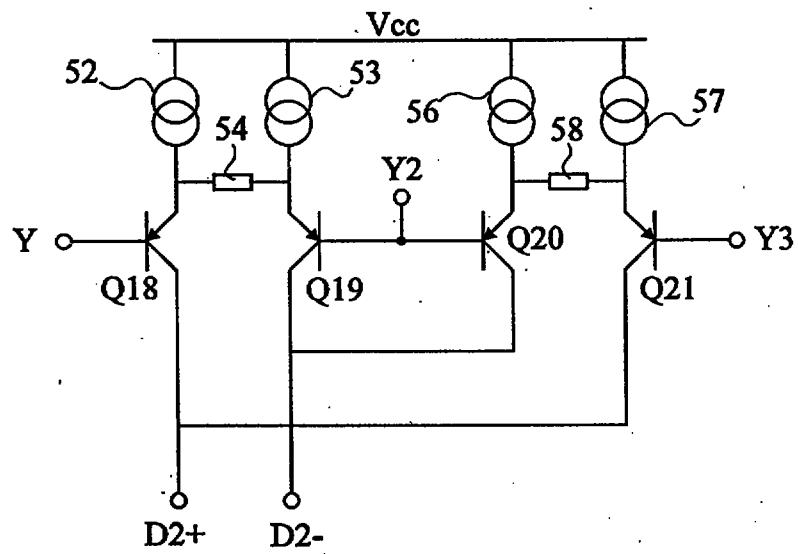


Fig 5

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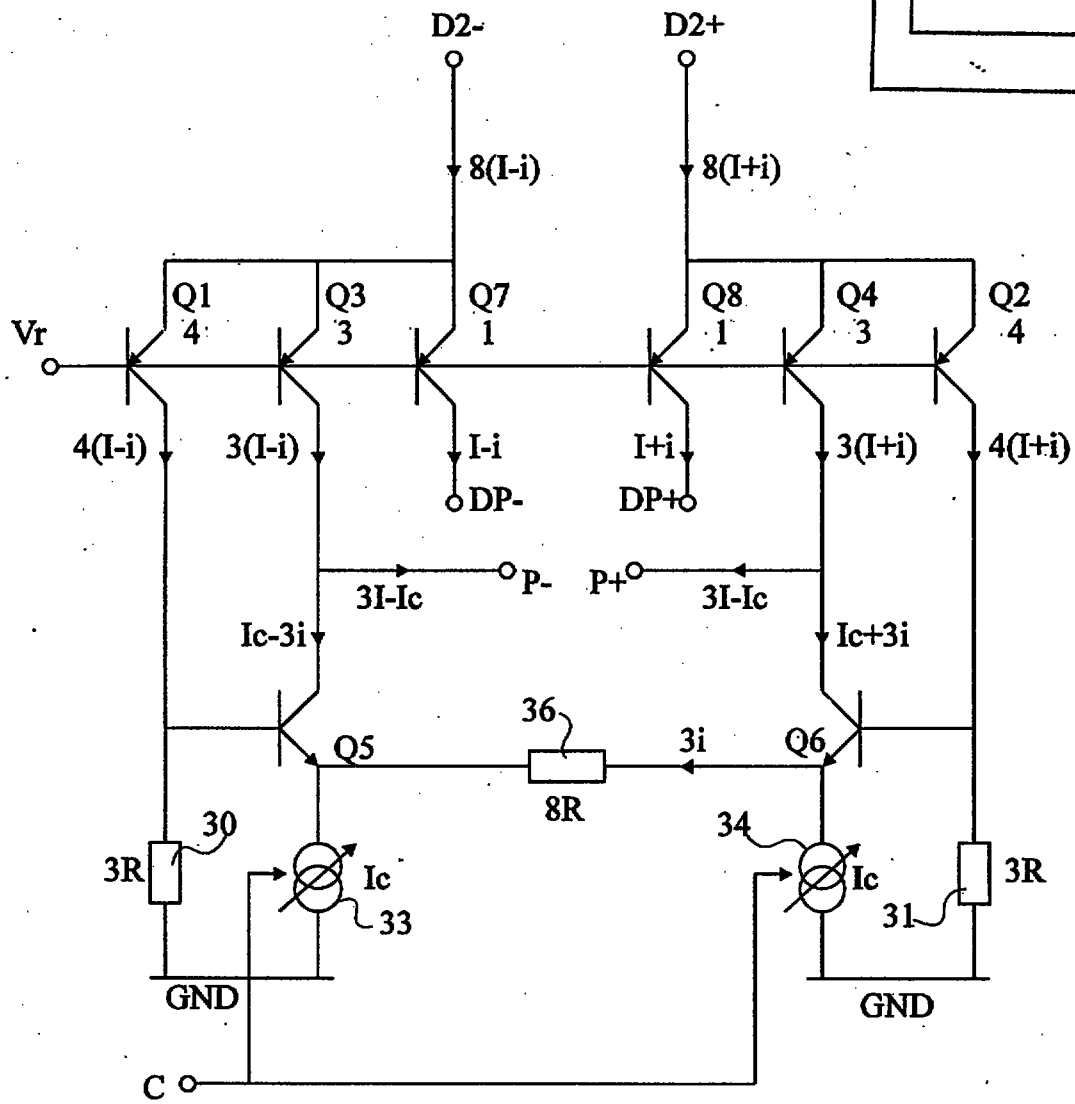


Fig 2

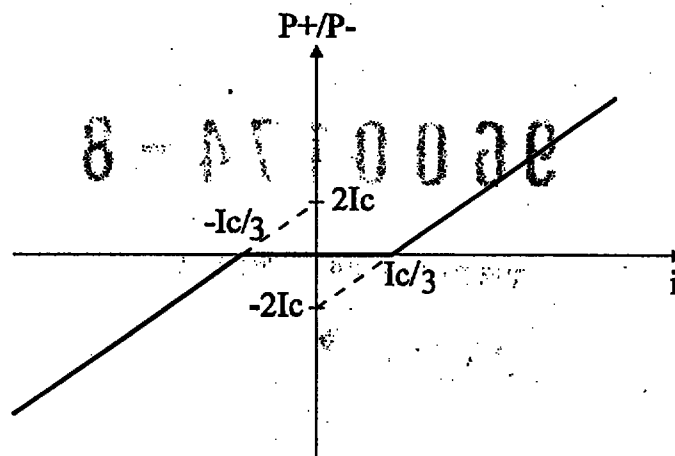


Fig 3



CLAIMS

1. A coring circuit for an input signal (D2), characterized in that the input signal is a differential input current having two components in phase opposition (D2+, D2-), the coring circuit comprising:

5 - a first pair of cascode transistors (Q1, Q2) biased by a same reference voltage (Vr), for applying a first fraction of the components of the differential current to two respective first resistors (30, 31);

10 - a second pair of cascode transistors (Q3, Q4) biased by said reference voltage, for providing a second fraction of the components of said differential current to a differential current output (P+, P-) of the circuit and to first two respective branches of a differential stage (Q5, Q6) receiving the voltages across the first resistors; and

15 - two coring current sources (33, 34) respectively connecting two transistors (Q5, Q6) forming the differential stage to a supply voltage (GND), the two coring current sources being connected to each other through a second resistor (36).

20 2. The coring circuit of claim 1, wherein the ratio between the value of the second resistor (36) and the value of the first resistors is twice the ratio between the first and second fractions.

3. A peaking/depeaking circuit comprising:

25 - the coring circuit of claim 1;
 - a third pair of cascode transistors (Q7, Q8) biased by said reference voltage (Vr), for injecting a third fraction of the components of said differential current respectively into an input branch and an output branch of a current mirror (Q9, Q10); and

30 - a differential multiplier (Q11, Q14) receiving a differential multiplication voltage (G+, G-) and the differential current output (P+, P-) of the coring circuit, two output branches of the multiplier being respectively connected to the branches of the current mirror.

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4. The peaking/depeaking circuit of claim 3, wherein the differential input current (D2+, D2-) of the coring circuit is obtained from an input voltage (Y), said input voltage delayed once (Y2) and said input voltage delayed twice (Y3), and comprising a differential stage (Q16, Q17) receiving the voltage of the output branch of the current mirror (Q9, Q10) and said input voltage (Y2) delayed once, the two branches of said differential stage being respectively connected to the input and output branches of the current mirror, the voltage of the output branch of the current mirror constituting the output signal (Yp) of the peaking/depeaking circuit.

5. The peaking/depeaking circuit of claim 4, wherein the differential input current (D2+, D2-) of the coring circuit is provided by two parallel connected output branches of two differential stages, one of which receives the input voltage (Y) and the input voltage delayed once (Y2), the other stage receiving the input voltage delayed once (Y2) and the input voltage delayed twice (Y3).

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