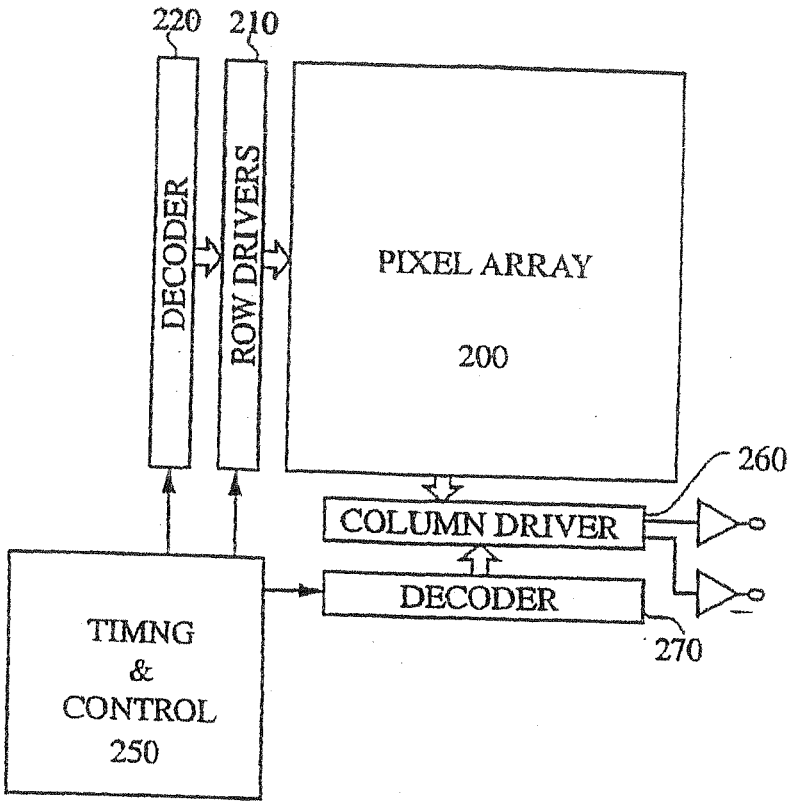

220
210
DECODER
ROW DRIVERS
PIXEL ARRAY
200
260
COLUMN DRIVER
DECODER
270
TIMNG
&
CONTROL
250

FIG. 1

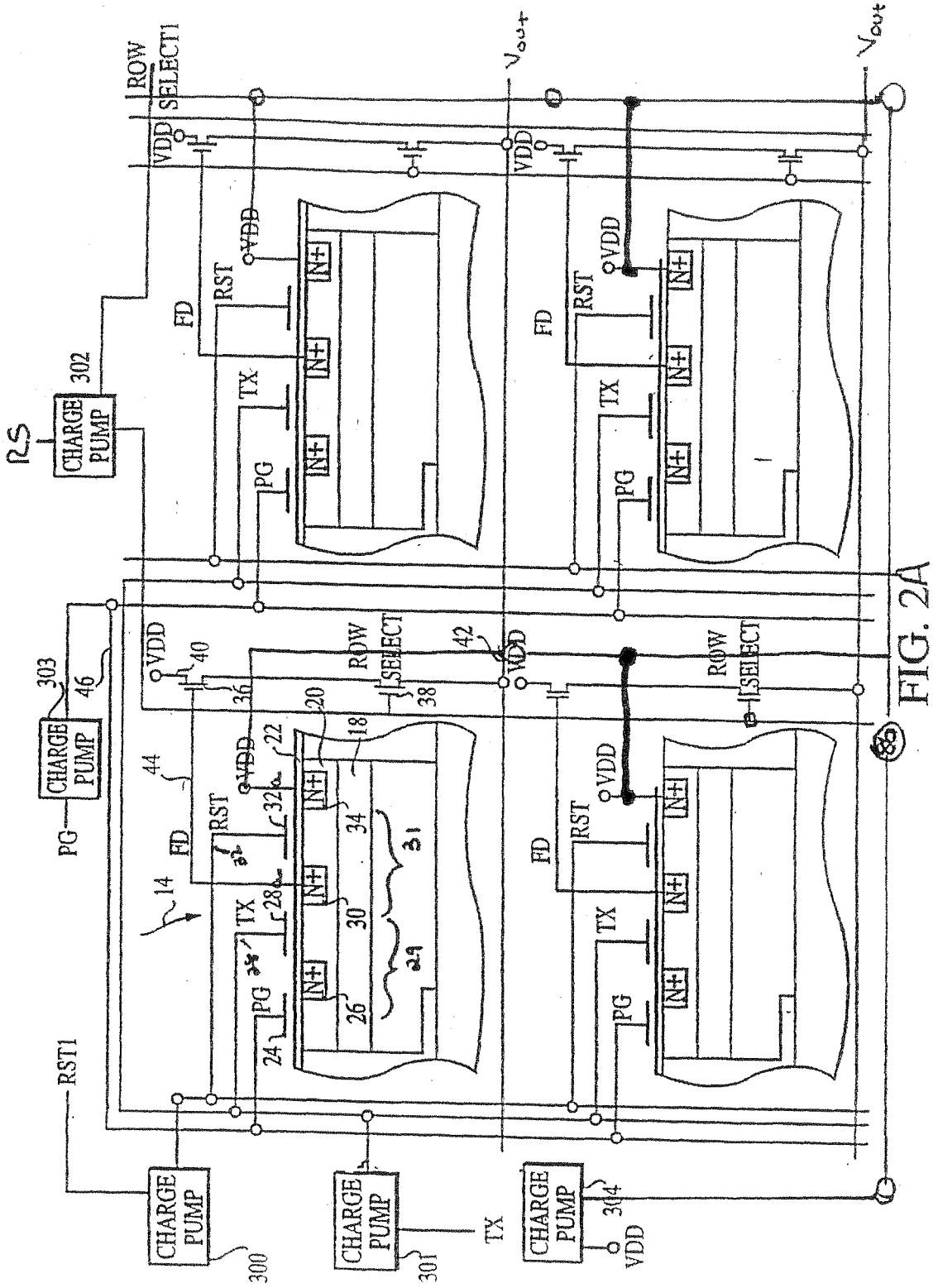

ROW SELECT1
VDD
RST
FD
TX
PG
CHARGE PUMP
302
303
300
301
304
RS
RST1
N+
Vout
ROW SELECT
14
18
20
22
24
26
28
29
30
31
32
34
36
38
40
42
44
46

FIG. 2A

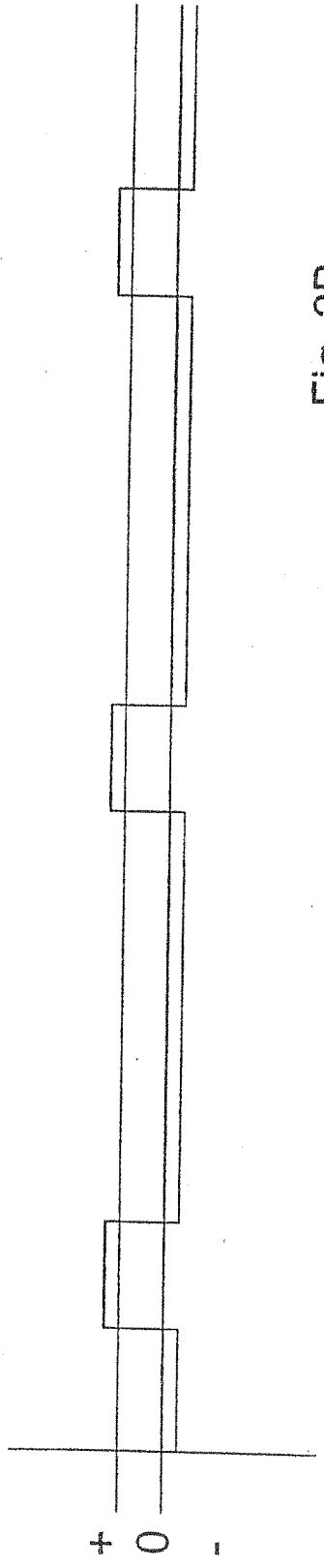


Fig. 2B

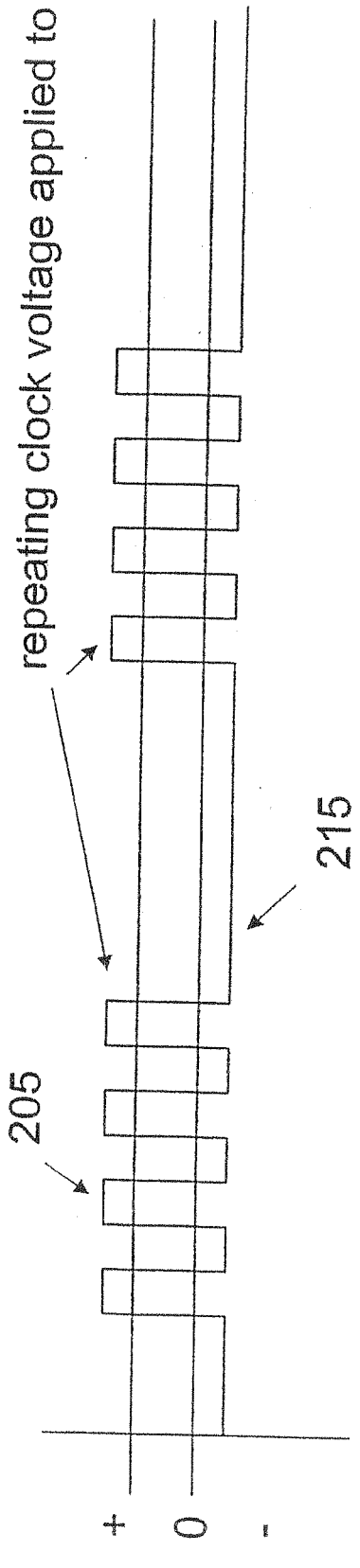


Fig. 2C

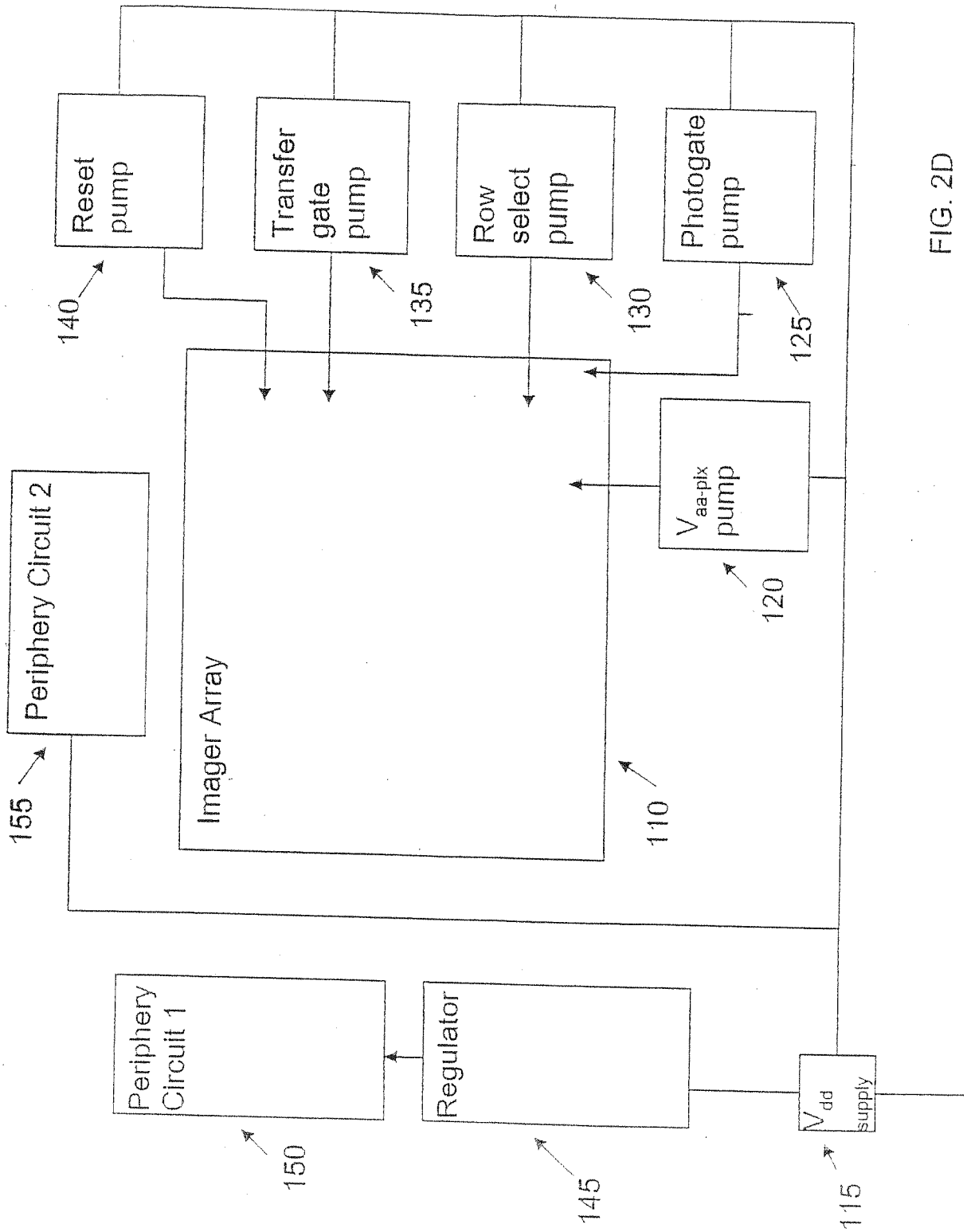

Reset pump
Transfer gate pump
Row select pump
Photogate pump
140
135
130
125
Periphery Circuit 2
Imager Array
V_{aa-pix} pump
155
110
120
Periphery Circuit 1
Regulator
V_{dd} supply
150
145
115

FIG. 2D

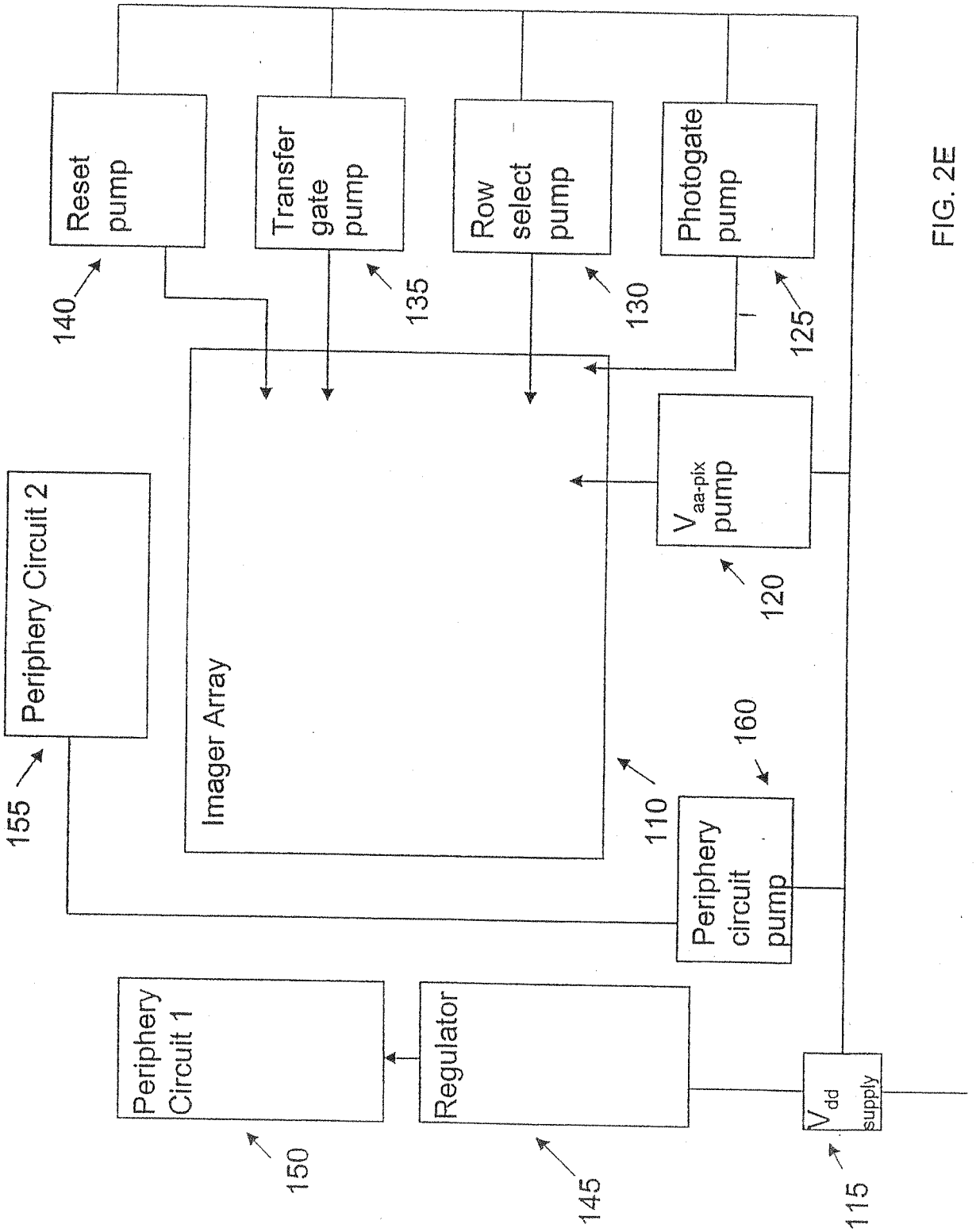

Reset pump
Transfer gate pump
Row select pump
Photogate pump
140
135
130
125
Periphery Circuit 2
155
Imager Array
110
V_{aa-pix} pump
120
160
Periphery circuit pump
Periphery Circuit 1
150
Regulator
145
V_{dd} supply
115

FIG. 2E

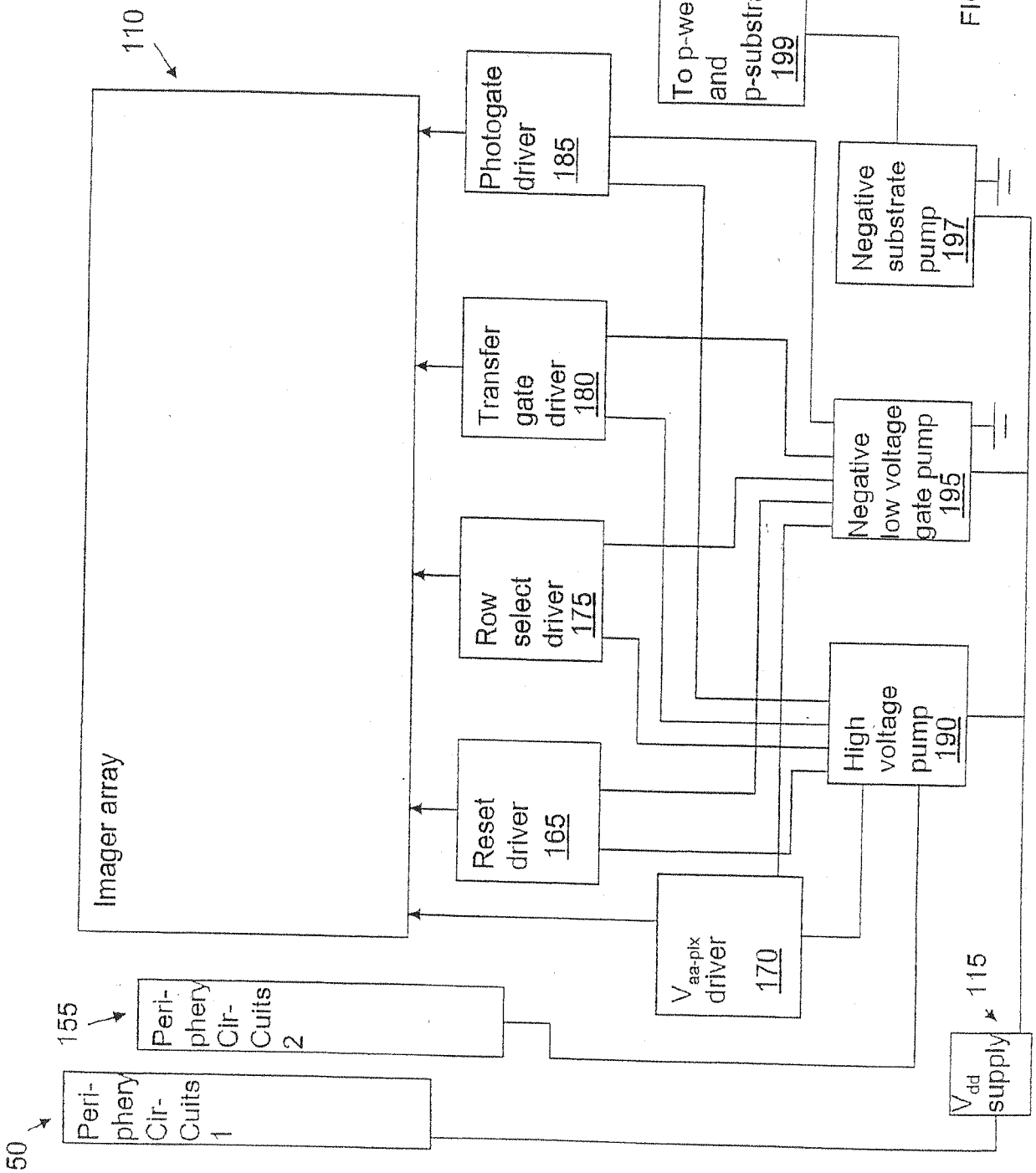

150
Peri-pheny Cir-Cuits 1
155
Peri-pheny Cir-Cuits 2
115
V_{dd} supply
$V_{aa\text{-}pix}$ driver 170
Reset driver 165
Row select driver 175
Transfer gate driver 180
Photogate driver 185
Imager array
110
High voltage pump 190
Negative low voltage gate pump 195
Negative substrate pump 197
To p-well and p-substrate 199

FIG. 2F

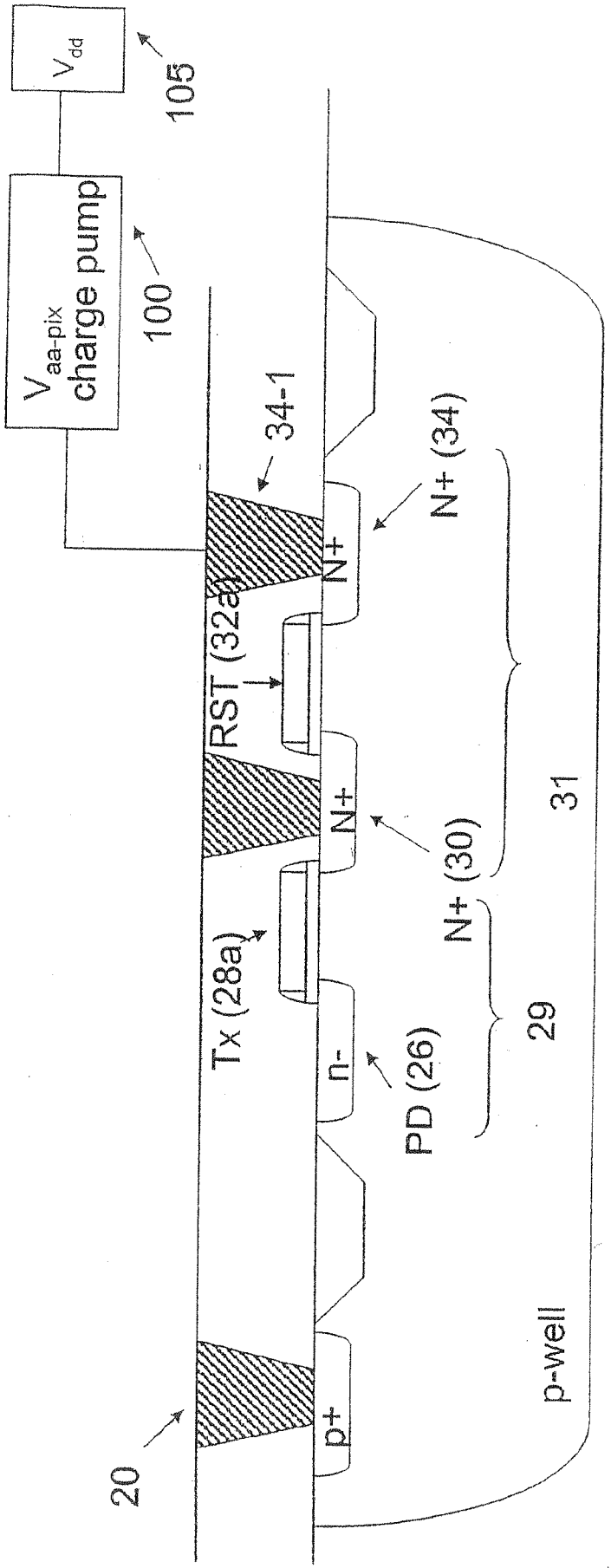

V_{dd}
105
$V_{aa\text{-}pix}$ charge pump
100
34-1
N+ (34)
N+
RST (32a)
N+
N+ (30)
Tx (28a)
n-
PD (26)
29
31
p-well
p+
20

Fig. 3

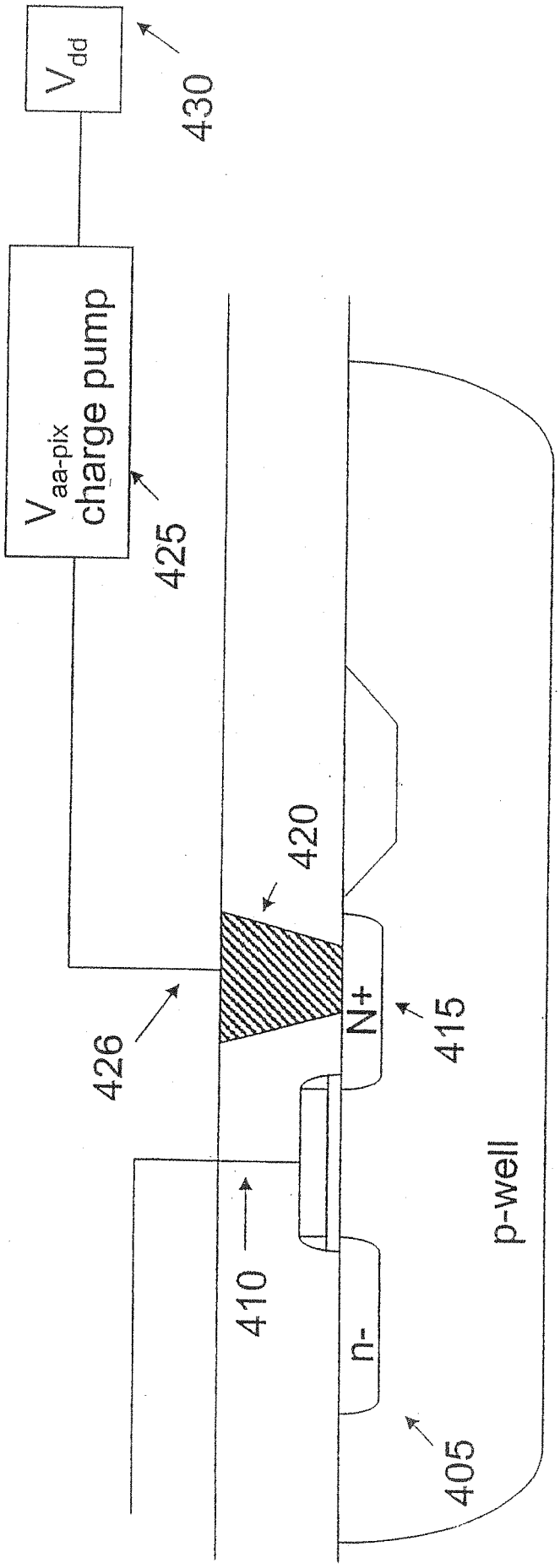

V_{dd}
430
$V_{aa\text{-}pix}$ charge pump
425
420
426
N+
415
410
n-
405
p-well

Fig. 4

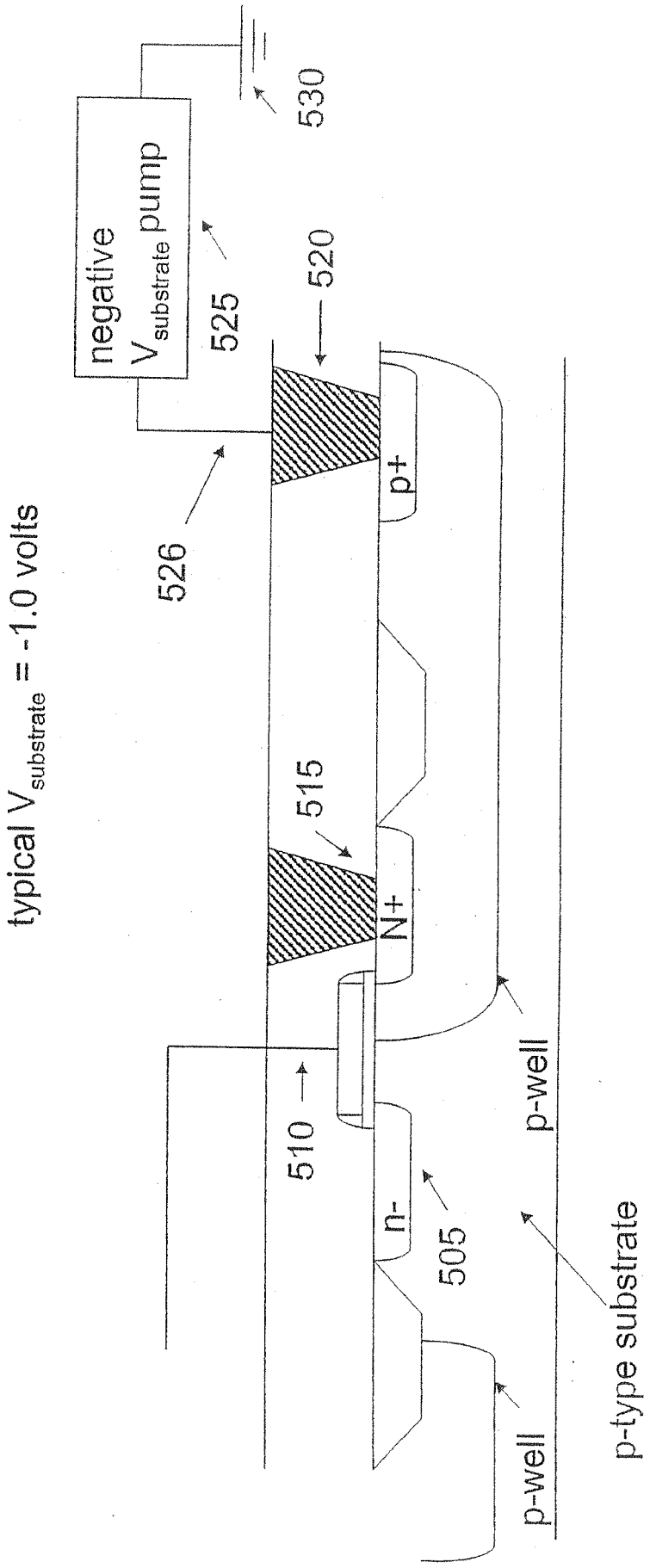

typical $V_{substrate}$ = -1.0 volts
negative $V_{substrate}$ pump
530
525
520
526
515
510
505
p+
N+
n-
p-well
p-well
p-type substrate

Fig. 5

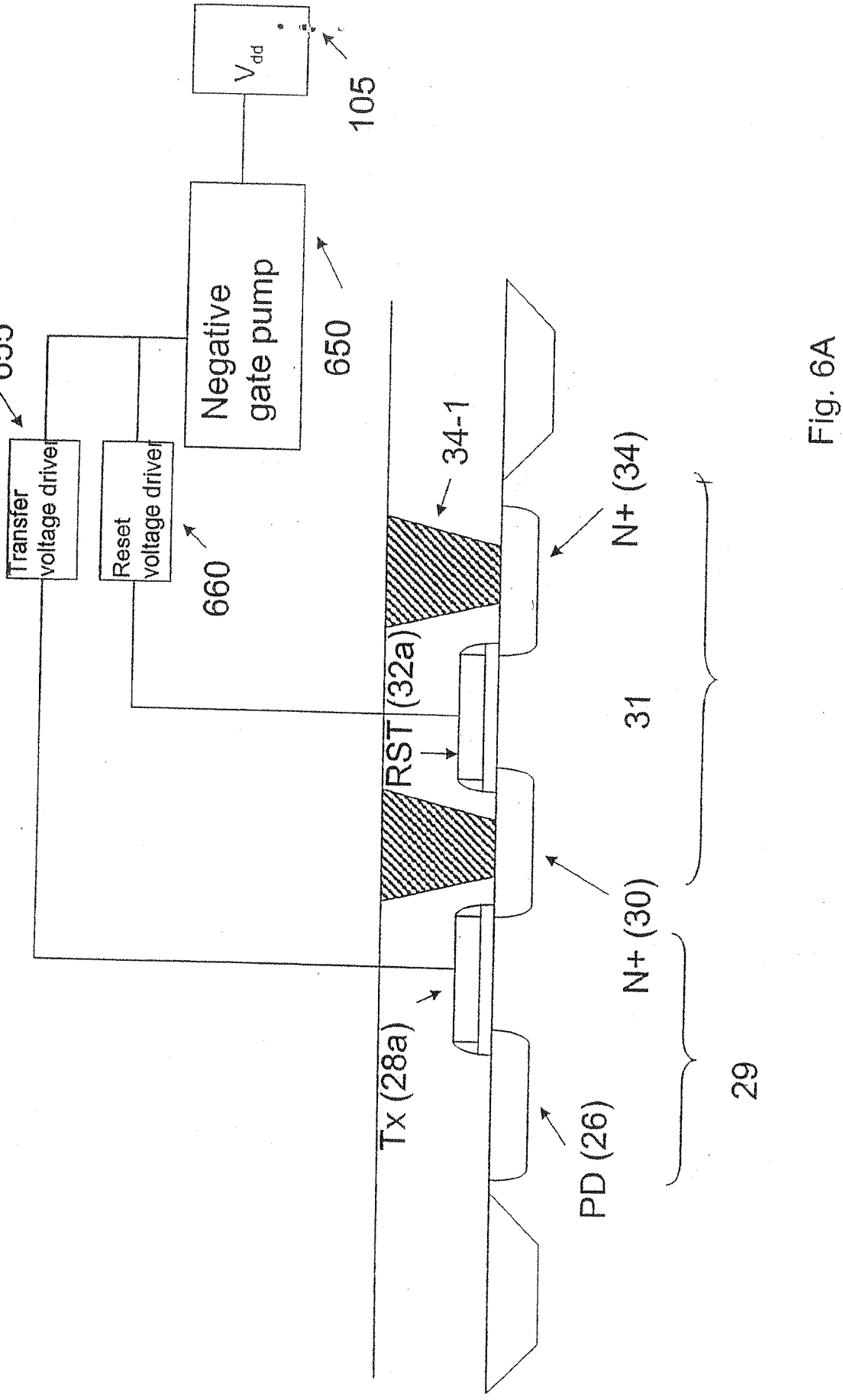

V_{dd}
105
Negative gate pump
650
655
Transfer voltage driver
Reset voltage driver
660
34-1
N+ (34)
RST (32a)
31
Tx (28a)
N+ (30)
PD (26)
29

Fig. 6A

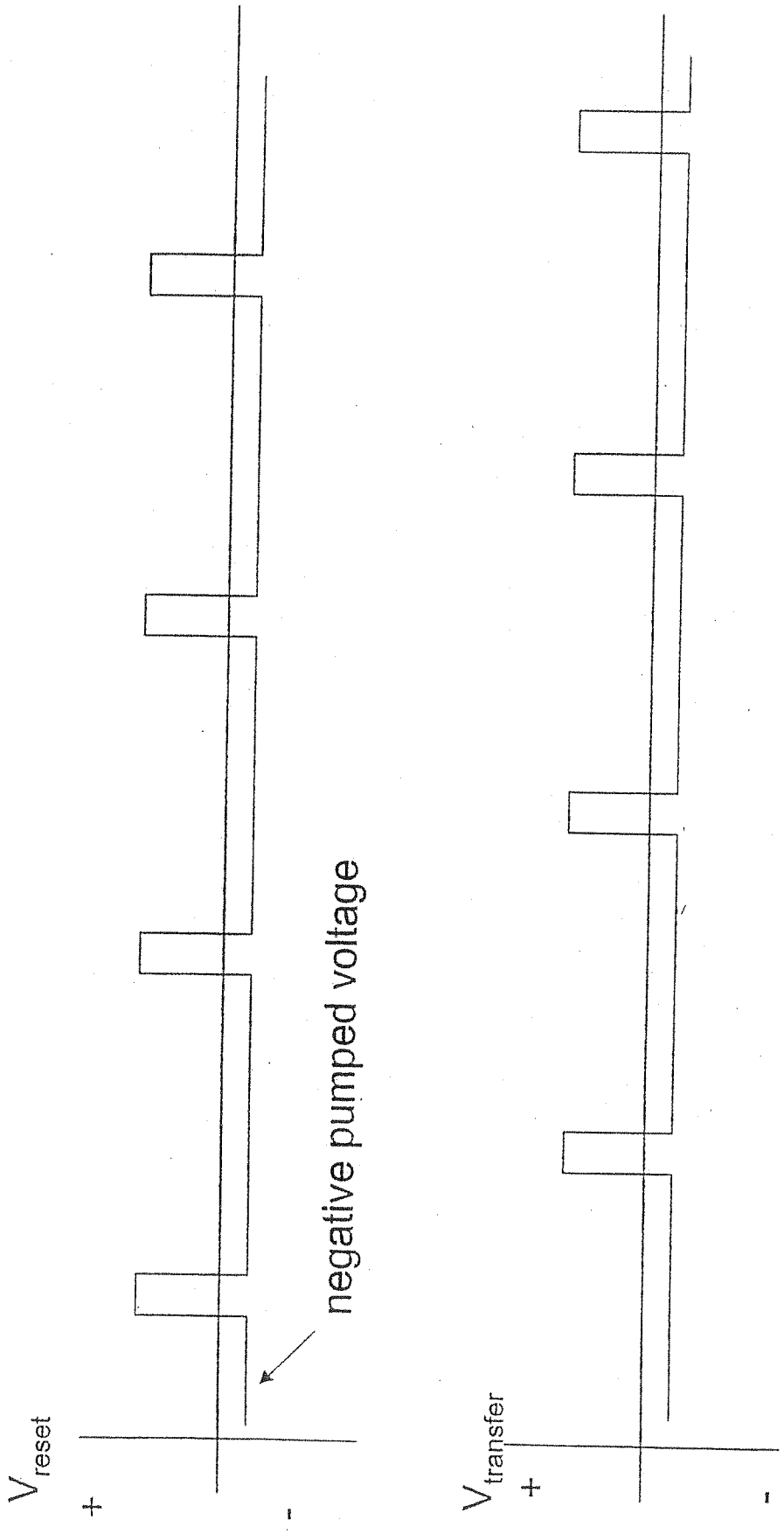


Fig. 6B

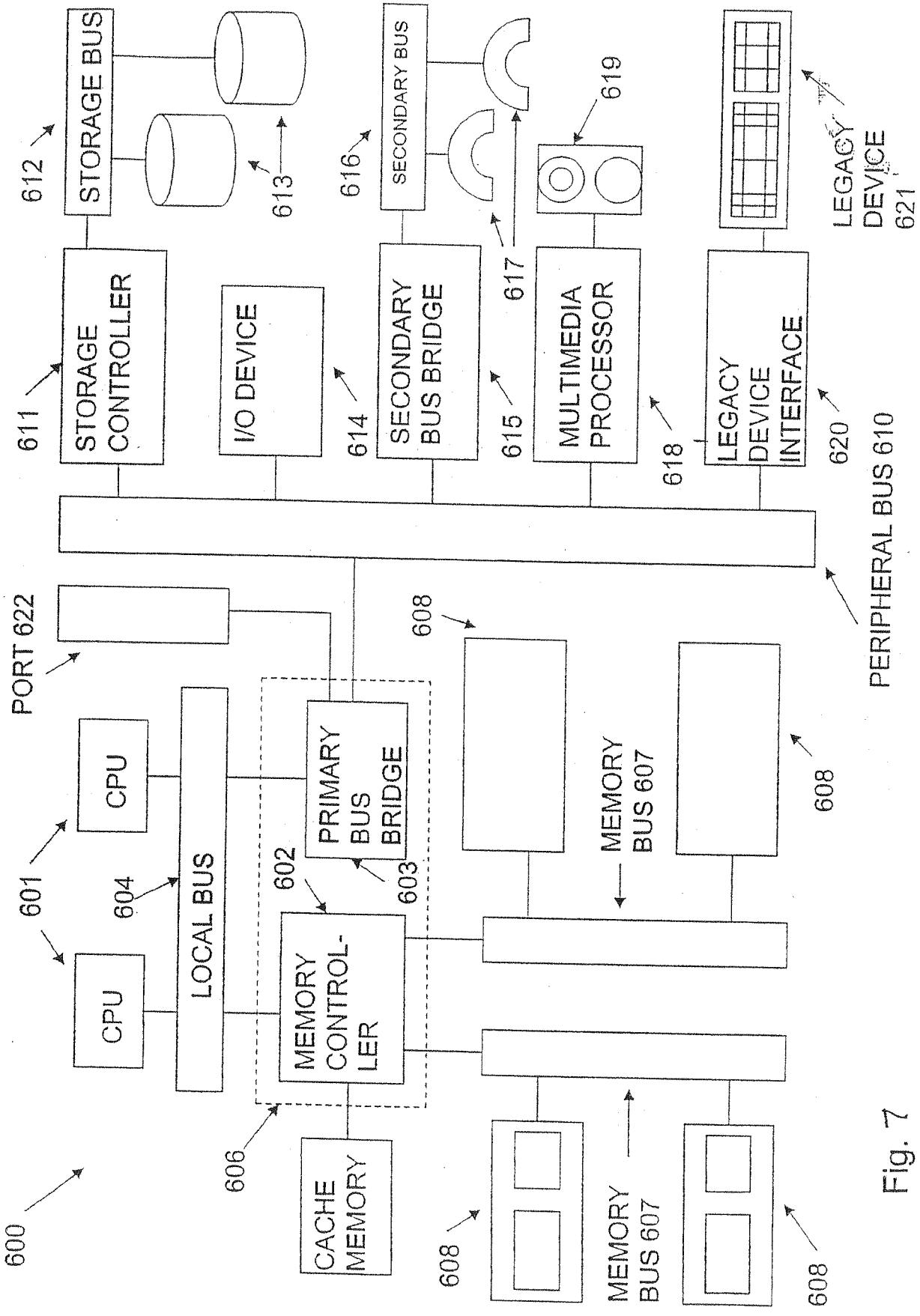

600
601
CPU
CPU
604
LOCAL BUS
602
PRIMARY BUS BRIDGE
603
MEMORY CONTROL-LER
606
CACHE MEMORY
PORT 622
608
608
608
608
MEMORY BUS 607
MEMORY BUS 607
PERIPHERAL BUS 610
611
STORAGE CONTROLLER
612
STORAGE BUS
613
I/O DEVICE
614
SECONDARY BUS BRIDGE
615
616
SECONDARY BUS
617
MULTIMEDIA PROCESSOR
618
619
LEGACY DEVICE INTERFACE
620
LEGACY DEVICE
621

Fig. 7