ABSTRACT

AN IMPROVED METHOD TO FORM SHALLOW TRENCH ISOLATION STRUCTURES

A method of forming a shallow trench isolation trenches in a silicon substrate of an integrated circuit device is achieved. A silicon substrate is provided. A buffer layer is deposited overlying the silicon substrate. An etching endpoint layer is deposited overlying the buffer layer. A silicon layer is deposited layer overlying the etching endpoint layer. A photoresist layer is coated overlying the silicon layer. The photoresist layer is developed wherein the photoresist layer is removed where the trenches are planned. The silicon layer, the etching endpoint layer, and the buffer layer are etched through to expose the top surface of the silicon substrate. The silicon layer and the silicon substrate layer are etched until the top surface of the etching endpoint layer is exposed, and the trenches are thereby formed. The integrated circuit device is completed.

(FIGURE 2 IS SUGGESTED FOR PUBLICATION)