CLAIMS

What is claimed is:

1. A video decoding apparatus, comprising one or more processors, wherein the one or more processors are configured to:

determine that affine mode is enabled for a video sequence;

determine, based on a value of an adaptive motion vector difference resolution (AMVR) enablement indicator, whether an affine mode AMVR enablement indicator is present in a parameter set associated with the video sequence; and

decode the video sequence based on the determination of whether the affine mode AMVR enablement indicator is present in the parameter set associated with the video sequence.

2. The video decoding apparatus of claim 1, wherein, on a condition that the value of the AMVR enablement indicator indicates AMVR mode is enabled for the video sequence, the one or more processors are configured to determine that the affine mode AMVR enablement indicator is present in the parameter set associated with the video sequence, and, on a condition that the value of the AMVR enablement indicator indicates AMVR mode is disabled for the video sequence, the one or more processors are configured to determine that the affine mode AMVR enablement indicator is not present in the parameter set associated with the video sequence.

3. The video decoding apparatus of claim 1, wherein the one or more processors are further configured to:

set the value of the AMVR enablement indicator to a value indicative of disabling AMVR for the video sequence based on general constraint information (GCI); and

determine that the affine mode AMVR enablement indicator is not present in the parameter set associated with the video sequence based on the value of the AMVR enablement indicator indicative of disabling AMVR for the video sequence.

4. The video decoding apparatus of claim 1, wherein the one or more processors are further configured to:

determine that intra-block copy (IBC) is enabled for the video sequence; and

obtain an IBC AMVR enablement indicator in response to the determination that IBC is enabled for the video sequence, wherein the video sequence is decoded based on the IBC AMVR enablement indicator.

5. A video decoding method, comprising:

determining that affine mode is enabled for a video sequence;

determining, based on a value of an adaptive motion vector difference resolution (AMVR) enablement indicator, whether an affine mode AMVR enablement indicator is present in a parameter set associated with the video sequence; and

decoding the video sequence based on the determination of whether the affine mode AMVR enablement indicator is present in the parameter set associated with the video sequence.

6. The video decoding method of claim 5, further comprising, on a condition that the value of the AMVR enablement indicator indicates AMVR is enabled for the video sequence, determining that the affine mode AMVR enablement indicator is present in the parameter set associated with the video sequence, and, on a condition that the value of the AMVR enablement indicator indicates AMVR is disabled for the video sequence, determining that the affine mode AMVR enablement indicator is not present in the parameter set associated with the video sequence.

7. The video decoding method of claim 5, further comprising:

setting the value of the AMVR enablement indicator to a value indicative of disabling AMVR for the video sequence based on general constraint information (GCI); and

determining that the affine mode AMVR enablement indicator is not present in the parameter set associated with the video sequence based on the value of the AMVR enablement indicator indicative of disabling AMVR for the video sequence.

8. The video decoding method of claim 5, further comprising:

determining that intra-block copy (IBC) is enabled for the video sequence; and

obtaining an affine mode IBC enablement indicator in response to the determination that IBC is enabled for the video sequence, wherein the video sequence is decoded based on the affine mode IBC enablement indicator.

9. A video encoding apparatus, comprising one or more processors, wherein the one or more processors are configured to:

determine that an affine mode is enabled for a video sequence;

determine, based on a value of an adaptive motion vector difference resolution (AMVR) enablement indicator, whether to include an affine mode AMVR enablement indicator in a parameter set associated with the video sequence; and

generate the parameter set associated with the video sequence based on the determination of whether to include the affine mode AMVR enablement indicator in the parameter set associated with the video sequence.

10. The video encoding apparatus of claim 9, further comprising, on a condition that the value of the AMVR enablement indicator indicates AMVR is enabled for the video sequence, determining that the affine mode AMVR enablement indicator is present in the parameter set associated with the video sequence, and, on a condition that the value of the AMVR enablement indicator indicates AMVR is disabled for the video sequence, determining that the affine mode AMVR enablement indicator is not present in the parameter set associated with the video sequence.

11. The video encoding apparatus of claim 9, further comprising:

determining that intra-block copy (IBC) is enabled for the video sequence; and

obtaining an affine mode IBC enablement indicator in response to the determination that IBC is enabled for the video sequence, wherein the video sequence is decoded based on the affine mode IBC enablement indicator.

12. A video encoding method, comprising:

determining that an affine mode is enabled for a video sequence;

determining, based on a value of an adaptive motion vector difference resolution (AMVR) enablement indicator, whether to include an affine mode AMVR enablement indicator in a parameter set associated with the video sequence; and

generating the parameter set associated with the video sequence based on the determination of whether to include the affine mode AMVR enablement indicator in the parameter set associated with the video sequence.

13. The video encoding method of claim 12, further comprising, on a condition that the value of the AMVR enablement indicator indicates AMVR is enabled for the video sequence, determining that the affine mode AMVR enablement indicator is present in the parameter set associated with the video sequence, and, on a condition that the value of the AMVR enablement indicator indicates AMVR is disabled for the video sequence, determining that the affine mode AMVR enablement indicator is not present in the parameter set associated with the video sequence.

14. The video encoding method of claim 12, further comprising:

determining that intra-block copy (IBC) is enabled for the video sequence; and

obtaining an affine mode IBC enablement indicator in response to the determination that IBC is enabled for the video sequence, wherein the video sequence is decoded based on the affine mode IBC enablement indicator.

15. A computer readable medium including instructions for causing one or more processors to perform the method of any one of claims 5-8 and 12-14.