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POWER AMPLIFIER

ABSTRACT

A power amplifier has an input terminal for receiving a signal to be amplified and an output terminal to which the amplified signal is passed, and comprises single stage which-, or a plurality of cascaded amplifier stages one of, which-, is formed from a plurality of amplifiers connected in parallel with their input ports interconnected and their output ports interconnected. Said one stage may be the last stage. In one arrangement said one stage comprises two or more amplifiers at least one of which is biased at class AB and at least another of which is biased at class C. Alternatively said one stage comprises two or more amplifiers at least one of which is biased at class AB and at least another of which may be switchably biased at class AB or class C.

Again, alternatively, the said one stage may comprise two or more amplifiers, each of which may be switchably biased at class AB or class C and the gates widths of which may be different. The amplifier stages may comprise bipolar junction transistors or field effect transistors. Means are preferably provided enabling the power to be divided to the input to each amplifier in said one stage and means enabling the outputs of each of said amplifiers to be combined. There may be provided between the power dividing point to the input of each of said amplifiers a matching circuit enabling phase shifting to compensate for the amplitude and phase response of each of said amplifiers. In said one stage there may be provided between the output ports of each of said amplifiers and the combining point a matching circuit enabling phase shifting to compensate for the amplitude and phase response of each of said amplifiers.

(Fig. 1)