transistor 303 of Fig. 1 is reported on Fig. 2b. The result is that the total size is of the order of $6W_{303}$. Thus, the circuit of Figs. 2a and 2b proves to be actually simpler than that of Fig. 1, nevertheless it remains area consuming.

SHORT DESCRIPTION OF THE INVENTION

Embodiments of the invention seek to provide a circuit which does not have the drawbacks mentioned earlier, in particular a relatively not very bulky, low consumption circuit, which may be used as a wordline driver circuit in a memory array.

Embodiments of the invention also seek to provide a particularly simple and not very bulky circuit which may be used for providing different logic functions.

According to a first aspect of the present invention, there is provided a circuit including a transistor of P-type channel in series with a transistor of N-type channel between first and second terminals for applying a power supply potential, each of the transistors being a multiple gate transistor having at least a first and a second independent control gates, said transistor of P-type channel having a source connected to the first terminal for applying a power supply potential and said transistor of N-type channel having a source connected to the second terminal for applying a power supply potential, wherein at least one of the transistors is configured for operating in a depletion mode under the action of a second gate signal applied to its second control gate, wherein said circuit provides the logic NOR function with respect to the first gate signal and the second gate signal, the output being the common drain of the transistor of P-type channel and the transistor of N-type channel, and wherein the second control gates are biased by a same second gate signal and the first terminal for application of a power supply potential is biased by the complementary signal of said second gate signal, whereas the second terminal for application of a power supply potential is biased at an OFF state.

According to a second aspect of the present invention, there is provided a circuit including a transistor of a P-type channel in series with a transistor of a N-type channel between first and second terminals for applying a power supply potential, each of the transistors being a multiple gate transistor having at least a first and a second independent control gates, said transistor of P-type channel having a source connected to the first terminal for applying a power supply potential and said transistor of N-type channel having a source connected to the second terminal for applying a power supply potential, wherein said circuit provides the logic NAND

function with respect to the first gate signal and the signal biasing the first terminal for application of a power supply potential, the output being the common drain of the transistor of P-type channel and the transistor of N-type channel, and wherein at least one of the transistors is configured for operating in a depletion mode under the action of a second gate signal applied to its second control gate, wherein the second control gates are biased by a same second gate signal and wherein the second terminal for application of a power supply potential is biased by the complementary signal of said second gate signal, the first terminal for application of a power supply potential is biased to a ON state.

Certain preferred but non-limiting embodiments of this device are the following:

- the transistor of the second type of channel is configured in order to operate in a depletion mode when the second gate signal is in the ON state;

CLAIMS

1. A circuit including a transistor of P-type channel in series with a transistor of N-type channel between first and second terminals for applying a power supply potential, each of the transistors being a multiple gate transistor having at least a first and a second independent control gates, said transistor of P-type channel having a source connected to the first terminal for applying a power supply potential and said transistor of N-type channel having a source connected to the second terminal for applying a power supply potential,
wherein at least one of the transistors is configured for operating in a depletion mode under the action of a second gate signal applied to its second control gate,
wherein said circuit provides the logic NOR function with respect to the first gate signal and the second gate signal, the output being the common drain of the transistor of P-type channel and the transistor of N-type channel, and
wherein the second control gates are biased by a same second gate signal and the first terminal for application of a power supply potential is biased by the complementary signal of said second gate signal, whereas the second terminal for application of a power supply potential is biased at an OFF state.

2. The circuit according to claim 1, wherein the transistor of the N-type of channel is configured in order to operate in a depletion mode when the second gate signal is in the ON state.

3. A circuit including a transistor of a P-type channel in series with a transistor of a N- type channel between first and second terminals for applying a power supply potential, each of the transistors being a multiple gate transistor having at least a first and a second independent control gates, said transistor of P-type channel having a source connected to the first terminal for applying a power supply potential and said transistor of N-type channel having a source connected to the second terminal for applying a power supply potential,

wherein said circuit provides the logic NAND function with respect to the first gate signal and the signal biasing the first terminal for application of a power supply potential, the output being the common drain of the transistor of P-type channel and the transistor of N-type channel, and

wherein at least one of the transistors is configured for operating in a depletion mode under the action of a second gate signal applied to its second control gate, wherein the second control gates are biased by a same second gate signal and wherein the second terminal for application of a power supply potential is biased by the complementary signal of said second gate signal, the first terminal for application of a power supply potential is biased to a ON state.

4. The circuit according to claim 3, wherein the transistor of the P-type of channel is configured in order to operate in a depletion mode when the second gate signal is in the OFF state.