In the case of view data (BTX), it is known to transmit a so-called FSK (frequency shift keying) signal over the telephone network. This signal is a sinusoidal oscillation, the frequency of which is switched over between two values according to a digital signal to be transmitted. The one frequency is 1,300 Hz and corresponds, in the digital signal, to the logical value HIGH or 1. The second frequency is 2,100 Hz and corresponds, in the digital signal, to the logical value LOW or 0.

Such an FSK signal is an analogue signal from which a digital signal is produced in a decoder. The digital signal then serves, for example in a character generator, for the production of character signals which, after storage of the FSK signals transmitted over a relatively long period of time, represent a printed page on the screen of a television receiver.

For the decoding of the FSK signal, it is known to supply the signal to a PLL phase control loop of which the voltage-controlled oscillator (VCO) is adjusted to the frequency of the FSK signal each time. On a variation in the frequency of the FSK signal, the control voltage obtained in the phase comparison stage of the PLL circuit and conveyed through a low-pass filter must be altered for this adjustment. Thus this varying voltage contains the information contained in the FSK signal. It is supplied, as a signal voltage, through a further low-pass filter, to a circuit with a threshold-value characteristic, for example a trigger stage, which produces, at its output, a digital signal corresponding to the frequency-shift keying of the FSK signal. Such an FSK decoder with a PLL circuit is described in more detail in the company pamphlet "FSK Demodulator/Tone Decoder" No. XR-2211 of the firm EXAR INTEGRATED SYSTEMS, INC., October 1976, pages 1-6.

The values of the said signal voltage at the input of the trigger stage are dependent on various factors, for example on the frequencies of the FSK signal, on the natural frequency of the oscillator of the PLL circuit and on tolerances in the individual components. These parameters are subject to fluctuations in practice so that the digital signal at the output of the said trigger stage can be falsified. A portion of the signal which corresponds, for example, to a signal portion of a specific frequency in the FSK signal may then be shortened for example. As a result, so-called isochronous distortions develop during the decoding of the digital signal.

In order to avoid such isochronous distortions, it is necessary to adjust the PLL decoder accurately. This adjustment is necessary during the manufacture of the decoder. If variations in the said parameters occur later, a re-adjustment may also be necessary during the operating time.

An FSK decoder with a PLL circuit to compensate for frequency fluctuations in FM systems is known from DE-A-30 22 287. The frequency fluctuations are controlled by acting on the VCO of the PLL by means of a control voltage which is obtained from the difference between signal voltage and a reference voltage.

Furthermore, it is known from CE-C-11 31 260 to derive from a signal voltage for frequency-keyed telegraphy, by means of a discriminator, a mean d.c. voltage component which can be used for a follow-up control, for example of an oscillator.

It is the object of the invention to develop a decoder for frequency-keyed signals so that no adjustment is necessary either during manufacture or in operation and yet no isochronous distortions occur.

This problem is solved by the invention described in Claim 1. Advantageous further developments of the invention are described in the sub-claims.

With the solution according to the invention, therefore, an adjustment is always carried out automatically so that a single adjustment during production or a repeated manual adjustment during operation is no longer necessary. The adjustment according to the invention acts quasi statically and always establishes the optimum conditions even over a long period of time. Since the adjustment is essentially necessary only for deviations which occur once or occur slowly, the circuit can be provided with a very high time constant. This has the advantage that the additional compensating circuit is largely protected from disturbances.

One example of embodiment of the invention will be explained with reference to the drawing.

In this

Figure 1 shows a block circuit diagram of a known decoder with the circuit according to the invention,

Figure 2 shows an example of a practical embodiment of the AFC circuit in Figure 1 with voltage-limiting diode,

Figures 3, 4 show curves to explain the mode of operation of the adjustment according to the invention and

Figure 5 shows an example of a practical embodiment of the AFC circuit in Figure 1 with stand-by voltage sources which can be connected in.

In Figure 1, the FSK signal 2, the frequency of which is shifted between the value f1 = 1,300 Hz (logical 1) and the value f2 = 2,100 Hz (logical 0), appears at the terminal 1. The signal 2 reaches the PLL circuit with the phase comparison stage 3, the low-pass filter 4

and the voltage-controlled oscillator 5 in the form of a VCO. Through the further low-pass filter 6, the phase comparison stage 4 delivers the signal voltage Us, the value of which changes between two values according to the frequency shift keying of the signal 2. The signal voltage Us reaches the comparison stage 7 to which a constant reference voltage Uref is also supplied from the voltage source 9. The comparison stage 7 is so dimensioned that a digital signal 10 with the two voltage values 0 and 1 corresponding to the voltage values of the signal voltage Us appears at the output terminal 8. The circuit described so far is known.

In addition, the AFC circuit 11 is provided which is fed with the signal voltage Us and the reference voltage Uref. The circuit 11 detects the amplitude position of the signal voltage Us at the terminal a in relation to the reference voltage Uref at the terminal b. On a variation in the two values of the voltage Us, which leads to a change in the digital signal 10 and causes isochronous distortions, a control voltage Ur appears at the terminal c at the output of the circuit 11. This control voltage alters the natural frequency of the oscillator 5, that is to say the position of its characteristic curve in relation to the frequency axis, in such a manner that the signal voltage Us again assumes the correct amplitude position in relation to the reference voltage Uref.

Figure 2 shows the practical embodiment of the circuit 11, the terminals a, b, c in Figures 1 and 2 corresponding to one another. The positive value of the signal voltage Us at the terminal a is stored in the capacitor C1 through the transistor T2 and the negative value of the signal voltage Us at the

capacitor C2 through the complementary transistor T1. The capacitors C1, C2 are connected to one another through the resistors R1, R2. The junction point d is connected to the "+" input of the amplifier 12 to the "-" input of which, the reference voltage Uref is applied from the terminal b through the resistor R3. The control voltage Ur shown in Figure 1 appears at the output terminal c. The RC network R4/C3 from the output to the "-" input of the amplifier 12 forms a time constant of 470 ms corresponding to a limit frequency of 0.338 Hz.

Figure 3 shows the correct amplitude position of the signal voltage Us in relation to the reference voltage Uref at the inputs of the comparison stage 7. The signal voltage Us changes between the values U1 and U2, the differences $\Delta U1$ and $\Delta U2$ of which from the reference voltage Uref are equal as desired. Each time the signal voltage Us passes through the reference voltage Uref, the value of the digital voltage 10 at the terminal 8 changes. Let it be assumed that the component of the voltage 10 from t1-t3 is interrogated in the middle between t1 and t3 at t2 in an evaluation circuit connected to the terminal 8, for example in a USART device for serial data transmission. In the case illustrated, the logical state 0 is found during this interrogation.

In Figure 4, the signal voltage Us is displaced in the positive direction in relation to the reference voltage Uref as a result of deviation in the parameters described so that the signal component of the digital voltage 10 with the logical value 0 is shortened. If this shortening reaches the order of magnitude of 50% as illustrated in broken lines in Figure 3, the evaluation of the signal 10 at the moment t2 becomes uncertain and can lead to erroneous evaluations of the digital signal 10 in the circuit connected up.

In the control circuit according to the invention, with the deviation illustrated in Figure 4, the natural frequency of the oscillator 5 is now altered by the control voltage Ur so that the signal voltage Us in Figure 4 is again displaced in the direction of the arrow 13 into the position in relation to the reference voltage Uref shown in Figure 3 so that the shortening of the signal 10 illustrated in Figure 4 no longer occurs.

In Figure 2, the voltage at the capacitor C2 is limited by the diode D1 to the voltage value at the junction point of the resistors R8 and R9 of +0.7 V forward voltage. This voltage limitation has the following purpose:

During asynchronous, serial data transmission, only the frequency f1 = 1,300 Hz corresponding to the stop bit or the logical state "1" is transmitted during the intervals in transmission. As a result, a reversal of the charge of the capacitor C2 occurs because the signal level belonging to f2 = 2,1000 Hz, through which the capacitor C2 is charged to or kept at a value below the reference voltage, is not present over any length of time. As a result of the reversal of the charge of the capacitor C2, because of the asymmetrical position of the reference voltage Uref from $\Delta U1$ and $\Delta U2$, a control operation is initiated until there is no longer any deviation from Uref at the point d. Without the diode D1, this would lead to $\Delta U1$ and $-\Delta U2$ each corresponding to the peak value of the disturbing signal superimposed on the voltage U1. In this case, the arithmetical mean value of the disturbing signal would correspond to the reference voltage Uref and so lead to a decoding of a non-existent signal. This is prevented by the diode D1 in that $\Delta U2$ is limited to a maximum voltage value which, at least in the value of the amplitude of the disturbing

signal on U1, differs in the negative direction from Uref but on the other hand does not lie within the range of variation of ΔU2.

In an example of embodiment which has been tried out in practice, the components illustrated in Figure 2 had the following values.

R1: 220 kOhm
R2: 220 kOhm
R3: 100 kOhm
R4: 1.0 MOhm
R5: 47 kOhm
R8: 22 kOhm
R9: 11 kOhm
D1: type 1N 4148
T1: type BC 558B
T2: BC 548B
Amplifier 12: (OP) IC of the type TL 071
C1: 1 µF
C2: 1 µF
C3: 0.47 µF

Figure 5 shows a modification of Figure 2 which works advantageously even if one of the two voltage values U1, U2 of the signal voltage US is not received over any length of time. For such a case, for example in the absence of U2 corresponding to 2100 Hz, the capacitor C2 is connected to the voltage source U5 through the transistor T7 which is controlled through T3 and T5, or, in the absence of U1 corresponding to 1300 Hz, the capacitor C1 is connected to the voltage source U4 through the transistor T8, controlled by T4 and T6. This connecting up is dependent on the particular voltage US present. If this voltage alternates between U1 and U2 in rapid succession, the capacitors C4 and C5 are charged by the one half-wave

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and discharged again through the diode D2 or D3 respectively immediately on the appearance of the other half wave. As a result, the transistors T2 and T4 remain blocked and the circuit operates as described in Figure 2. If there is no alternation in the control voltage US, that is to say if one of the two frequencies, for example f = 2100 Hz is absent in the intervals in transmission, in this case the capacitor C4 is positively charged as a recult of which the voltage U5 is applied to C2 through the E-C path of T7. This voltage U5 is produced by the voltage divider R8/R9 which is so designed that for example $\frac{1}{4}$ UB is applied to C2.

In the other case or in the absence of U1 = 1300 Hz, C5 is charged. As a result, the voltage U4, which is fixed at $\frac{3}{4}$ UB for example by the voltage divider R10/R11, is applied to C1.

The time constant for the connection of the stand-by voltage source to the capacitors is such that in the absence of one of the frequencies f1, f2, the voltage at the capacitors C1 or C2 can drop by 10% at the maximum before T2 or T8 is closed. This time constant is fixed by the dimensioning of the resistors R6 and R7 respectively and of the capacitors C4 and C5 respectively.

* C L M S *

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Claims

1. A decoder for a frequency-keyed signal (2), particularly an FSK view-data signal, having a PLL circuit consisting of a controllable oscillator (5) and a phase-comparison stage (3) from which a signal voltage (Us) varying between two values (U1, U2) is derived, which voltage is evaluated, in relation to a reference voltage (Uref), on the one hand for the generation of a control voltage (Ur) in a control-voltage generator circuit (11) for the automatic frequency control (AFC) of the oscillator (5) and on the other hand for the generation of an output signal (10) in an amplitude-selection circuit (7), characterised in that the two voltage values (U1, U2) of the signal voltage (Us) are stored in the control-voltage generator circuit (11), in two capacitors (C1, C2) connected to one another via a resistor network (R1, R2) and the voltage at a tap (d) of this network (R1, R2) is fed, together with the reference voltage (Uref), to a comparison stage (12) delivering the control voltage (Ur).

2. A decoder according to Claim 1, characterised in that the network consists of two equally large resistors (R1, R2).

3. A decoder according to Claims 1 and 2, characterised in that a terminal (a) carrying the signal voltage (Us) is connected to the bases of two complementary transistors (T1, T2) each in a collector-to-base circuit and in the emitter circuits of which, the two capacitors (C1, C2) are connected.

4. A decoder according to Claim 1, characterised in that a diode (D1) serving to limit the voltage is connected to one capacitor (C2).

* C L M S *

5. A decoder according to Claims 1, 2 and 3, characterised in that, in the absence of one of the two voltage values (U1, U2) of the signal voltage (Us) at the capacitors (C1, C2), means are provided whereby a stand-by voltage source (U4, U5) is connected in.

6. A decoder according to Claim 5, characterised in that the stand-by voltage source (U4, U5) corresponds to a voltage which trims the frequency of the generator (5) as if a voltage (U1, U2) were present.

7. A decoder according to Claim 6, characterised in that, in the absence of one of the two voltage values (U1, U2) of the signal voltage (US), the stand-by voltage source (U4, U5) is connected in with such a delay that a drop of the voltage appearing at the capacitors (C1, C2) by more than 10% is avoided.

8. A decoder according to Claim 1, characterised in that an active low-pass filter (R4, C3) with a critical frequency of the order of magnitude of 0.35 Hz is connected into the path of the control voltage (Ur).