

Claims

[Claim 1] A supporting glass substrate, comprising a polished surface on each of both surfaces thereof, and having a thickness of 0.3 mm or more and less than 2.0 mm and a total thickness variation of less than 5.0 μm .

[Claim 2] The supporting glass substrate according to claim 1, wherein the supporting glass substrate has a total thickness variation of less than 2.0 μm .

[Claim 3] The supporting glass substrate according to claim 1 or 2, wherein the supporting glass substrate has a warpage level of 60 μm or less.

[Claim 4] A supporting glass substrate, comprising a polished surface on each of both surfaces thereof, and having a thickness of 0.3 mm or more and less than 2.0 mm and a total thickness variation of less than 2.0 μm , wherein the supporting glass substrate is formed by an overflow down-draw method.

[Claim 5] The supporting glass substrate according to any one of claims 1 to 4, wherein the supporting glass substrate is used for supporting a processed substrate in a manufacturing process for a semiconductor package.

[Claim 6] The supporting glass substrate according to any one of claims 1 to 5, wherein the supporting glass substrate has a Young's modulus of 65 GPa or more.

[Claim 7] A laminate, comprising at least a processed substrate and a supporting glass substrate configured to support the processed substrate, the supporting glass substrate comprising the supporting glass substrate of any one of claims 1 to 6.

[Claim 8] The laminate according to claim 7, wherein the processed substrate comprises at least a semiconductor chip molded with a sealing material.

[Claim 9] A method of manufacturing a semiconductor package, comprising the steps of:

- preparing a laminate comprising at least a processed substrate and a supporting glass substrate configured to support the processed substrate;

- conveying the laminate; and

- subjecting the processed substrate to processing treatment, the supporting glass substrate comprising the supporting glass substrate of any one of claims 1 to 6.

[Claim 10] The method of manufacturing a semiconductor package according to claim 9, wherein the processing treatment comprises

a step of arranging wiring on one surface of the processed substrate.

[Claim 11] The method of manufacturing a semiconductor package according to claim 9 or 10, wherein the processing treatment comprises a step of forming a solder bump on one surface of the processed substrate.