

Description

The invention relates to a fault protection circuit in a power supply of, for example, a television apparatus and, in particular, to one that prevents an over-current condition in a power MOSFET transistor.

EP-A-0 255 067 shows a circuit of this art. Within this circuit a measuring device in form of a differential amplifier is disabled when a switching power transistor is non-conductive. However, the signal to be measured still contains the large peaks which occur when the switching power transistor is non-conductive. As a result, the measuring is not as accurate as would be desired.

ADC-to-DC converter, or chopper, used in, for example, a television apparatus power supply, may utilize a switching power transistor operating at a given frequency and having a first main current conducting electrode that is coupled to a first terminal of a primary winding of a transformer. A second terminal of the primary winding may be coupled to an input DC voltage that may be obtained from a battery or from a rectifier that rectifies an AC mains voltage. When the transistor is switched off, a voltage is induced in a secondary winding of the transformer. The induced voltage in the secondary winding is rectified for producing an output DC voltage that energizes a load circuit. The load circuit may be, for example, a deflection circuit of a television receiver.

It may be desirable to protect the power transistor against an over-current condition that may be destructive. Such over-current condition may be caused by, for example, an excessive loading condition in the secondary winding of the transformer.

In one prior art television circuit, a current level sampling resistor is coupled in series with the main current conducting electrodes of the power transistor. A voltage that is representative of the current flowing between the main current conducting electrodes is developed across the sampling resistor. A comparator, responsive to the voltage across the sampling resistor, generates an output signal when an over-current condition occurs. The over-current condition occurs when the current in the power transistor exceeds a predetermined threshold level that is considered a safe operating level. The comparator output signal is coupled to a drive circuitry of the power transistor to turn off the power transistor, thus preventing further conduction in the power transistor when the over-current condition is detected.

In high current applications, such sampling resistor, disadvantageously, may dissipate considerable power. Hence, the efficiency of the converter is reduced. Therefore, it may be desirable to sense the current in the power transistor without interposing such sampling resistor in series with the power transistor.

In a circuit embodying a feature of the invention,

the power transistor is, for example, of the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) type. The source electrode is grounded and the drain electrode is coupled to the primary winding of the aforementioned transformer. The voltage that is developed between the drain electrode and ground is proportional to the current in the MOSFET during its conduction. Therefore, such voltage is indicative of the level of the current that flows in the MOSFET during conduction. Such voltage is used for generating an over-current protection signal, embodying an aspect of the invention.

On the other hand, the voltage between the drain electrode and ground, when the MOSFET is nonconductive, may be substantially higher and may not be indicative of the current that flows during the conduction time of the MOSFET transistor. It may be desirable to prevent that voltage from affecting the over-current protection signal.

In accordance with an aspect of the invention, the voltage that is developed at, for example, the drain electrode, is used for generating a first portion of a first signal, embodying a feature of the invention. The voltage at the drain electrode may be referred to as the voltage that is developed across the "on" resistance of the MOSFET. When the MOSFET is conductive, the level of the first portion of the first signal varies proportionally as the voltage at the drain electrode. The level of the first portion of the first signal is indicative of the current in the transistor. When the MOSFET is nonconductive, a second portion of the first signal is established at, or clamped to a constant level such as, for example, zero volts. In this way, an amplitude of the first signal is, advantageously, indicative of the current in the transistor but is unaffected by the voltage at the drain electrode when the transistor is nonconductive.

The first signal is coupled to a current sensing arrangement that may include a comparator. When a magnitude of the first signal exceeds a predetermined level, indicative of an over-current condition, the current sensing arrangement generates a control signal that is coupled to the gate electrode of the MOSFET, causing it to turn off. In this way, the MOSFET is advantageously protected against a potentially destructive over-current condition. In one embodiment of the invention, a second transistor is used for clamping the first signal to the zero volt level when the MOSFET power switch is nonconductive.

A fault detection and protection apparatus, embodying an aspect of the invention, in a switching power supply includes a source of an input supply voltage and a first switching power transistor having first and second main current conduction electrodes and a control electrode. The apparatus includes a source of a first control signal at a given frequency that is coupled to the control electrode of the first switching power transistor. The first control signal causes, dur-

ing normal operation, the first switching transistor to operate at a switching frequency determined in accordance with the given frequency. A utilization circuit of the apparatus includes an impedance coupled to the input supply voltage and to the first main current conducting electrode for developing an output supply voltage in the utilization circuit. The impedance forms a current path to a switched main current that flows in the first switching power transistor. A first current sensing signal is developed at a frequency determined in accordance with the given frequency between the first and second main current conducting electrodes of the first switching power transistor when the first switching power transistor is conductive. The first current sensing signal is indicative of a level of the main current when the first switching power transistor is conductive. A first portion of a second current sensing signal that is indicative of the level of the main current is generated at an output terminal, in accordance with the first control signal and in accordance with the first current sensing signal, when the first switching power transistor is at a conductive state. The output terminal is decoupled from the power transistor when the first switching power transistor is at a nonconductive state to prevent a voltage that is developed at the first main current conducting electrode of the first switching power transistor when the power transistor is nonconductive, from having a substantial contribution to an amplitude of the second current sensing signal. A second control signal is generated when a magnitude of the first portion of the second current sensing signal is outside a normal operation range, indicating an occurrence of a fault condition in the power supply. The second control signal is coupled to the control electrode of the first switching power transistor for preventing the first switching power transistor from further conducting.

In the Drawing:

FIGURE 1 illustrates a first embodiment of an over-current protection circuit, embodying an aspect of the invention;

FIGURES 2a-2d illustrate waveforms useful in explaining the operation of the circuit of FIGURE 1;

FIGURE 3 illustrates a second embodiment of an over-current protection circuit, embodying another aspect of the invention;

FIGURES 4a-4d illustrate waveforms useful for explaining the operation of the circuit of FIGURE 3; and

FIGURE 5 illustrates a third embodiment of an over-current protection circuit embodying a further aspect of the invention that is utilized in a push-pull output stage.

FIGURE 1 illustrates a DC-to-DC converter, or chopper arrangement 100 of a television apparatus that includes an over-current protection arrangement 100a, embodying an aspect of the invention. FIG-

URES 2a-2d illustrate waveforms useful for explaining the operation of arrangement 100 of FIGURE 1. Similar numbers and symbols in FIGURES 1 and 2a-2d indicate similar items or functions.

Arrangement 100 of FIGURE 1 includes an oscillator and driver stage 50 that generates a square wave signal V_G at a given frequency during normal operation, as shown in FIGURE 2a. During normal operation, signal V_G of FIGURE 1 causes a MOSFET Q_1 to switch on and off, alternately, at the switching frequency that is determined by that of signal V_G . A primary winding T_{1a} of a chopper transformer T_1 has a first terminal that is coupled to a drain electrode of transistor Q_1 and a second terminal that is coupled to a DC input voltage $B+$. The switching operation of transistor Q_1 causes a voltage to be induced in a secondary winding T_{1b} of transformer T_1 . Such voltage is rectified by a rectifier arrangement 60 comprising a diode D_1 and a capacitor C_1 . Rectifier arrangement 60 produces a DC output voltage V_{RL} across a load, such as a resistor R_L . Resistor R_L is representative of the load formed by circuitry of the television apparatus, not further illustrated in FIGURE 1, that is energized by voltage V_{RL} .

As a result of the conduction of transistor Q_1 , a ramping current I_1 flows in winding T_{1a} , as shown in FIGURE 2b. The dashed lines in FIGURES 2b-2d correspond to a first example in which current I_1 is larger than in a second example, shown by a solid line.

During, for example, interval t_1 - t_2 of FIGURE 2c, current I_1 of FIGURE 1 develops an upramping voltage V_{Q1} at the drain of transistor Q_1 , that is proportional to current I_1 . Voltage V_{Q1} is equal to the magnitude of current I_1 multiplied by r_{DS} , where r_{DS} denotes the value of the "on" or forward resistance of transistor Q_1 when transistor Q_1 is fully turned-on. When transistor Q_1 is nonconductive, such as during interval t_2 - t_1' of FIGURE 2c, voltage V_{Q1} of FIGURE 1 is, as a result of transformer operation of transformer T_1 , more positive than voltage $B+$. During interval t_1 - t_2 , for example, voltage V_{Q1} of FIGURE 2c is indicative of the magnitude of current I_1 of FIGURE 1. During interval t_2 - t_1' of FIGURE 2c, voltage V_{Q1} includes a portion that is not readily representative of current I_1 in transistor Q_1 of FIGURE 1.

In accordance with an aspect of the invention, a current sensing signal V_{Q2} is generated from voltage V_{Q1} that is proportional to current I_1 when transistor Q_1 is conductive, and that is, for example, zero when transistor Q_1 is nonconductive. Therefore, signal V_{Q2} is, advantageously, unaffected by voltage V_{Q1} , during the "off" time of transistor Q_1 . In this way, an amplitude of signal V_{Q2} , such as, for example, its peak-to-peak amplitude, is proportional to current I_1 that occurs during the "on" time of transistor Q_1 . Such feature of signal V_{Q2} is advantageous in that it simplifies further processing of signal V_{Q2} because signal V_{Q2} is unaffected by voltage V_{Q1} when transistor Q_1 is non-

conductive. Such processing of signal V_{Q2} may include, for example, low-pass filtering signal V_Q to reduce noise or averaging signal V_{Q2} to form a signal that is indicative of the average value or of the peak value of current i_1 of FIGURE 1.

To generate signal V_{Q2} , the drain electrode of transistor Q_1 is coupled through a resistor R_1 to a drain electrode Q_{2a} of a JFET (Junction Field Effect Transistor) Q_2 operating as a shunt switch. The gate electrode of transistor Q_2 is coupled to signal V_G . Transistors Q_1 and Q_2 operate in a complementary manner; when one is conductive, the other is not, and vice versa.

Signal V_{Q2} , embodying an aspect of the invention and developed at electrode Q_{2a} , as shown in FIGURE 2d, is equal, during interval t_1 - t_2 , to voltage V_{Q1} of FIGURE 2c. During interval t_2 - t_1' , for example, that occurs when transistor Q_1 is nonconductive, voltage V_{Q1} may not be readily representative of current i_1 of FIGURE 1. During interval t_2 - t_1' , signal V_{Q2} of FIGURE 2d is clamped to approximately zero volts the "on" resistance of conductive JFET transistor Q_2 of FIGURE 1. Therefore, the contribution of voltage V_{Q1} to signal V_{Q2} when transistor Q_1 is conductive is substantially larger than when transistor Q_1 is nonconductive. Therefore, advantageously, a change in current i_1 will cause, proportionally, a larger change in, for example, the peak amplitude or the average of signal V_{Q2} than if signal V_{Q2} were not so clamped. The result is an over-current detection arrangement that is more sensitive to variations in current i_1 . It should be understood that resistor R_1 and transistor Q_2 form a controllable attenuator having a very high or infinite attenuation factor that attenuates mainly when transistor Q_1 is nonconductive and that couples, for example, unattenuated voltage V_{Q1} to form signal V_{Q2} , when transistor Q_1 is conductive.

Advantageously, signal V_{Q2} of FIGURE 2d is an analog signal. As an analog signal, signal V_{Q2} is capable of assuming any value from a range including infinite distinct values when current i_1 assumes any value from a corresponding range of values. In contrast, a digital signal may assume only a finite number of values. Being an analog signal, signal V_{Q2} of FIGURE 1 may be, advantageously, readily low-pass filtered in a conventional low-pass filter for obtaining a filtered current sensing signal, not shown in the FIGURES, that is coupled to current sensing arrangement 51. Note that if voltage V_{Q1} were low-pass filtered directly, its amplitude would not be readily representative of current i_1 . This is so, because the portion of voltage V_{Q1} when transistor Q_1 is nonconductive may not be necessarily related to current i_1 in magnitude. Such portion may be much larger than the other portion of voltage V_{Q1} when transistor Q_1 is conductive that makes the process of extracting information of current i_1 more difficult.

Signal V_{Q2} is coupled to an input terminal 51a of

current sensing arrangement 51 that may include the aforementioned low-pass filter. An over-current condition may occur when current i_1 of FIGURE 2b exceeds a predetermined level that is considered a safe operating level. When such over-current condition occurs, the peak or the average value signal V_{Q2} becomes larger than a corresponding predetermined reference voltage level. Consequently, current sensing arrangement 51 of FIGURE 1, that may include a comparator, generates an over current protection signal INHIBIT that is coupled to a control terminal 50a of oscillator and driver 50. Signal INHIBIT causes signal V_G to be maintained at, for example, zero volts, that forces transistor Q_1 to remain nonconductive. Current i_1 of FIGURE 1 becomes zero, thereby protecting transistor Q_1 from the aforementioned over-current condition. The clamping operation of transistor Q_2 , advantageously, simplifies the manner by which information regarding the magnitude of current i_1 is obtained from voltage V_{Q1} for producing signal INHIBIT.

FIGURE 3 illustrates a power supply arrangement 100', embodying another aspect of the invention, that is similar to arrangement 100 of FIGURE 1. In particular, the magnitude of the current in each MOSFET transistor, Q_1 and Q_1' of FIGURES 1 and 3, respectively, is obtained from a voltage that is developed between the corresponding drain and source electrodes when the respective transistor is on. Similar numbers and symbols in FIGURES 1 and 3 indicate similar items or functions.

A signal $V_{G'}$ of FIGURE 3 that is analogous to signal V_G of FIGURE 1 contains information of the magnitude of a current i_1' . FIGURES 4a-4d illustrate waveforms useful for explaining the operation of arrangement 100' of FIGURE 3. Similar numbers and symbols in FIGURES 3 and 4a-4d indicate similar items or functions.

In arrangement 100' of FIGURE 3, a signal $V_{G'}$ that controls the switching operation of transistor Q_1' is coupled to an anode electrode of a diode D_2' via a resistor R_2' . Diode D_2' , operating as a series coupled switch, has a cathode electrode that is coupled to the drain electrode of transistor Q_1' . Signal $V_{G'}$ supplies a small forward biasing current through diode D_2' at the same time that signal $V_{G'}$ causes transistor Q_1' to turn on. Consequently, signal $V_{G'}$ is proportional to current i_1' . Signal $V_{G'}$ is developed at a terminal 51a' that is coupled at a junction between resistor R_2' and the anode of diode D_1' . Signal $V_{G'}$ is equal, during interval t_a - t_b of FIGURE 4d, to the magnitude of current i_1' multiplied by resistance $r_{DS'}$ plus the level of voltage $V_{D2'}$. Voltage $V_{D2'}$ is the forward voltage drop across diode D_2' of FIGURE 3 that is approximately equal to 0.7 volts.

When signal $V_{G'}$ is zero, such as, for example, during interval t_b - t_c of FIGURE 4a, occurring when transistor Q_1 is nonconductive, the current in resistor

R_2' of FIGURE 3 is zero and diode D_2' is back biased. The nonconductive diode D_2' advantageously isolates input terminal 51a' from voltage V_{Q1}' . When diode D_2 is nonconductive, voltage V_{Q1} is higher than voltage B+. Thus, during, for example, interval t_b - t_c of FIGURE 4d, signal V_s' is maintained at approximately zero volts.

When signal V_G' of FIGURE 3, due to some fault condition, is too small, or when the magnitude of current i_1' is excessive, protection signal INHIBIT' of current sensing arrangement 51' is generated. Signal INHIBIT', advantageously, prevents transistor Q_1' from being turned on.

In some switched mode power supply applications it may be desirable to increase the frequency of signal V_G' when current i_1' increases so as to increase the range of regulation of the DC output voltage in the face of corresponding variations in current i_1 and in voltage B+. Advantageously, signal V_s' may also be coupled, as shown in FIGURE 3 by a dashed line, to a frequency controlling terminal 50b' of oscillator and driver 50' to increase, for example, the frequency of signal V_G' when the magnitude current i_1' increases, and vice versa.

FIGURE 5 illustrates a converter 100" embodying a further aspect of the invention. Converter 100", that includes a push-pull stage, generates a 24 volt output voltage V_{24} by DC-to-DC converting a 12 volt battery input voltage V_B . Converter 100" of FIGURE 5 may be used in, for example, a portable color television receiver having a ten inch picture tube of the type 250ATB22, made by Hitachi Co., and not shown in the figures. Additionally, converter 100" of FIGURE 5 may provide a 15 volt standby supply voltage V_{SB} and a 220 volt supply voltage V_{DG} . Voltage V_{DG} may be used for energizing a resonant degaussing circuit, not shown in the figures.

In converter 100", the drain electrodes of MOS-FET'S Q_{10} and Q_{20} are coupled to end terminals 90 and 91, respectively, of a primary windin T_{10a} of a chopper transformer T_{10} . A terminal 92 of windin T_{10a} , located intermediate terminals 90 and 91, is coupled to battery voltage V_B . An oscillator U_1 generates signals at opposite phases that are coupled via a drive circuit U_2 to form oppositely phased signals V_{2a} and V_{2b} , respectively. Signals V_{2a} and V_{2b} coupled, respectively, to the gate electrodes of transistors Q_{10} and Q_{20} , via resistors R_3 and R_4 , cause transistors Q_{10} and Q_{20} to operate in a push-pull manner.

A drain current i_{10} of transistor Q_{10} is sampled by a diode D_{20} in a manner that is analogous to that done by diode D_2' of FIGURE 3. Consequently, a voltage V_{S10} of FIGURE 5 is formed in a similar manner to the way signal V_s' of FIGURE 3 is formed. Similarly, a drain current i_{20} of transistor Q_{20} of FIGURE 5 is sampled by a diode D_{30} to form a voltage V_{S20} . Voltages V_{S10} and V_{S20} , that are alternately developed, are applied to respective resistors R_6 and R_7 . Consequently,

a signal V_{SUM} at a junction terminal A of resistors R_6 and R_7 is formed. Signal V_{SUM} is developed across a resistor R_{18} and an integrating capacitor C_6 , and coupled to an inverting input terminal of a comparator U_{3C} . Diode D_{20} , for example, prevents voltage V_{S0} across transistor Q_{10} from affecting signal V_{SUM} when transistor Q_{10} is nonconductive.

Should a fault condition occur that causes either of currents i_{10} and i_{20} to exceed a predetermined level, signal V_{SUM} will exceed a reference voltage V_{RF} , developed across a diode D_6 at a noninverting input terminal of comparator U_{3C} . Consequently, a signal V_0 will be generated at an output terminal of comparator U_{3C} . Signal V_0 is coupled via a noninverting input terminal of a comparator U_{3B} having an output terminal that feeds an inverting input terminal of a comparator U_{3A} . As a result Signal V_0 occurs when signal V_{SUM} is greater than reference voltage V_{RF} . When signal V_0 is generated, a signal INHIBIT at a first or HIGH, logic level is generated at an output terminal of comparator U_{3A} . Signal INHIBIT at the first logic level causes the output signals of oscillator U_1 to remain at zero volts. The result is that each of signals V_{2a} and V_{2b} becomes zero. Therefore, the switching operation in transistors Q_{10} and Q_{20} ceases and transistors Q_{10} and Q_{20} are prevented from being turned on. Therefore, signal V_{SUM} becomes zero and signal V_0 returns to its normal operation level.

Comparator U_{3B} operates as a time-out timer. Once its output signal V_{3BOUT} changes, signal V_{3BOUT} is prevented from immediately returning to its normal operation level. Signal V_{3BOUT} is so prevented until a shut-down period of, illustratively, 150 milliseconds has elapsed from the time signal V_0 returns to its normal operation level. The 150 millisecond minimum delay is determined by the time constant that is associated with a capacitor C_6 , coupled to an inverting input terminal of comparator U_{3B} , as described below.

During normal operation of converter 100", signal V_{SUM} is smaller than voltage V_{RF} . An output terminal of comparator U_{3C} , pin number 13, represents a high impedance that is formed at an open collector transistor, not shown in the figures. An output terminal of comparator U_{3B} , pin number 14, also represents a high impedance. Capacitor C_6 is charged to a voltage that is determined by resistors R_{15} , R_{14} , R_{13} and R_{16} that form a voltage divider.

When signal INHIBIT at the output terminal of comparator U_{3A} is low, signal INHIBIT enables oscillator U_1 . When an overload condition occurs, signal V_{SUM} increases above the level of voltage V_{RF} and triggers comparators U_{3C} and U_{3B} . Their output terminals switch to the LOW state that is approximately at ground potential and drive comparator U_{3A} output signal INHIBIT to the HIGH state level which disables oscillator U_1 . As a result of converter 100" being disabled, signal V_{SUM} decreases to a value that is below that of voltage V_{RF} and comparator U_{3C} output termi-

nal switches to a high impedance. Because of the feedback provided by resistor R_{13} , comparator U_{3B} output signal V_{3BOUT} remains at the LOW state until capacitor C_5 discharges through resistor R_{14} to a voltage that is lower than the voltage of signal V_0 . Signal V_0 is developed at the noninverting input terminal of comparator U_{3B} . Consequently, comparator U_{3B} output terminal switches to the high impedance and capacitor C_5 begins charging via resistors R_{16} , R_{13} and R_{14} . When the voltage at the inverting input terminal of comparator U_{3A} , pin number 6, has increased above the voltage at the noninverting input terminal, pin number 7, comparator U_{3A} output signal INHIBIT switches to the LOW state and again enables oscillator U_1 . Therefore, the generation of signals V_{2a} and V_{2b} is resumed.

The time interval between the triggering that is caused by signal V_{SUM} and the time that the switching operation of transistors Q_{10} and Q_{20} ceases is, advantageously, very short, approximately 1 microsecond. After the switching operation in transistors Q_{10} and Q_{20} stops, the switching operation, cannot immediately resume, as indicated before. The resumption of the switching operation may occur, at the earliest, after the 150 millisecond shut-down period has elapsed, as described before. Thus, transistors Q_{10} and Q_{20} can recover or cool down from the over-current condition before they can be turned on again.

In the circuit of FIGURE 5, the triggering level occurs when signal V_{SUM} exceeds approximately 0.7 volts that is determined by the forward voltage of diode D_6 . Such level corresponds to voltages V_{90} and V_{91} each being at approximately 0.8 volts. In each of MOSFET'S Q_{10} and Q_{20} of FIGURE 5, the "on" resistance that occurs when the transistor is fully turned on may be approximately 0.12 ohms. Thus, shut-down of converter 100" occurs when the current I_{10} or I_{20} exceeds approximately 6.5 amperes. The protection threshold voltage or current may be controlled by changing the value of resistor R_{18} .

Voltage comparator U_{3A} receives, via its noninverting input terminal, a reference voltage developed in a zener diode D_{16} . When battery voltage V_B falls below, for example, 11 volts, signal INHIBIT is generated because signal U_{3BOUT} at the inverting input terminal of comparator U_{3A} becomes smaller than the voltage at the noninverting input terminal V_{REF} . Therefore, the switching operation of transistors Q_{10} and Q_{20} ceases. Consequently, further discharge of the battery is prevented.

The positive portions of voltages V_{90} and V_{91} are coupled to a charge storage capacitor C_{10} via diodes D_4 and D_5 , respectively. Capacitor C_{10} is thereby charged to approximately 24 volts. A voltage that is developed across a secondary winding T_{10b} of transformer T_{10} is rectified and doubled in a voltage doubler 66 comprising a capacitor C_{12} , a diode D_8 , a diode D_7 and a capacitor C_{13} . Voltage doubler 66 produces

a voltage V_{DG} that may be used as the supply voltage in a resonant degaussing circuit, not illustrated.

Voltage V_{DG} is also coupled to the gate of a MOSFET Q_{30} to turn on the transistor. Capacitor C_{10} is coupled via MOSFET Q_{30} to a terminal 77 to develop voltage V_{24} at terminal 77 when the switching operation is normal. When the switching operation ceases, as a result of, for example, an over-current condition, transistor Q_{30} becomes immediately nonconductive. When transistor Q_{30} becomes nonconductive, the transistor isolates terminal 77 from storage capacitor C_{10} . In this way, transistor Q_{30} , advantageously, immediately decouples power to the load.

Claims

1. Fault detection and protection apparatus in a switching power supply, comprising:
 - a source of an input supply voltage (B+);
 - a first switching power transistor (Q1) having first (D) and second (S) main current conducting electrodes and a control electrode (G);
 - a source (50) of a first control signal (VG) at a given frequency that is coupled to said control electrode of said first switching power transistor (Q1) for causing, during normal operation, said first switching transistor (Q1) to operate at a switching frequency determined in accordance with said given frequency;
 - a utilization circuit (T₁) including an impedance (T_{1a}) coupled to said input supply voltage and to said first main current conducting electrode for developing an output supply voltage (VRL) in said utilization circuit, whereby said impedance (T_{1a}) forming a current path to a switched main current (I_l) that flows in said first switching power transistor (Q1) to develop a first current sensing signal (VQ1) at a frequency determined in accordance with said given frequency, and that is developed between said first (D) and second (S) main current conducting electrodes of said first switching power transistor (Q1) when said first switching power transistor (Q1) is conductive, said first current sensing signal (VQ1) being indicative of a level of said main current when said first switching power transistor (Q1) is conductive;
 - characterized by
 - first means (Q2) responsive to said first control signal (VG) and to said first current sensing signal (VQ1) and having resistor (R1) that is coupled to said first main current conducting electrode (D) for generating at an output terminal (Q2a) a first portion of a second current sensing signal (VQ2) that is indicative of said level of said main current (I_l) when said first switching power transistor (Q1) is at a conductive state, and for decoupling

nal switches to a high impedance. Because of the feedback provided by resistor R_{13} , comparator U_{3B} output signal V_{3BOUT} remains at the LOW state until capacitor C_5 discharges through resistor R_{14} to a voltage that is lower than the voltage of signal V_0 . Signal V_0 is developed at the noninverting input terminal of comparator U_{3B} . Consequently, comparator U_{3B} output terminal switches to the high impedance and capacitor C_5 begins charging via resistors R_{16} , R_{13} and R_{14} . When the voltage at the inverting input terminal of comparator U_{3A} , pin number 6, has increased above the voltage at the noninverting input terminal, pin number 7, comparator U_{3A} output signal INHIBIT switches to the LOW state and again enables oscillator U_1 . Therefore, the generation of signals V_{2a} and V_{2b} is resumed.

The time interval between the triggering that is caused by signal V_{SUM} and the time that the switching operation of transistors Q_{10} and Q_{20} ceases is, advantageously, very short, approximately 1 microsecond. After the switching operation in transistors Q_{10} and Q_{20} stops, the switching operation, cannot immediately resume, as indicated before. The resumption of the switching operation may occur, at the earliest, after the 150 millisecond shut-down period has elapsed, as described before. Thus, transistors Q_{10} and Q_{20} can recover or cool down from the over-current condition before they can be turned on again.

In the circuit of FIGURE 5, the triggering level occurs when signal V_{SUM} exceeds approximately 0.7 volts that is determined by the forward voltage of diode D_6 . Such level corresponds to voltages V_{90} and V_{91} each being at approximately 0.8 volts. In each of MOSFET'S Q_{10} and Q_{20} of FIGURE 5, the "on" resistance that occurs when the transistor is fully turned on may be approximately 0.12 ohms. Thus, shut-down of converter 100" occurs when the current I_{10} or I_{20} exceeds approximately 6.5 amperes. The protection threshold voltage or current may be controlled by changing the value of resistor R_{18} .

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The positive portions of voltages V_{90} and V_{91} are coupled to a charge storage capacitor C_{10} via diodes D_4 and D_6 , respectively. Capacitor C_{10} is thereby charged to approximately 24 volts. A voltage that is developed across a secondary winding T_{10b} of transformer T_{10} is rectified and doubled in a voltage doubler 66 comprising a capacitor C_{12} , a diode D_8 , a diode D_7 and a capacitor C_{13} . Voltage doubler 66 produces

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Claims

1. Fault detection and protection apparatus in a switching power supply, comprising:
 - a source of an input supply voltage (B+);
 - a first switching power transistor (Q1) having first (D) and second (S) main current conducting electrodes and a control electrode (G);
 - a source (50) of a first control signal (VG) at a given frequency that is coupled to said control electrode of said first switching power transistor (Q1) for causing, during normal operation, said first switching transistor (Q1) to operate at a switching frequency determined in accordance with said given frequency;
 - a utilization circuit (T₁) including an impedance (T_{1a}) coupled to said input supply voltage and to said first main current conducting electrode for developing an output supply voltage (VRL) in said utilization circuit, whereby
 - said impedance (T_{1a}) forming a current path to a switched main current (i1) that flows in said first switching power transistor (Q1) to develop a first current sensing signal (VQ1) at a frequency determined in accordance with said given frequency, and that is developed between said first (D) and second (S) main current conducting electrodes of said first switching power transistor (Q1) when said first switching power transistor (Q1) is conductive, said first current sensing signal (VQ1) being indicative of a level of said main current when said first switching power transistor (Q1) is conductive;
 - characterized by
 - first means (Q2) responsive to said first control signal (VG) and to said first current sensing signal (VQ1) and having resistor (R1) that is coupled to said first main current conducting electrode (D) for generating at an output terminal (Q2a) a first portion of a second current sensing signal (VQ2) that is indicative of said level of said main current (i1) when said first switching power transistor (Q1) is at a conductive state, and for decoupling



said output terminal (Q2a) from said power transistor (Q1) when said first switching power transistor (Q1) is at a non-conductive state to prevent a voltage (VQ1) that is developed at said first main current conducting electrode (D) of said first switching power transistor (Q1) when said power transistor is non-conductive from having a substantial contribution to an amplitude of said second current sensing signal (VQ2); and second means (51) responsive to said second current sensing signal (VQ2) for generating a second control signal (INHIBIT), when a magnitude of said first portion of said second current sensing signal (VQ2) is outside a normal operation range indicating an occurrence of a fault condition in said power supply, said second control signal (INHIBIT) being coupled to said source (50) of said first control signal (VG) controlling control said first switching power transistor (Q1) for preventing said first switching power transistor (Q1) from further conducting.

2. Apparatus according to claim 1, characterized in that said first means comprises a second switching transistor (Q2) having a control electrode that is coupled to said first control signal (VG) and a main current conducting electrode that is coupled via said resistor (R1) to said first main current conducting electrode (D) of said first switching power transistor (Q1) for developing said second current sensing signal (VQ2) at said main current conducting electrode of said second switching transistor (Q2) such that when said first switching power transistor (Q1) is conductive said second switching transistor (Q2) is non-conductive, and vice versa.
3. Apparatus according to claim 1, characterized in that said first means (Q2) operates at a frequency that is related to that of said first control signal (VG) and wherein, when said first switching power transistor (Q1) is non-conductive, said first means (Q2) causes said second current sensing signal (VQ2) to be at a predetermined constant level that is substantially lower than of said first portion of said second current sensing signal (VQ2).
4. An apparatus according to Claim 1, characterized in that said first means comprises a diode (D2') having a first terminal that is coupled to said first main current conducting electrode (D) of said first switching power transistor (Q1) for developing said second current sensing signal (VD2') at a second terminal of said diode (D2') such that, when said first switching power transistor (Q1') is conductive, said diode (D2') is forward biased, and when said first switching power transistor

(Q1) is non-conductive, said first current sensing signal (VQ1') that is developed at said first main current conducting electrode (D) of said first switching power transistor (Q1') back biases said diode (D2') to decouple said first main current conducting electrode (D) of said first switching power transistor (Q1') from said second terminal (anode) of said diode (D2').

5. An apparatus according to Claim 1, characterized in that said impedance comprises, a first transformer winding (T10a) having a first terminal (90) that is coupled to said first main current conducting electrode (D) of said first switching power transistor (Q10), a second switching power transistor (Q20) having a first main current conducting electrode (D) that is coupled to a second terminal (91) of said first transformer winding (T10a) that is remote from said first switching power transistor (Q10) for conducting a second switching current in said second switching power transistor (Q20) and having a control electrode that is responsive to a control signal (V2b) at a frequency that is related to that of said first control signal (V2a) such that said first (Q10) and second (Q20) switching power transistors operate in a push-pull manner, and wherein said second means (51) is coupled to said first main current conducting electrodes (D) of said first (Q10) and second (Q20) switching power transistors for generating said second current sensing signal (VSUM) that is indicative of an overcurrent condition in either one of said first (Q10) and second (Q20) switching power transistors.
6. An apparatus according to Claim 5, characterized in that said second means comprises first (D20) and second (D30) diodes, said first diode (D20) having a first terminal that is coupled to said first main current conducting electrode (D) of said first switching power transistor (Q10) and said second diode (D30) having a first terminal that is coupled to said first main current conducting electrode (D) of said second switching power transistor (Q20) and combining means (R6, R7) coupled to said diodes (D20, D30) for developing said second current sensing signal (VSUM) in accordance with a signal (VS10) that is developed at a second terminal of said first diode (D20) and in accordance with a signal (VS20) that is developed at a second terminal of said second diode (D30).
7. An apparatus according to Claim 5, characterized by a rectifier arrangement (D4, D5) coupled to said first winding (T10a) for generating a first DC output voltage (VDG) in a capacitor (C10) and a switching third means (D30) responsive to a sig-



nal that is developed at a second winding (T10b) of said transformer (T10) for coupling said first DC output voltage to an output terminal (77) of said third means (Q30) during normal operation and for fast decoupling said output terminal (77) from said capacitor (C10) when a fault condition occurs.

8. An apparatus according to Claim 1, characterized by a delay means (U3b) responsive to said second current sensing signal (VSUM) for generating a signal (V3BOUT) that enables resumption of the switching operation in said first switching power transistor (Q10) only after a period having at least a predetermined length has elapsed following the occurrence of said second control signal (INHIBIT) that is sufficient to prevent harm to said first switching power transistor (Q10).

Patentansprüche

1. Fehlerfeststellungs- und -schutzvorrichtung in einem Schaltnetzteil, umfassend:
eine Quelle einer Eingangsversorgungsspannung (B+);
einen ersten Schalteistungstransistor (Q1) mit einer ersten (D) und einer zweiten (S) den Hauptstrom leitenden Elektrode und einer Steuerelektrode (G);
eine Quelle (50) eines ersten Steuersignales (VG) mit einer gegebenen Frequenz, das an der Steuerelektrode des ersten Schalteistungstransistors (Q1) anliegt, um im normalen Betrieb den ersten Schalttransistor (Q1) dazu zu veranlassen, mit einer Schaltfrequenz zu arbeiten, die in Übereinstimmung mit der gegebenen Frequenz bestimmt ist;
eine Anwendungsschaltung T₁, die eine Impedanz T_{1a} enthält, die mit der Eingangsversorgungsspannung und der ersten den Hauptstrom leitenden Elektrode verbunden ist, um eine Ausgangsversorgungsspannung (VRL) in der Anwendungsschaltung zu erzeugen, wobei die Impedanz (T_{1a}) einen Stromweg zu einem geschalteten Hauptstrom (i₁) bildet, der im ersten Schalteistungstransistor (Q1) fließt, um ein erstes Stromabtastsignal (VQ1) mit einer Frequenz zu bilden, die in Übereinstimmung mit der gegebenen Frequenz bestimmt wird, und die zwischen der ersten (D) und der zweiten (S) den Hauptstrom leitenden Elektrode des ersten Schalteistungstransistors (Q1) erzeugt wird, wenn der erste Schalteistungstransistor (Q1) leitet, wobei das erste Stromabtastsignal (VQ1) die Stärke des Hauptstromes anzeigt, wenn der erste Schalteistungstransistor (Q1) leitet;
gekennzeichnet durch

ein erstes Mittel (Q2), das auf das erste Steuersignal (VG) und das erste Stromabtastsignal (VQ1) reagiert und über einen Widerstand (R1) verfügt, der mit der ersten den Hauptstrom leitenden Elektrode (D) verbunden ist, um an einem Ausgang (Q2a) einen ersten Teil eines zweiten Stromabtastsignales (VQ2) zu erzeugen, das die Stärke des Hauptstromes (i₁) anzeigt, wenn der erste Schalteistungstransistor (Q1) leitet, und um den Ausgang (Q2a) vom Leistungstransistor (Q1) zu trennen, wenn der erste Schalteistungstransistor (Q1) sperrt, um eine Spannung (VQ1), die an der ersten den Hauptstrom leitenden Elektrode (D) des ersten Schalteistungstransistors (Q1) entsteht, wenn der Leistungstransistor sperrt, daran zu hindern, einen wesentlichen Anteil an einer Amplitude des zweiten Stromabtastsignales (VQ2) zu haben;

und ein zweites Mittel (51), das auf das zweite Stromabtastsignal (VQ2) reagiert, um ein zweites Steuersignal (INHIBIT) zu erzeugen, wenn sich eine Größe des ersten Teiles des zweiten Stromabtastsignales (VQ2) außerhalb eines normalen Betriebsbereiches befindet, was das Auftreten eines Fehlers im Netzteil anzeigt, wobei das zweite Steuersignal (INHIBIT) mit der Quelle (50) des ersten Steuersignales (VG) verbunden ist, das den ersten Schalteistungstransistor derart steuert, daß der erste Schalteistungstransistor (Q1) an weiterem Leiten gehindert wird.

2. Vorrichtung nach Patentanspruch 1, dadurch gekennzeichnet, daß das erste Mittel einen zweiten Schalttransistor (Q2) enthält, der eine Steuerelektrode aufweist, die mit dem ersten Steuersignal (VG) verbunden ist, und eine den Hauptstrom leitende Elektrode, die über den Widerstand (R1) mit der ersten den Hauptstrom leitenden Elektrode (D) des ersten Schalteistungstransistors (Q1) zur Erzeugung des zweiten Stromabtastsignales (VQ2) an der den Hauptstrom leitenden Elektrode des zweiten Schalttransistors (Q2) verbunden ist, so daß der zweite Schalttransistor (Q2) sperrt, wenn der erste Schalteistungstransistor (Q1) leitet, und umgekehrt.
3. Vorrichtung nach Patentanspruch 1, dadurch gekennzeichnet, daß das erste Mittel (Q2) mit einer Frequenz arbeitet, die mit der des ersten Steuersignales (VG) in Beziehung steht, und wobei das erste Mittel (Q2) bewirkt, daß das zweite Stromabtastsignal (VQ2) auf einem vorbestimmtem konstanten Wert verharrt, der wesentlich niedriger ist, als der des ersten Teiles des zweiten Stromabtastsignales (VQ2), wenn der erste Schalteistungstransistor (Q1) sperrt.



4. Vorrichtung nach Patentanspruch 1, dadurch gekennzeichnet, daß das erste Mittel eine Diode (D2') umfaßt, die einen ersten Anschluß aufweist, der mit der ersten den Hauptstrom leitenden Elektrode (D) des ersten Schalteistungstransistors (Q1) verbunden ist, um das zweite Stromabtastsignal (VD2') an einem zweiten Anschluß der Diode (D2') zu bilden, derart, daß die Diode (D2') in Durchlaßrichtung vorgespannt ist, wenn der erste Schalteistungstransistor (Q1') leitet, und daß das erste Stromabtastsignal (VQ1'), das an der ersten, den Hauptstrom leitenden Elektrode (D) des ersten Schalteistungstransistors (Q1') entsteht, die Diode (D2') in Sperrrichtung vorspannt, wenn der erste Schalteistungstransistor (Q1) sperrt, um die erste den Hauptstrom leitende Elektrode (D) des ersten Schalteistungstransistors (Q1') vom zweiten Anschluß (Anode) der Diode (D2') zu trennen.

5. Vorrichtung nach Patentanspruch 1, dadurch gekennzeichnet, daß die Impedanz eine erste Transformatorwicklung (T10a) umfaßt, die einen ersten Anschluß (90) aufweist, der mit der ersten, den Hauptstrom leitenden Elektrode (D) des ersten Schalteistungstransistors (Q10) verbunden ist, einen zweiten Schalteistungstransistor (Q20), der eine erste den Hauptstrom leitende Elektrode (D) aufweist, die mit einem zweiten Anschluß (91) der ersten Transformatorwicklung (T10a) verbunden ist, der vom ersten Schalteistungstransistor (Q10) entfernt ist, um einen zweiten Schaltstrom in den zweiten Schalteistungstransistor (Q20) zu leiten, und der eine Steuerelektrode aufweist, die auf ein Steuersignal (V2b) mit einer Frequenz reagiert, die zu der des ersten Steuersignales (V2a) in Beziehung steht, derart, daß der erste (Q10) und der zweite (Q20) Schalteistungstransistor im Gegentakt arbeiten, und wobei das zweite Mittel (51) mit der ersten den Hauptstrom leitenden Elektrode (D) des ersten (Q10) und des zweiten (Q20) Schalteistungstransistors verbunden ist, um das zweite Stromabtastsignal (VSUM) zu erzeugen, das einen Überstrom im ersten (Q10) oder zweiten (Q20) Schalteistungstransistor anzeigt.

6. Vorrichtung nach Patentanspruch 5, dadurch gekennzeichnet, daß das zweite Mittel eine erste (D20) und eine zweite (D30) Diode enthält, wobei die erste Diode (D20) einen ersten Anschluß aufweist, der mit der ersten den Hauptstrom leitenden Elektrode (D) des ersten Schalteistungstransistors (Q10) verbunden ist, und die zweite Diode (D30) einen ersten Anschluß aufweist, der mit der ersten den Hauptstrom leitenden Elektrode (D) des zweiten Schalteistungstransistors (Q20) verbunden ist, und Kombiniermittel (R6,

R7), die mit den Dioden (D20, D30) verbunden sind, um das zweite Stromabtastsignal (VSUM) in Übereinstimmung mit einem Signal (VS10) zu bilden, das an einem zweiten Anschluß der ersten Diode (D20) entsteht, und in Übereinstimmung mit einem Signal (VS20), das an einem zweiten Anschluß der zweiten Diode (D30) entsteht.

7. Vorrichtung nach Patentanspruch 5, gekennzeichnet durch eine Gleichrichteranordnung (D4, D5), die mit der ersten Wicklung (T10a) verbunden ist, um eine erste Ausgangsgleichspannung (VDG) in einem Kondensator (C10) zu erzeugen, und ein drittes schaltendes Mittel (D30), das auf ein Signal reagiert, das an einer zweiten Wicklung (T10b) des Transformators (T10) entsteht, um diese erste Ausgangsgleichspannung im Normalbetrieb an einen Ausgang (77) des genannten dritten Mittels (Q30) anzulegen und um den Ausgang (77) vom Kondensator (C10) zu trennen, wenn ein Fehler entsteht.

8. Vorrichtung nach Patentanspruch 1, gekennzeichnet durch Verzögerungsmittel (U3b), die auf das zweite Stromabtastsignal (VSUM) reagieren, um ein Signal (V3BOUT) zu erzeugen, das die Wiederaufnahme des Schaltbetriebes im ersten Schalteistungstransistor (Q10) erst nach einem Zeitraum, der mindestens eine vorgegebene Länge hat, nach Auftreten des zweiten Steuersignales (INHIBIT) freigibt, der ausreichend ist, um den ersten Schalteistungstransistor vor Beschädigung zu bewahren.

Revendications

1. Dispositif de détection et de protection contre les erreurs dans un bloc d'alimentation et de commutation comprenant :
une source de tension de secteur à l'entrée (B+);
un premier transistor de puissance de commutation (Q1) ayant une première (D) et une seconde électrode (S) conductrice de courant principal et une électrode de commande (G) ;
une source (50) d'un premier signal de commande (VG) à une fréquence donnée qui est couplé à ladite électrode de commande du premier transistor de puissance de commutation mentionné (Q1) pour provoquer, pendant le fonctionnement normal, le fonctionnement du premier transistor de commutation mentionné (Q1) à une fréquence de commutation déterminée en accord avec ladite fréquence donnée ;
un circuit d'utilisation (T1) comprenant une impédance (T1a) couplée à ladite tension de secteur à l'entrée et à ladite première électrode conduc-



trice de courant principal pour former une tension de secteur de sortie (VRL) dans ledit circuit d'utilisation, ladite impédance (T1a) formant un trajet de courant vers un courant principal commuté (I1) qui passe dans ledit premier transistor de puissance de commutation (Q1) pour former un premier signal balayeur de courant (VQ1) à une fréquence déterminée en accord avec ladite fréquence donnée et qui est formé entre les première (D) et seconde (S) électrodes conductrices de courant principal du premier transistor de puissance de commutation mentionné (Q1) lorsque ledit premier transistor de puissance de commutation (Q1) est conducteur, ledit premier courant de balayage de courant (VQ1) étant indicateur d'un niveau du courant principal mentionné lorsque ledit premier transistor de puissance de commutation (Q1) est conducteur ; caractérisé par un premier organe (Q2) sensible au premier signal de commande mentionné (VG) et au premier signal de balayage de courant mentionné (VQ1) et ayant une résistance (R1) qui est couplée à ladite première électrode conductrice de courant principal (D) pour générer à une borne de sortie (Q2a) une première portion d'un second signal de balayage de courant (VQ2) qui est indicateur de l'intensité du courant principal mentionné (I1) lorsque ledit premier transistor de puissance de commutation (Q1) est à un état conducteur et pour découpler ladite borne de sortie (Q2a) du transistor de puissance mentionné (Q1) lorsque ledit premier transistor de puissance de commutation (Q1) est à un état non conducteur pour empêcher une tension (VQ1) qui est formée à ladite première électrode conductrice de courant principal (D) du premier transistor de puissance de commutation mentionné (Q1), lorsque ledit transistor de puissance n'est pas conducteur, d'avoir une contribution substantielle à une amplitude du second signal de balayage de courant mentionné (VQ2) et un second organe (51) sensible au second signal de détection de courant mentionné (VQ2) pour générer un second signal de commande (INHIBIT) lorsqu'une intensité de ladite première portion du second signal balayeur de courant mentionné (VQ2) est en dehors d'une plage de fonctionnement normal indiquant l'apparition d'un état d'erreur dans ledit bloc d'alimentation, ledit second signal de commande (INHIBIT) étant couplé à ladite source (50) du premier signal de commande mentionné (VG) commandant ledit premier transistor de puissance de commutation (Q1) pour empêcher que le premier transistor de puissance de commutation mentionné (Q1) continue à être conducteur.

2. Dispositif selon la revendication 1, caractérisé en ce que ledit premier organe comprend un second transistor de commutation (Q2) ayant une électrode de commande qui est couplée au premier signal de commande mentionné (VG) et une électrode conductrice de courant principal qui est couplée par ladite résistance (R1) à ladite première électrode conductrice de courant principal (D) du premier transistor de puissance de commutation mentionné (Q1) pour former ledit second signal balayeur de courant (VQ2) à ladite électrode conductrice de courant principal du second transistor de commutation mentionné (Q2) de telle manière que, lorsque ledit premier transistor de puissance de commutation (Q1) est conducteur, ledit second transistor de commutation (Q2) n'est pas conducteur et vice-versa.
3. Dispositif selon la revendication 1, caractérisé en ce que ledit premier organe (Q2) fonctionne à une fréquence qui est apparentée à celle du premier signal de commande mentionné (VG) et en ce que, lorsque ledit premier transistor de puissance de commutation (Q1) n'est pas conducteur, ledit premier organe (Q2) fait en sorte que ledit second signal balayeur de courant (VQ2) soit à une valeur constante prédéfinie qui est substantiellement plus basse que celle de ladite première portion du second signal balayeur de courant mentionné (VQ2).
4. Dispositif selon la revendication 1, caractérisé en ce que ledit premier organe comprend une diode (D2') ayant une première borne qui est couplée à ladite première électrode conductrice de courant principal (D) du premier transistor de puissance de commutation mentionné (Q1) pour former ledit second signal balayeur de courant (VD2') à une seconde borne de la dite diode (D2') de telle manière que, lorsque ledit premier transistor de puissance de commutation (Q1) est conducteur, ladite diode (D2') est polarisée en sens direct et que, lorsque ledit premier transistor de puissance de commutation (Q1) n'est pas conducteur, ledit premier signal balayeur de courant (VQ1) qui est formé à ladite première électrode conductrice de courant principal (D) du premier transistor de puissance de commutation mentionné (Q1) polarise en sens inverse ladite diode (D2') pour découpler ladite électrode conductrice de courant principal (D) du premier transistor de puissance de commutation mentionné (Q1) de ladite seconde borne (anode) de ladite diode (D2').
5. Dispositif selon la revendication 1, caractérisé en ce que ladite impédance comprend un premier enroulement de transformateur (T10a)



ayant une première borne (90) qui est couplée à ladite première électrode conductrice de courant principal (D) du premier transistor de puissance de commutation mentionné (Q10), un second transistor de puissance de commutation (Q20) ayant une première électrode conductrice de courant principal (D) qui est couplée à une seconde borne (91) du premier enroulement de transformateur mentionné (T10a) qui est éloigné du premier transistor de puissance de commutation mentionné (Q10) pour conduire un second courant de commutation dans ledit second transistor de puissance de commutation (Q20) et ayant une électrode de commande qui est sensible à un signal de commande (V2b) à une fréquence qui est apparentée à celle du premier signal de commande mentionné (V2a) de telle manière que ledit premier (Q10) et ledit second (Q20) transistor de commutation fonctionnent en push-pull et dans lequel ledit second organe (51) est couplé à ladite première électrode conductrice de courant principal (D) des premier (Q10) et second (Q20) transistors de puissance de commutation mentionnés pour générer ledit second signal balayeur de courant (VSUM) qui est indicateur d'un état de courant de surcharge dans l'un ou l'autre des premier (Q10) et second (Q20) transistors de puissance de commutation mentionnés.

6. Dispositif selon la revendication 5, caractérisé en ce que ledit second organe comprend une première (D20) et une seconde (D30) diodes, ladite première diode (D20) ayant une première borne qui est couplée à ladite première électrode conductrice de courant principal (D) du premier transistor de puissance de commutation mentionné (Q10) et ladite seconde diode (D30) ayant une première borne qui est couplée à ladite première électrode conductrice de courant principal (D) du second transistor de puissance de commutation mentionné (Q20) et un organe de combinaison (R6, R7) couplé aux diodes mentionnées (D20, D30) pour former ledit second signal balayeur de courant (VSUM) en accord avec un signal (VS10) qui est formé à une seconde borne de ladite première diode (D20) et en accord avec un signal (VS20) qui est formé à une seconde borne de ladite seconde diode (D30).

7. Dispositif selon la revendication 5, caractérisé par un arrangement redresseur (D4, D5) couplé au premier enroulement mentionné (T10a) pour générer une première tension de sortie directe (VDG) dans un condensateur (C10) et un troisième organe de commutation (D30) sensible à un signal qui est formé à un second enroulement (T10b) du transformateur mentionné (T10) pour coupler ladite première tension de sortie continue

à une borne de sortie (77) du troisième organe mentionné (Q30) pendant le fonctionnement normal et pour presque découpler ladite borne de sortie (77) du condensateur mentionné (C10) lorsqu'un état d'erreur apparaît.

8. Dispositif selon la revendication 1, caractérisé par un élément de retard (U3b) sensible au second signal balayeur de courant mentionné (VSUM) pour générer un signal (V3BOUT) qui valide la reprise de l'opération de commutation dans ledit premier transistor de puissance de commutation (Q10) seulement après qu'une période ayant au moins une longueur prédéterminée se soit écoulée suivant l'intervention du second signal de commande mentionné (INHIBIT) qui est suffisant pour empêcher un dommage au premier transistor de puissance de commutation mentionné (Q10).

