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SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND FABRICATION METHOD THEREOF

This invention relates to a semiconductor integrated circuit device (hereinafter simply referred to as an "IC") including an I^2L (Integrated Injection Logic) element portion having an inverse transistor and a bipolar circuit element portion having a normal transistor. It also relates to a method of fabricating the IC.

The term "inverse transistor" herein denotes a transistor having a structure in which a semiconductor body such as a semiconductor substrate or a semiconductor layer (epitaxial layer) is used as its emitter region, a first semiconductor region formed in the semiconductor body is used as the base region and a second semiconductor region formed in the first semiconductor region is used as the collector region. On the other hand, the term "normal transistor" herein denotes a transistor having a structure in which the above-mentioned second semiconductor region is used as the emitter region, the above-mentioned first semiconductor region is used as the base region and the above-mentioned semiconductor body is used as the collector region.

When an I^2L element and a linear or digital circuit element are to be separately disposed on a common epitaxial

layer, there is a problem, in that the current amplification factor β_i of the inverse transistor of the I^2L element increases with decreasing thickness of the epitaxial layer, whereas the collector-to-emitter or collector-to-base breakdown voltage in the linear circuit element having a normal vertical transistor structure increases with increasing thickness of the epitaxial layer. Therefore, in order to have both elements present together on a common epitaxial layer, it is necessary to sacrifice either the current amplification factor or the breakdown voltage, according to the thickness chosen for the epitaxial layer.

A problem therefore resides in providing an IC of a composite element type in which both kinds of transistors are disposed on a single semiconductor substrate without lowering either the current amplification factor of the inverse transistor or the withstand voltage of the normal transistor.

Furthermore, it is desirable to provide a method of fabricating the above-mentioned IC with a high level of reproducibility.

In a first aspect the present invention provides a semiconductor integrated circuit device wherein an inverse transistor element and a normal transistor element are formed in adjacent portions of a common semiconductor layer which is disposed on a common semiconductor substrate, said adjacent portions being separated from each other by

an oxide layer penetrating said semiconductor layer in the direction of its thickness, and wherein said adjacent portions each include a surface oxide film with the thickness of the surface oxide film of said inverse transistor element portion being greater than that of the surface oxide film of said normal transistor element portion so that said inverse transistor element portion of said semiconductor layer is thinner than said normal transistor element portion of said semiconductor layer.

In a second aspect the invention provides a method of fabricating a semiconductor integrated circuit device comprising:

(a) oxidizing predetermined regions of a semiconductor layer to an intermediate depth of said semiconductor layer in the direction of its thickness thereby to separate said semiconductor layer into a first region in which a normal transistor is to be formed and a second region in which an inverse transistor is to be formed;

(b) covering the first region in which a normal transistor element portion is to be formed with an oxidation- resistant mask while leaving the second region in which said inverse transistor is to be formed uncovered; and

(c) oxidizing uncovered parts of said semiconductor layer, including said oxidised predetermined regions and said second region of said semiconductor layer, to make said oxidised predetermined regions penetrate through said semiconductor layer in the direction of its thickness and, at the same time, to make a surface oxide film on said second region of said semiconductor layer thicker than a surface oxide film on said first region of said semiconductor layer so that said second region is made thinner than said first region.

In the drawings:

Figures 1A through 1G are sectional views showing the principal portions of an I^2L - linear element co-presence type IC in accordance with an embodiment of the present invention at various stages of the production process, and

Figures 2A through 2B are sectional views showing another embodiment of the present invention.

Hereinafter, an embodiment in which the present invention is applied to a composite type IC including an I^2L circuit element portion having an inverse transistor and a linear transistor circuit element portion having a normal transistor will be described with reference to the drawings.

The IC of this embodiment will be explained according to its production steps. First, as depicted in Figure 1A, an N^- type epitaxial layer 3 is grown to a thickness of 1.8 to 2.0 μm on a P type Si substrate 1 over an N^+ type buried layer 2. The surface of this epitaxial layer 3 is thermally oxidized to grow a thin protective SiO_2 film 4. Then, a

Si_3N_4 film is grown on the SiO_2 film 4 by vapor growth and shaped in predetermined patterns 5a and 5b by ordinary photoprocessing. In this case, the Si_3N_4 film 5a covers a portion where a bipolar transistor will be formed while the Si_3N_4 film 5b covers a portion where the I^2L element will be formed.

Next, as shown in Figure 1B, the SiO_2 film 4 and the epitaxial layer 3 below these Si_3N_4 films 5a, 5b are selectively etched to a depth of 0.6 to 1.2 μm using the films 5a, 5b as a mask, forming a recess 6 for LOCOS oxidation (local oxidation).

Subsequently, Si in the recess 6 is thermally oxidized using the Si_3N_4 films 5a, 5b as a mask as shown in Figure 1C so as to form a relatively thick SiO_2 layer 7 which extends into the epitaxial layer 3 in the direction of its thickness. This SiO_2 layer 7 surrounds each element region (i.e. the inverse transistor and the normal transistor) and separates them from one another. The oxidizing condition for growing the SiO_2 layer 7 is a temperature of 1,000°C. for a period of 5 hours in wet O_2, for example.

Next, as shown in Figure 1D, a photoresist 8 is deposited by ordinary techniques so as to cover a region in which the normal transistor of the bipolar transistor circuit element portion is to be formed. The Si_3N_4 film 5b on the I^2L side that is not covered with the photoresist 8 is selectively removed by exposure to CF_4 plasma, exposing the original SiO_2 film 4 at that portion.

Next, as shown in Figure 1E, the surface is successively thermally oxidized to extend the SiO_2 layer 7 until it penetrates epitaxial layer 3, thereby growing a thick SiO_2 layer 9 separating the epitaxial layer 3 into the element regions 3a and 3b. This process is referred to as "LOCOS oxidation", and the SiO_2 layer 9 thus obtained functions as an isolating film. Simultaneously with this LOCOS oxidation, the region 3b is oxidized so that the thin SiO_2 film 4 grows into a relatively thick thermal oxidation SiO_2 film 10 as shown in the drawing. This oxidation may be performed at a temperature of 1,000°C. for a period of three hours in wet O_2. By this treatment, the thickness of the SiO_2 film 10 becomes 0.5 to 0.7 μm. Consequently, the difference between the thickness of the surface SiO_2 film 4 of the region 3a of the bipolar transistor circuit element portion and the thickness of the surface SiO_2 film 10 of the inverse transistor region 3b of the I^2L circuit element portion becomes approximately 0.3 μm, for example, at this time. This difference is considerable since the original epitaxial layer 3 is extremely thin, i.e., 1.8 to 2.0 μm.

Next, as shown in Figure 1F, after the Si_3N_4 film 5a is removed by plasma etching as described above, windows are bored in the SiO_2 surface films 4 and 10 by an ordinary photoprocess, and a P type impurity such as boron vapor

is diffused through the thus-formed openings. This forms a P type semiconductor region 11 to serve as the base in the region 3a, and P^+ semiconductor regions 12 and 13 to serve as the injector and base, respectively, of the inverse transistor in the region 3b.

As shown in Figure 1G, the surface of each SiO_2 film 4 and 10 is further selectively etched using an ordinary photoprocess, and an N type impurity such as phosphorous is diffused in the gaseous phase through each opening thus formed. In this manner, region 3a an N^+ ohmic contact region 14 is formed for taking out a collector electrode, and an N^+ semiconductor region 15 is formed to serve as the emitter. In region 3b an N^+ ohmic contact region 16 is formed to take out the emitter electrode of the inverse transistor, and an N^+ semiconductor region 17 is formed as a multicollector. The SiO_2 films 4 and 10 on the surface are left as passivation films, but the surfaces of these films 4 and 10 are preferably treated with phosphorous to stabilize them. Though not shown in the drawing, an opening is formed in the surface of each SiO_2 film by an ordinary photoprocess, and electrodes are then fitted into these openings (by patterning after vacuum evaporation Aℓ on the entire surface, for example). Also an Aℓ upper wiring layer is provided, with the necessary inter-layer insulating film, thereby completing the IC. The Aℓ wiring layer and the insulating film have been omitted from the drawings for clarity, since their formation is well known in the art.

In accordance with the thus formed composite type IC in which the I^2L circuit element portion and the linear (bipolar) circuit element portion are both present, the thickness of the epitaxial layer 3b of the I^2L circuit element portion is considerably smaller than that of the epitaxial layer 3a of the linear circuit element portion due to the difference between the thicknesses of SiO_2 films 10 and 4. For this reason, the current amplification ratio β_i of the inverse transistor in the I^2L circuit element portion can be made large while retaining the breakdown voltage of the normal vertical transistor in the linear circuit element portion at a high level. Hence, both requirements for a high amplification factor and for a high breakdown voltage can be satisfied in the same chip. Further, an IC with these excellent characteristics can be easily fabricated by carrying out LOCOS oxidation over two stages as described above. Moreover, in this case, if the oxidizing conditions (especially the oxidation time) in the step shown in Figure 1D are suitably set, the difference between the thicknesses of epitaxial layers 3a and 3b can be controlled arbitrarily and with a high level of reproducibility. Accordingly, the structure and method in accordance with this embodiment are extremely effective when the epitaxial layer for forming each element is extremely thin.

In particular, because the impurity concentration distribution

in the direction of depth of the I^2L inverse transistor changes sharply between the semiconductor regions, the current amplification factor can also be improved in this respect. This advantage results from the fact that the thickness of the epitaxial layer 3b is reduced in this embodiment by growing the thick SiO_2 film on the surface as described above, and therefore high concentration post-diffusion of the N type impurity inside the same layer does not occur. If the phosphorous inside the N^+ buried layer 2 is post-diffused up into the epitaxial layer 3b in order to reduce the effective thickness of the epitaxial layer 3b, the change in the impurity concentration along the direction of thickness is only gradually graded towards the base side (13) due to the post-diffusion, and hence the current amplification ratio β_i becomes lower.

In the present embodiment, since the thickness of the semiconductor layer of the I^2L circuit element portion is made smaller than that of the normal bipolar circuit element portion already described, high current amplification ratio of the former and high breakdown voltage of the latter can be simultaneously accomplished on the same chip. Moreover, these requirements can be easily satisfied with a high level of reproducibility or controllability by suitably selecting the oxidizing conditions when performing the surface oxidation. This is

especially effective when the epitaxial layer is thin.

The present embodiment also ensures especial isolation between the circuit elements by the insulating film so that no parasitic transistor is likely to be formed. The integration density can also be improved in comparison with PN junction isolation.

Though the present invention is explained with reference to the above-mentioned embodiment, various modifications can be made on the basis of the technical concept of the present invention. For example, in the step shown in Figure 1D, the Si_3N_4 film 5b may be removed by etching with hot phosphoric acid in liquid phase. In such a case, it is preferred that an SiO_2 film be disposed by a chemical vapor growth process between the photoresist 8 and the Si_3N_4 film 5a. In the same figure, the Si_3N_4 film 5a may also be removed and an oxidation-resistant mask may be applied to that portion. The semiconductor type of each of the above-mentioned semiconductor regions may be suitably changed if desired.

As another embodiment of the present invention, the following method is proposed. Namely, after the step shown in Figure 1E is completed, the SiO_2 films 4 and 10 formed on the surface of the regions 3a and 3b are removed by etching, as shown in Figure 2A. Then, as shown in Figure 2B, insulating films 20a and 20b of a desired thickness are formed on the exposed surface of the regions 3a and 3b. Thereafter, the steps shown in Figures 1F and 1G are carried out, in order to form the various regions of the respective transistors.

Most preferably, the insulating films 20a and 20b are SiO_2 films formed by oxidizing the surface of the regions 3a and 3b. However, if desired, they may be oxide films formed by a CVD (chemical vapor deposition) process.

In any event, in accordance with this method, the insulating films 20a and 20b formed on the surface of the regions 3a and 3b are equal to each other so that simultaneous etching of these insulating films 20a and 20b can be readily be accomplished.

In the step shown in Figure 1D in each of the above-mentioned embodiments, the photoresist 8 may be left as such and an N type such as phosphorous may be introduced into the epitaxial layer 3b through the thin SiO_2 film 4 so as to reach the N^+ type buried layer 2. Introduction of the N type impurity into the epitaxial layer 3b makes it possible to increase the speed of the I^2L circuit element. In this regard, it should be noted that since no mask is necessary for introducing the N type impurity, increasing the speed of the I^2L circuit element can easily be accomplished.

CLAIMS:

1. A semiconductor integrated circuit device wherein an inverse transistor element and a normal transistor element are formed in adjacent portions of a common semiconductor layer which is disposed on a common semiconductor substrate, said adjacent portions being separated from each other by an oxide layer penetrating said semiconductor layer in the direction of its thickness, and wherein said adjacent portions each include a surface oxide film with the thickness of the surface oxide film of said inverse transistor element portion being greater than that of the surface oxide film of said normal transistor element portion so that said inverse transistor element portion of said semiconductor layer is thinner than said normal transistor element portion of said semiconductor layer.

2. A method of fabricating a semiconductor integrated circuit device comprising:

(a) oxidizing predetermined regions of a semiconductor layer to an intermediate depth of said semiconductor layer in the direction of its thickness thereby to separate said semiconductor layer into a first region in which a normal transistor is to be formed and a second region in which an inverse transistor is to be formed;

(b) covering the first region in which a normal transistor element portion is to be formed with an oxidation- resistant mask while leaving the second region in which said inverse transistor is to be formed uncovered; and

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(c) oxidizing uncovered parts of said semiconductor layer, including said oxidised predetermined regions and said second region of said semiconductor layer, to make said oxidised predetermined regions penetrate through said semiconductor layer in the direction of its thickness and, at the same time, to make a surface oxide film on said second region of said semiconductor layer thicker than a surface oxide film on said first region of said semiconductor layer so that said second region is made thinner than said first region.

3. A method of fabricating a semiconductor integrated circuit device according to claim 2, further comprising removing the surface oxide films of uneven thickness after step (c) and forming surface oxide films of equal thickness on both the first and second regions of the semiconductor layer.

4. A method according to claim 2 or claim 3 including a preliminary step of etching a recess in said semiconductor layer in said predetermined regions.

5. A method of fabricating a semiconductor integrated circuit, substantially as any described herein with reference to the accompanying drawings.

6. A semiconductor integrated circuit made by a method according to any one of claims 2 to 5.

7. A semiconductor integrated circuit substantially as any described herein with reference to the accompanying drawings.