Claims

1. A method for simulating a power line carrier communication system, wherein the method comprises the following steps:

S1. constructing simulation models of a sending end, a receiving end, and power line channels of a power line carrier communication system;

S2. sending test data to the constructed simulation model of the sending end, and obtaining and displaying the simulation result data;

wherein, the simulation model of the sending end comprises a channel encoding model, and the channel encoding model comprises: a simulation model of an ARM core chip and a peripheral logic circuit of the ARM core chip, and a simulation model of a RS error correction encoding algorithm of the ARM core chip; the simulation model of the receiving end comprises a channel decoding model, and the channel decoding model comprises: a simulation model of the ARM core chip and a peripheral logic circuit of the ARM core chip, and a simulation model of a RS error correction decoding algorithm of the ARM core chip.

2. The method as claimed in claim 1, wherein, the simulation model of the sending end further comprises:

a carrier modulation model, the carrier modulation model comprises a simulation model of a PLC chip and a algorithm simulation model of the PLC chip;

a cyclic prefix adding algorithm model coupled with the carrier modulation model;

an guard interval inserting algorithm model coupled with the cyclic prefix adding algorithm model; and

a parallel/serial conversion algorithm model coupled with the guard interval inserting algorithm model and simulation model of power line channel.

3. The method as claimed in claim 2, wherein, the ARM core chip is a STM32 chip, and the simulation model of the receiving end further comprises:

a parallel/serial conversion algorithm model coupled with the simulation model of power line channel;

a guard interval removing algorithm model coupled with the parallel/serial conversion algorithm model;

a cyclic prefix removing algorithm model coupled with the guard interval removing algorithm model;

a channel equalization model coupled with the cyclic prefix removing algorithm model;

a channel estimation algorithm model coupled between the cyclic prefix removing algorithm model and the channel equalization model;

a zero removing algorithm model coupled with the channel equalization model;

a carrier demodulation model coupled with the zero removing algorithm model; and

a channel decoding model coupled with the carrier demodulation model.

4. The method as claimed in claim 3, wherein, the method further comprises:

S0: before or after step S1, constructing a first bit error rate calculation algorithm model and a second bit error rate calculation algorithm model;

wherein, the first bit error rate calculation algorithm model is configured for coupling channels between the channel encoding model and the carrier modulation model, and coupling channels between channel decoding model and the carrier demodulation model; and the second bit error rate calculation algorithm model is configured for coupling channels between the carrier modulation model and the cyclic prefix adding algorithm model, and coupling channels between the carrier demodulation model and zero removing algorithm model.

5. The method as claimed in any one of claims 1 to 4, wherein, the simulation model of the power line channel comprises:

a multi-path attenuation channel model;

a Gaussian white noise channel model coupled with the multi-path attenuation channel model;

a noise interference model, the noise interference model comprises: a colored background noise model, a narrowband noise model, a periodic pulse noise model

synchronous to the power frequency, and a periodic pulse noise model asynchronous to the power frequency, and a random pulse noise model; and

an additive algorithm model coupled with the Gaussian white noise channel model and the noise interference model.

6. A system for simulating a power line carrier communication system, wherein the system comprises:

a simulation model constructing module configured for constructing simulation models of a sending end, a receiving end and power line channels of a power line carrier communication system;

a simulation execution module, configured for sending test data to the simulation model of the sending end constructed by the simulation model constructing module and obtaining and displaying the simulation results data;

wherein, the simulation model of the sending end comprises: a channel encoding model, and the channel encoding model comprises: a simulation model of an ARM core chip and a peripheral logic circuit of the ARM core chip, and a simulation model of a RS error correction encoding algorithm of the ARM core chip; the simulation model of the receiving end comprises: a channel decoding model, and the channel decoding model comprises: a simulation model of an ARM core chip and a peripheral logic circuit of the ARM core chip, and a simulation model of a RS error correction decoding algorithm of the ARM core chip.

7. The system as claimed in claim 6, wherein, the simulation model of the sending end further comprises：

a carrier modulation model, the carrier modulation model comprises a simulation model of a PLC chip and a simulation model of the algorithm of the PLC chip;

a cyclic prefix adding algorithm model coupled with the carrier modulation model;

an guard interval inserting algorithm model coupled with the cyclic prefix adding algorithm model; and

a parallel/serial conversion algorithm model coupled with the guard interval inserting algorithm model and simulation model of power line channel.

8. The system as claimed in claim 7, wherein the ARM core chip is a STM32 chip, and the simulation model of the receiving end further comprises:

a parallel/serial conversion algorithm model coupled with the simulation model of power line channel;

a guard interval removing algorithm model coupled with the parallel/serial conversion algorithm model;

a cyclic prefix removing algorithm model coupled with the guard interval removing algorithm model;

a channel equalization model coupled with the cyclic prefix removing algorithm model;

a channel estimation algorithm model coupled between the cyclic prefix removing algorithm model and the channel equalization model;

a zero removing algorithm model coupled with the channel equalization model;

a carrier demodulation model coupled with the zero removing algorithm model; and

a channel decoding model coupled with the carrier demodulation model.

9. The system as claimed in claim 8, wherein the simulation model constructing module is further configured for constructing a first bit error rate calculation algorithm model and a second bit error rate calculation algorithm model;

wherein, the first bit error rate calculation algorithm model is configured for coupling channels between the channel encoding model and the carrier modulation model, and coupling channels between channel decoding model and the carrier demodulation model; the second bit error rate calculation algorithm model is configured for coupling channels between the carrier modulation model and the cyclic prefix adding algorithm model, and coupling channels between the carrier demodulation model and zero removing algorithm model.

10. The system as claimed in any one of claims 6 to 9, wherein, the simulation

model of the power line channel comprises:

a multi-path attenuation channel model;

a Gaussian white noise channel model coupled with the multi-path attenuation channel model;

a noise interference model,

the noise interference model comprises: a colored background noise model, a narrowband noise model, a periodic pulse noise model synchronous to the power frequency, and a periodic pulse noise model asynchronous to the power frequency and a random pulse noise model; and

an additive algorithm model coupled with the Gaussian white noise channel model and the noise interference model.